

Power balancing control strategies for the cascaded H-bridge multilevel DSTATCOM

Abstract. This paper proposes a novel power balancing control scheme for the cascaded H-bridge (CHB) DSTATCOM. The principle of the carrier phase-shifted pulse-width modulation (CPS-PWM) and the mathematical model of the CHB-DSTATCOM are presented. The power balancing mechanism and the stable control region are analyzed using the phasorial diagram representation. The current loop controller is designed by using root locus approach, and the dc-link voltage balancing controller is synthesized based on the devised power balancing mechanism. The simulation results obtained from the alternative transient program (ATP) are presented and evaluated. The validity and effectiveness of the control scheme is confirmed by the simulation and experimental results.

Streszczenie. Zaproponowano nowa metode równoważenia mocy w kaskadowym H-mostkowym SSTATCOM. Zaprezentowano zasadę modulacji przesunięcia fazowego i szerokości impulsu CPS-PWM i model matematyczny CHB-DSTATCOM. Równoważenie mocy i analiza stabilnego sterowania zostały przeprowadzone przy użyciu diagramu fazowego. Kontroler pętli prądowej został zaprojektowany przy użyciu obwiedni pierwiastkowej a kontroler napięcia dc-link jest syntetyzowany na podstawie balansu mocy. Przedstawiono symulowane rezultaty. Symulacje i eksperymenty potwierdziły skuteczność metody. **(Strategie równoważenia mocy w kaskadowym wielopoziomowym mostkowym DSTATCOM)**

Keywords: DSTATCOM, cascaded H-bridge, multilevel inverter, power balancing, alternative transient program (ATP)

Słowa kluczowe: DSTATCOM, przekształtnik wielopoziomowy, równoważenie mocy.

I. Introduction

In recent years, the power quality issues have become important topic due to the proliferation of disturbing loads, which causes significant voltage fluctuations, sag/swell and temporary interruptions [1-5, 12, 16]. To mitigate the voltage disturbance problems, the static synchronous compensator (STATCOM) are the most suitable solutions, which can be installed at the transmission networks or at the distribution networks to protect the voltage sensitive loads [6-10].

Due to its modularity and flexibility of manufacturing, the cascaded H-bridge (CHB) multilevel inverter topology is appreciated for high-power medium-voltage power quality conditioning applications [3, 4]. However, restricted by the limited switching frequency of the power electronic devices, achieving simultaneous dc-link voltage balancing and sufficient controller bandwidth is rather complicated [10]. The systematical design guidelines for CHB-DSTATCOM have not been reported in the previous literatures. Hence, this paper aims to cover this gap. The analysis for the active and reactive power distribution between the two cells is presented. Based on the power balancing mechanism, a novel dc-link voltage control scheme is proposed by splitting the control task into two parts, i.e., the average voltage controller (AVC) and the voltage balancing controller (VBC).

The organization of this paper is as follows. Section II presents the principle of carrier phase-shifted pulse-width modulation (CPS-PWM) for the CHB-DSTATCOM. Section III presents the mathematical modeling of the system using state-space equation. Section IV presents the analysis for the power balancing among the individual inverters for the CHB-DSTATCOM and the control methodology synthesis is presented in Section V. The simulation results obtained from the Alternative Transient Program (ATP/EMTP) are presented in Section VI. The experimental results are given in Section VII. Finally, Section VIII concludes this paper.

II. Carrier Phase-Shifted Pulse-width Modulation (CPS-PWM) of the CHB-DSTATCOM

Fig.1 shows the circuit diagram of the five-level cascaded multilevel DSTATCOM based on two H-bridge modules. In Figure 1, L_g and R_g indicate the line impedance. Each H-bridge includes four IGBT switches with anti-parallel diodes and a dc-link capacitor. Thus the output voltages of the CHB-DSTATCOM can be derived as: $v_{aN} = v_{a1} + v_{a2}$.

Assuming $v_{dc1} = v_{dc2} = V_{dc}$ in steady state and the unipolar modulation scheme is adopted in the PWM process, thus each H-bridge would produce three voltage levels: $-V_{dc}$, 0 , V_{dc} . With reference to the upper bridge, it is possible to set $v_{a1} = +V_{dc}$ by turning on switches S_{11} and S_{14} and $v_{a1} = -V_{dc}$ by turning on switches S_{12} and S_{13} . Moreover, it is possible to set $v_{a1} = 0$ by turning on either S_{11} and S_{12} or S_{13} and S_{14} , the lower bridge operates in a similar manner. Thus five distinct voltage levels can be synthesized at the ac terminals. It is worth noticing that, the switching states of S_{x1}, S_{x2} ($x=1, 2, 3$) must be complementary to those of S_{x3}, S_{x4} ($x=1, 2, 3$) in order to avoid short circuit of the H-bridges [2-4, 9, 10, 16].

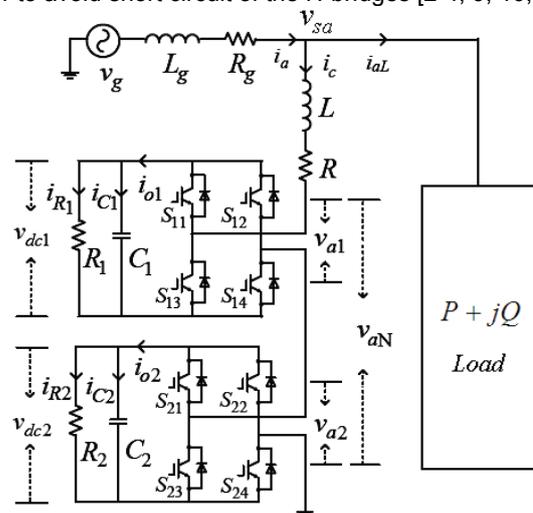


Fig.1 Block diagram of the cascaded H-bridge (CHB) DSTATCOM.

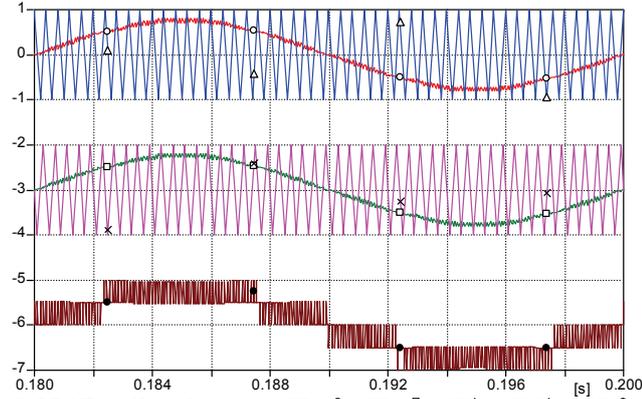
To obtain five level output voltage at the ac terminal, the carrier signals utilized in each cell must be phase shifted by 90 degree in case of two H-bridge module configuration. Fig.2(a) shows the waveforms of the modulation signal, phase-shifted carriers and the output multilevel voltage of the CHB-DSTATCOM. Fig.2(b) shows the enlarged view of Fig.2(a) including the gating signals of the first IGBT for each H-bridge inverter.

Notably, the variables in this paper are as follows:

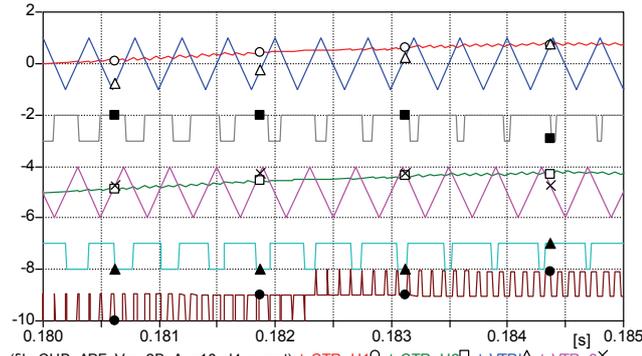
- t:CTR_H1→The modulation signal of the first cell;
- t:CTR_H2→ The modulation signal of the second cell;
- t:VTRI→The carrier signal of the first cell;

t:VTR_2→ The carrier signal of the second cell;
v: 'VOUT -'→The synthesizes multilevel voltage 'v_{an}';
t: 'SIG1'→The gating signal for IGBT S11;
t: 'SIG5'→The gating signal for IGBT S21;
t:VBC_H1→The output of the first VBC controller;
t:VBC_H2→The output of the second VBC controller;
t:P1, t:P2→The output of the average voltage controller;
t:VDC1→The dc-link voltage in the first inverter;
t:VDC2→The dc-link voltage in the second inverter;
c: 'SA -MA'→The grid side current;
t: IS_REF →The reference signal for the grid current;
t: IS_ERR →The grid side tracking error;

It should be noticed that, the scaling factors and offsets of these signals are marked at the bottom of each figure.



(a)



(b)

Fig.2 The simulated waveforms of the CHB-DSTATCOM: (a) The waveform of the modulation signal, phase-shifted carriers and the output multilevel voltage; (b) The enlarged view of (a) including the gating signals of the first IGBT for each H-bridge inverter.

III. Mathematical Modelling of the CHB-DSTATCOM

Referring to Fig. 1, the switching functions of the multilevel CHB-DSTATCOM can be derived as [9, 10, 16]:

$$(1) \quad \begin{cases} f_1 = S_{11} \cdot S_{14} - S_{12} \cdot S_{13} \\ f_2 = S_{21} \cdot S_{24} - S_{22} \cdot S_{23} \end{cases}$$

The value of f_x ($x=1, 2$) indicates the dynamic process of charging and discharging between the dc-link capacitors C_1 and C_2 . Supposing the DSTATCOM current i_c is positive, then the capacitor C_x ($x=1, 2$) is charging if $f_x=1$, discharging if $f_x=-1$, and not undergoing any of these processes if $f_x=0$. Complementary phenomenon appears if the inverter current

is negative. The following assumptions are made for deriving the model of the cascaded H-bridge inverters:

- (a) The grid is assumed to be AC voltage source;
- (b) The losses of the CHB-DSTATCOM are categorized as effective series loss and parallel loss. The series loss and interfacing inductor loss are represented as equivalent series resistance (ESR). Parallel losses are represented as shunt connected resistances across the dc-link capacitors, corresponding to the active power loss of the H-bridge, including blocking loss, capacitor loss and absorbing circuit loss, etc. The differential equation describing the dynamics of the coupling inductor between the cascaded H-bridge inverter and the grid is derived as:

$$(2) \quad v_{sa} = Ri_c + L \frac{di_c}{dt} + f_1 v_{dc1} + f_2 v_{dc2}$$

where the variable v_{sa} represents grid voltage at the point of common coupling (PCC) [see Figure 1], L represents the inductance of the coupling inductor and R represents the equivalent series resistance. The variables v_{dc1} and v_{dc2} are the actual voltages across the dc-link capacitors of the cascaded H-bridge inverter, which may not equal to the reference voltage during dynamic process. According to the Kirchoff's law, the currents flowing into the dc-link capacitors C_1 and C_2 can be expressed as:

$$(3) \quad \begin{cases} i_{C1} = C_1 \frac{dv_{dc1}}{dt} = i_{o1} - i_{R1} = f_1 i_c - \frac{v_{dc1}}{R_1} \\ i_{C2} = C_2 \frac{dv_{dc2}}{dt} = i_{o2} - i_{R2} = f_2 i_c - \frac{v_{dc2}}{R_2} \end{cases}$$

where R_1 and R_2 are the equivalent resistance of each H-bridges, representing the parallel losses. The variables i_{o1} and i_{o2} represent the total dc-link current and i_{R1} and i_{R2} represent the currents in the dc-link resistance of the individual H-bridge module. Let the vector of state variables as $X_2 = [i_c, v_{dc1}, v_{dc2}]^T$ and $U_2 = [v_{sa}, 0, 0]^T$, as input vector, rearranging Eqs.(1)-(3), the state equations can be rewritten in the compact matrix form as:

$$(4) \quad \dot{X}_2 = \mathbf{A}_2 X_2 + \mathbf{B}_2 U_2$$

where

$$\mathbf{A}_2 = \begin{bmatrix} -\frac{R}{L} & -\frac{f_1}{L} & -\frac{f_2}{L} \\ \frac{f_1}{C_1} & -\frac{1}{R_1 C_1} & 0 \\ \frac{f_2}{C_2} & 0 & -\frac{1}{R_2 C_2} \end{bmatrix}, \quad \mathbf{B}_2 = \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

IV. Power Balancing Analysis of the CHB-DSTATCOM

Fig.3 shows the equivalent circuit of the multilevel CHB-DSTATCOM for the steady-state power balance analysis. In Fig.3, the individual H-bridge inverters are represented by AC voltage sources v_{a1} and v_{a2} , which are derived as [3]:

$$(5) \quad \begin{cases} v_{a1} = f_1 v_{dc1}, p_{R1} = v_{dc1} i_{R1} \\ v_{a2} = f_2 v_{dc2}, p_{R2} = v_{dc2} i_{R2} \end{cases}$$

where p_{R1} and p_{R2} represents the active power consumed by the effective resistance across the dc-link capacitors. For

the sake of brevity, the equivalent resistance of the coupling inductor is neglected, hence Eq.(2) can be rewritten as:

$$(6) \quad v_{sa} = L \frac{di_c}{dt} + v_{a1} + v_{a2}$$

From Fig.1 and Fig.3, the power balancing equations of the CHB-DSTATCOM can be derived as [2-4, 9, 10,16]:

$$(7) \quad v_{a1}i_c = C_1 \frac{d}{dt} \left(\frac{v_{dc1}^2}{2} \right) + p_{R1}$$

$$(8) \quad v_{a2}i_c = C_2 \frac{d}{dt} \left(\frac{v_{dc2}^2}{2} \right) + p_{R2}$$

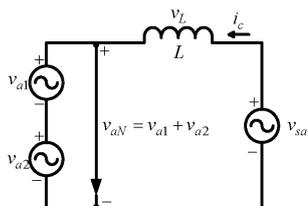


Fig.3 The equivalent circuit diagram of the CHB-DSTATCOM.

The behavior of the CHB-DSTATCOM is characterized by the inductor current dynamics and the dc-link capacitor voltage dynamics, as indicated by Eqs.(6)-(8). The power balance between the two H-bridge inverters depends on the dc-link voltages and the individual modulation signals. To better illustrate the mechanism of power exchange between the two modules, the phasor diagram of the output voltages and current of the CHB-DSTATCOM is given in Fig.4. In the analysis, it is assumed that v_{aN} is calculated in such a way that i_c is 90 degree phase-shifted with respect to v_{sa} . The angles θ_1 and θ_2 represent the phase shifts of the output voltages v_{a1} and v_{a2} with respect to v_{sa} , leading to a reactive power exchange between the individual H-bridge inverter with the grid.

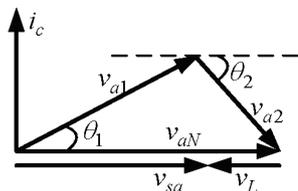


Fig.4 The phasor diagram of the voltages and current.

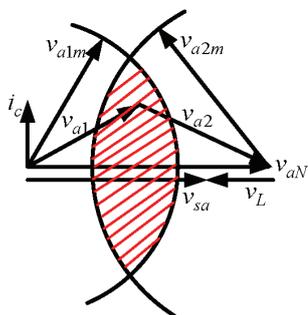


Fig.5 The stable control area of the CHB-DSTATCOM.

In the phasorial diagram (Fig.4), the maximum output voltages in root-mean square (rms) values of each H-bridge can be calculated as [3]:

$$(9) \quad v_{a1m} = \frac{4}{\pi\sqrt{2}} v_{dc1}, v_{a2m} = \frac{4}{\pi\sqrt{2}} v_{dc2}$$

The reactive power injected by each H-bridge inverter to the grid depends on the value of the capacitor voltage in the cell and the control signal modulated by each module. To ensure stable operation of the CHB-DSTATCOM, both cells must be utilized to synthesize the output voltage v_{aN} . Fig.5 shows the red marked area the possible points to achieve the desired output voltage. Any point outside of this region makes the system unstable since the output voltage of the CHB-DSTATCOM cannot be modulated with those values of the dc-link capacitor voltages. Furthermore, as shown in Fig.5, the projections of v_{a1} and v_{a2} over v_{sa} are always positive. Hence, the reactive power in both converters are positive, indicating that both inverters of CHB-DSTATCOM injects reactive power to the grid simultaneously. Moreover, it is not possible to find a point where one of the cells injects reactive power and, at the same time, the other cell absorbs reactive power from the grid. Further, it is also not possible to have only one cell injects or absorbs reactive power to the grid while the other one works in an idle mode.

Fig.6 shows that, for a given total amount of reactive power to be supplied or absorbed by the H-bridge inverter, the reactive power sharing by each cell has to be between a minimum and maximum value to achieve a stable operation of the CHB-inverter. Fig.6(a) shows the minimum reactive power that is supplied by the first inverter, which corresponds to the minimum reachable length of the projection of v_{a1} over v_{sa} , represented by $v_{a1q,min}$. As the amount of reactive power supplied by the CHB-DSTATCOM is fixed, this value is related with the maximum reactive power that is supplied to the second cell, shown in Fig.6(a) as $v_{a2q,max}$, which is the maximum reachable length of the projection of v_{a2} over v_{sa} . In the same way, the values for the maximum reactive power supplied by the first inverter $v_{a1q,max}$ and the minimum reactive power supplied by the second inverter $v_{a2q,min}$ can also be illustrated, as shown in Fig.6(b).

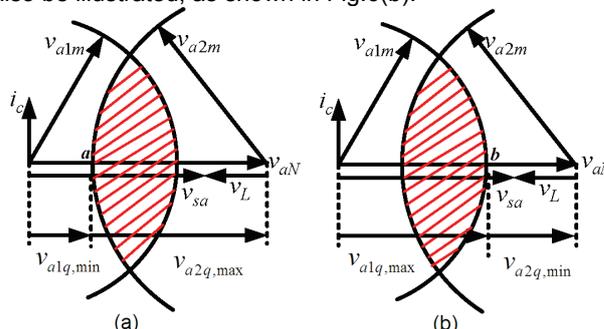


Fig.6 The diagram of maximum and minimum reactive power limits.

V. Control Strategies of the CHB-DSTATCOM

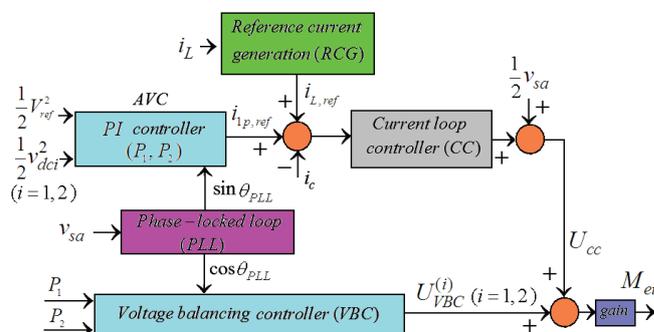


Fig.7 The block diagram of the devised control algorithms.

Based on the analysis of the power balancing mechanism, the control block diagram can be synthesized, as shown in Fig.7. The control algorithm consists of five blocks, i.e., the reference current generation (RCG) unit, the phase-locked loop (PLL), the current loop controller (CC), the average dc-

link voltage controller (AVC) and the dc voltage balancing controller (VBC). Notably, the RCG and PLL methods can be found in [11-15]. Further, the voltage balancing scheme based on the AVC and VBC control achieves equal reactive power sharing of the two cells by dynamically exchanging active power within the two inverters, and the outputs of the AVC controller (P_1 and P_2) are applied to the VBC controller to regulate the difference of dc-link voltages. Next, the design methodologies for the current loop controller and voltage balancing controller would be presented.

A. Current Loop Controller Design

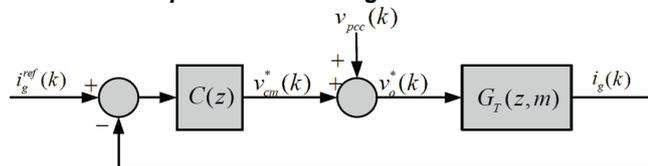


Fig.8 The closed-loop block diagram of the current tracking loop.

Fig.8 shows the discrete control diagram of the current loop controller for the CHB-DSTATCOM, where the transfer function $C(z)$ represents proportional-integral (PI) regulator:

$$(10) \quad C(z) = k_p + \frac{k_i T_s}{z-1}$$

where k_p and k_i denote the proportional and integral gains. The plant of the current controller is the coupling inductor, and $G_p(s) = 1/(L_0 s + R_0)$, where L_0 and R_0 denote the nominal

parameters. Equation (10) can be discretized using the zero-order hold (ZOH) method, as:

$$(11) \quad G_T(z, m) = Z \left\{ \frac{1-e^{-sT_s}}{s} G_p(s) e^{-smT_s} \right\} = \frac{z-1}{z} Z \left\{ \frac{G_p(s)}{s} e^{-smT_s} \right\} \\ = \frac{z-1}{z} Z_m \left\{ \frac{G_p(s)}{s} \right\} = \frac{T_s/L_0 \cdot z^{-m}}{z-(1-R_0 T_s/L_0)}$$

where 'm' denotes the equivalent sample of control delay. Neglecting the effect of the grid voltage and consider $m=1$, the open loop transfer function of the current loop controller can be derived as:

$$(12) \quad G_{open}^{cc}(z) = \frac{k_p T_s}{L_0} \cdot \frac{z-(1-(k_i T_s/k_p))}{z(z-1)[z-(1-(R_0 T_s/L_0))]}$$

Hence, the closed-loop transfer function can be easily derived from Eq.(12). The evaluation of the current loop controller under different control cycle and PI parameters are shown in Figs.9-10. It shows in Fig.9 that, the dominant pole of the closed-loop transfer function is critically damped when the control cycle $T_c=50\mu s$ and $k_p=8$, $k_i=160$. It shows in the Nichols diagram that the gain margin (GM) is 9.54dB and the phase margin (PM) is 60.9 degree. The bandwidth of the current loop controller is 2.45kHz and a settling time of 500 μs is observed in the step response and impulse response curves.

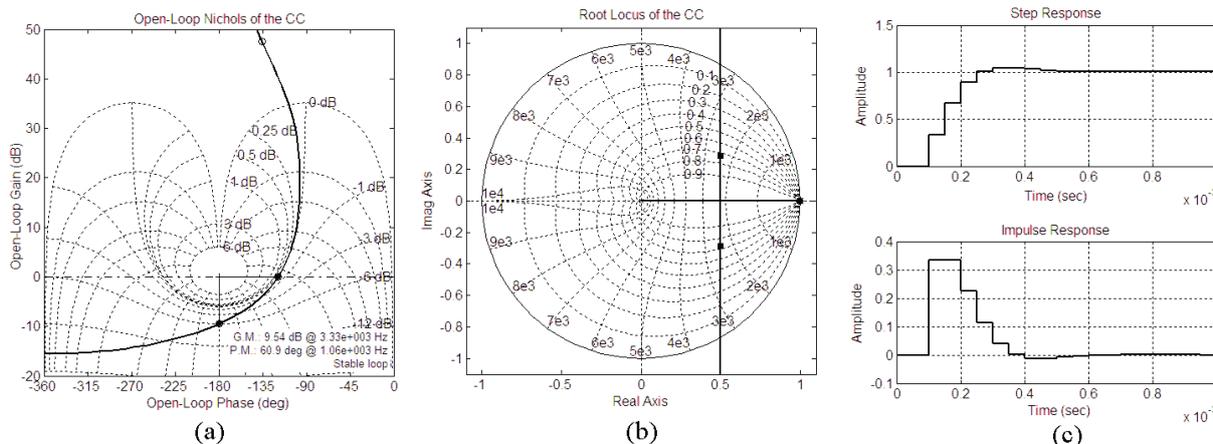


Fig.9 Evaluation of the current loop controller when the control cycle $T_c=50\mu s$ and $k_p=8$, $k_i=160$. (a) The open-loop Nichols diagram; (b) The closed-loop root locus; (c) The step response and impulse response of the current controller.

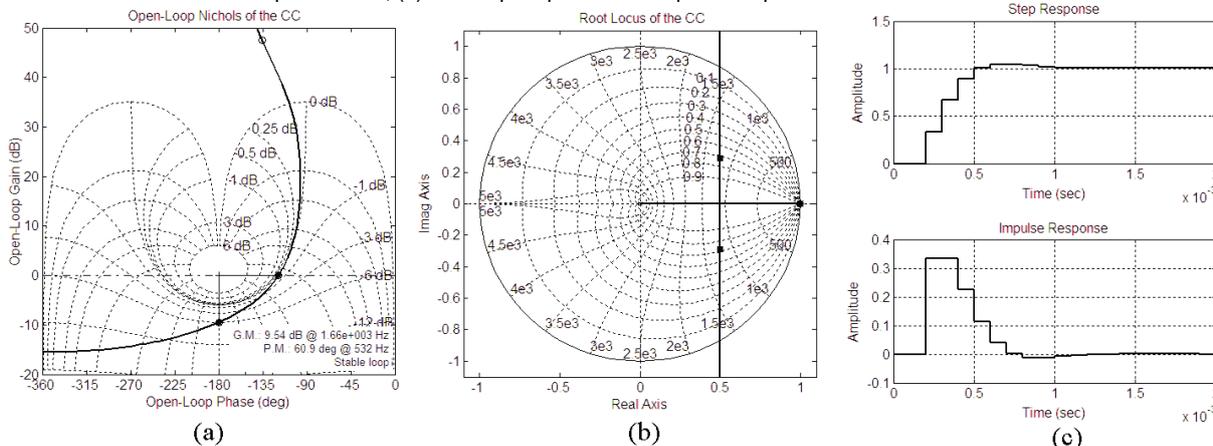


Fig.10 Evaluation of the current loop controller when the control cycle $T_c=100\mu s$ and $k_p=4$, $k_i=80$. (a) The open-loop Nichols diagram; (b) The closed-loop root locus; (c) The step response and impulse response of the current controller.

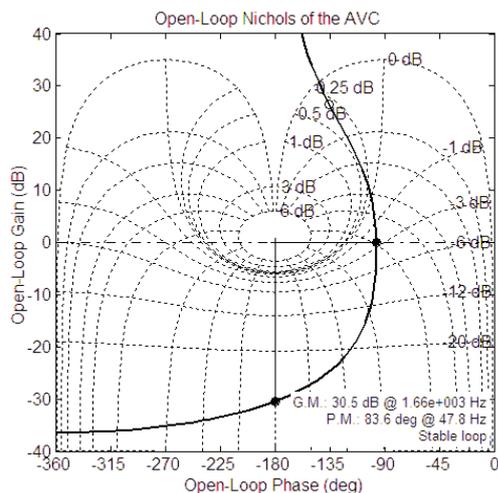


Fig.11 The open-loop Nichols diagram of the average voltage controller (AVC) when $T_c=100\mu s$.

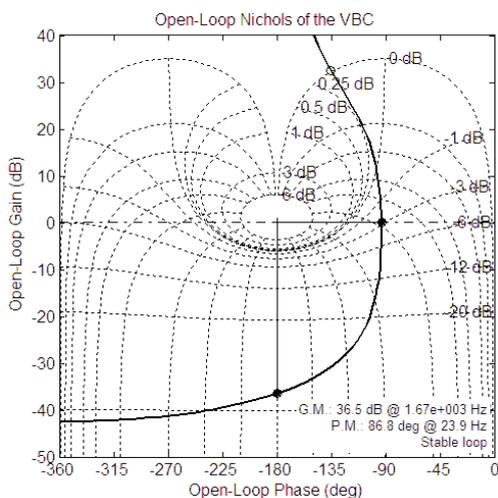


Fig.12 The open-loop Nichols diagram of the voltage balancing controller (VBC) when $T_c=100\mu s$.

Similarly, Fig.10 shows the performance of the current loop controller when the control cycle $T_c=100\mu s$ and $k_p=4$, $k_i=80$. The dominant pole of the current controller is also critically damped and $GM=9.54dB$, $PM=60.9$ degree. It is interesting to observe that the crossover frequency of the phase frequency diagram when the control cycle $T_c=100\mu s$ is half the value compared to the case when $T_c=50\mu s$. In addition, the bandwidth of the current controller is 1.22kHz, which is also half the value compared to the previous case. Besides, the settling time of the step response and impulse is 1ms, indicating that the dynamics of the current loop controller is proportional to the equivalent discretization frequency of the plant model. The comparative results reveal that, to ensure sufficient dynamics and bandwidth of the CHB-DSTATCOM, the control cycle should be as small as possible, especially when active filtering is also required. However, due to the computational limitation of the digital signal processors (DSPs), the execution speed is quite limited. Hence, a tradeoff must be achieved, the control cycle $T_c=100\mu s$ is adopted herein.

B. Dc-link Controller Synthesis for the Multilevel CHB-DSTATCOM based on Power Balancing Methodology

The voltage regulation loop includes the average voltage controller (AVC), which is designed to regulate the total active power balance between the CHB-DSTATCOM with the grid, and the voltage balancing controller (VBC), which is designed to regulate active power exchange between

the two H-bridge inverters and achieve the equal reactive power sharing for the two cells.

Fig.11 shows the open-loop Nichols diagram and closed-loop root locus diagram of the AVC, where the proportional-integral parameters are designed as $k_{p,AVC}=0.6$, $k_{i,AVC}=12$. It shows that a gain margin (GM) of 30.5dB and a phase margin (PM) of 83.6 degree is achieved. Hence the AVC loop is stable. Fig.12 shows the open-loop Nichols diagram and closed-loop root locus diagram of the VBC, where the proportional-integral parameters are designed as $k_{p,VBC}=0.1$, $k_{i,VBC}=1.2$. It shows that a gain margin (GM) of 36.5dB and a phase margin (PM) of 86.8 degree is achieved, thus the stability of the VBC loop is guaranteed.

VI. Simulation Results and Discussions

In order to verify the effectiveness of the devised control scheme, digital simulation using the Alternative Transient Program (ATP/EMTP) was performed and the results are evaluated. The parameters of the system are: $L_g=50\mu H$, $R_g=20m\Omega$, $L=1.5mH$, $R=50m\Omega$, and the nonideal dc-link parameters are: $C_1=C_2=2000\mu F$, $R_1=R_2=39000\Omega$, sampling time $T_s=100\mu s$, the grid voltage $v_{sa}=220V(rms)$, the target inverter dc-link voltage is 200V.

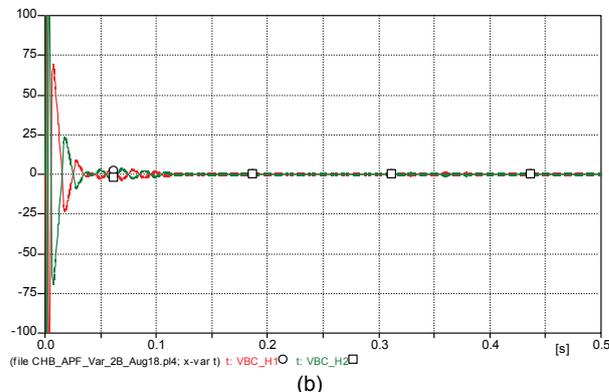
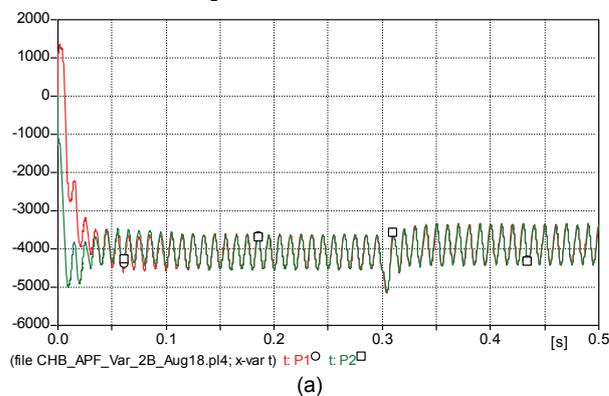
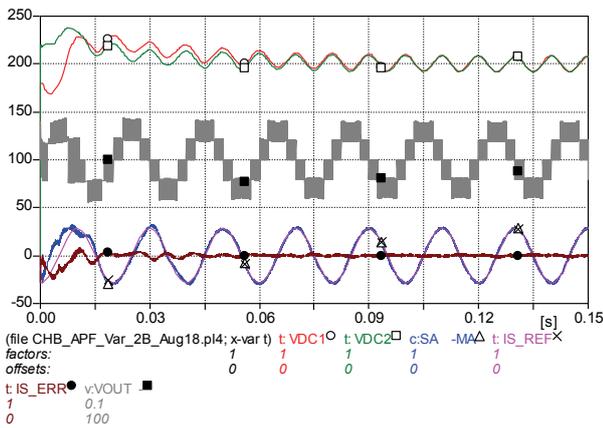
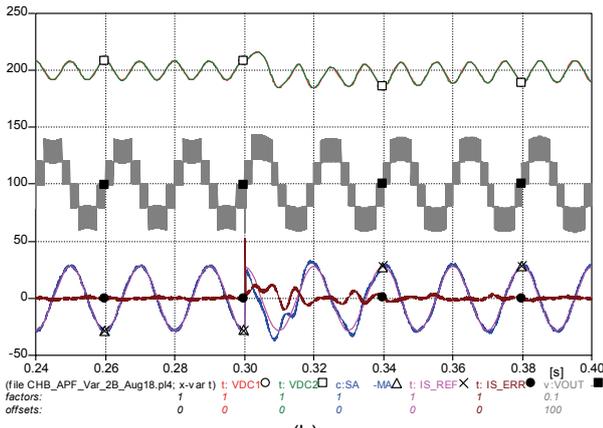


Fig.13 (a) The output of the voltage regulator P1 and P2; (b) The output of the voltage balancing controller (VBC).

It can be observed that, the CHB-DSTATCOM works in the inductive mode when $t<0.3s$, hence a constant reactive power is absorbed by the DSTATCOM. At $t=0.3s$, the reference signal for the CHB-DSTATCOM changes from inductive to capacitive to test the dynamic response of the system, hence the grid side current leads the grid voltage by 90 degree when $t>0.3s$. Fig.13 shows the output signals of the AVC and the VBC controllers. It can be observed in Fig.13(a) that the variables P1 and P2 reach a constant values in the steady state. And Fig.13(b) shows that the output of VBC controller approaches to zero. In addition, excellent dynamic response is achieved when the reference signal is undergone transient perturbations.



(a)

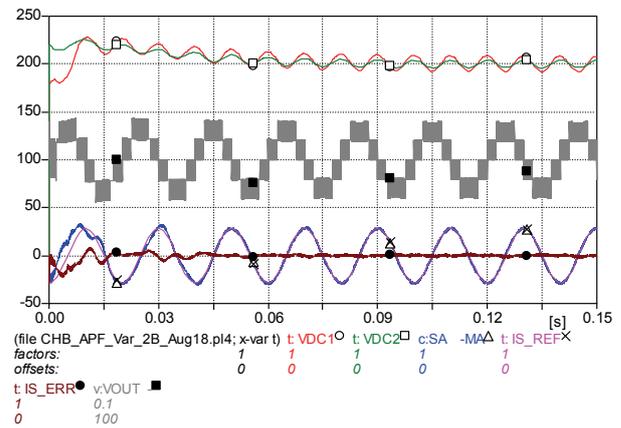


(b)

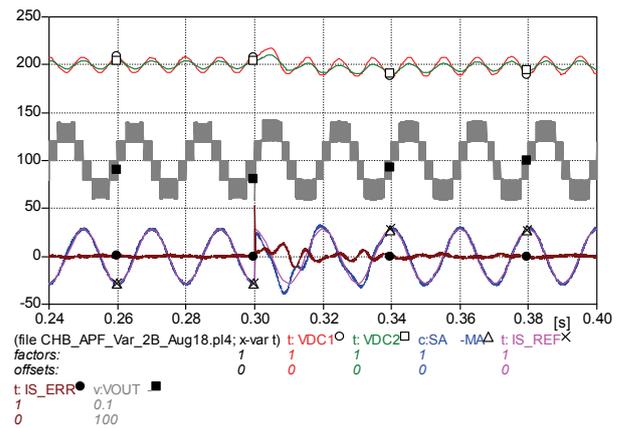
Fig.14 The simulation results of the CHB-DSTATCOM under nominal power-stage parameters. (a) The convergence process after system start-up; (b) Transient response from inductive mode to capacitive mode.

Fig.14 shows the time domain simulation results under nominal parameters, where the dc-link voltages, and the synthesized multilevel voltage, grid side current and its reference as well as the tracking error are illustrated. The convergence process after the system start-up is shown in Fig.14(a), where the initial dc-link voltages are set to 180V and 220V, respectively. It can be observed that the dc-link voltages converge to the same value after a few cycles. And the grid-side current tracks its reference value with fast dynamics and the tracking error approaches zero in the steady state. Fig.14(b) shows the dynamic response of the DSTATCOM when the reference current is undergone a transient change from inductive mode to capacitive mode. It can be observed that the stability of the dc-link voltages is preserved under the transient perturbations. And the grid current tracks its reference within two fundamental cycles, which demonstrates the validity of the control scheme.

To test the robustness of the devised control scheme, the simulation results under non-nominal parameters are also considered, as shown in Figs.15-17. Fig.15 shows the scenario when the capacitor value of the second inverter $C_{dc2}=4000\mu\text{F}$ and the other parameters remain unchanged. It can be observed that the stability of the DSTATCOM is ensured and all the waveforms resemble those in Fig.14. Notably, the only difference is that, the dc-link voltage ripple of the second inverter is much less than the first one. Besides, the tracking error of the grid side current is almost zero in the steady state and has a settling time of two cycles under transient perturbation of the reference current.



(a)



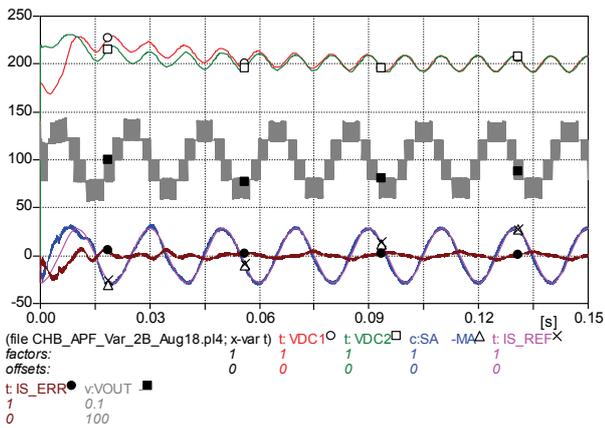
(b)

Fig.15 The simulation results of the CHB-DSTATCOM when $C_{dc2}=4000\mu\text{F}$. (a) The convergence process after system start-up; (b) Transient response from inductive mode to capacitive mode.

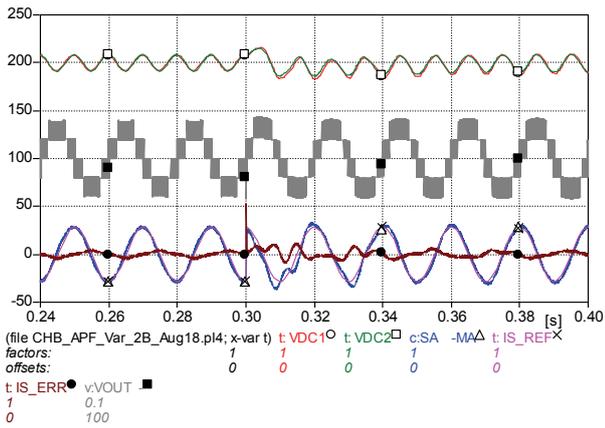
Fig.16 shows the scenario when the resistor value of the second inverter $R_{dc2}=100\Omega$ while other parameters remain unchanged. It can be observed that the stability of the DSTATCOM is ensured and all the waveforms resemble those in Fig.14. However, the tracking error of the grid side current is a little higher in the steady state compared to the case in Fig.14. Besides, a settling time of two cycles under transient perturbation of the reference current can also be observed.

Fig.17 shows the scenario when the resistor and capacitor value of the second inverter are changed as $C_{dc2}=4000\mu\text{F}$, $R_{dc2}=100\Omega$ while other parameters remain unchanged. It shows that the stability of the DSTATCOM is ensured and all the waveforms resemble those in Fig.14. However, the dc-link voltage ripple of the second inverter is much less than the first one. And the tracking error of the grid side current is higher in the steady state compared to the case in Fig.14. Besides, a settling time of two cycles under transient perturbation of the reference current can also be observed.

Figs.15-17 imply that the devised control scheme is quite robustness under power stage parameter variations since the dc-link voltage stability is ensured and the sinusoidal waveform is obtained in the grid side current, with a total harmonic distortion of less than 5% for all these scenarios. It can be inferred that the devised control scheme would produce robust control effect for the CHB-DSTATCOM. Normally, the power-stage parameters deviation is quite small hence a sufficient stability margin can be achieved.

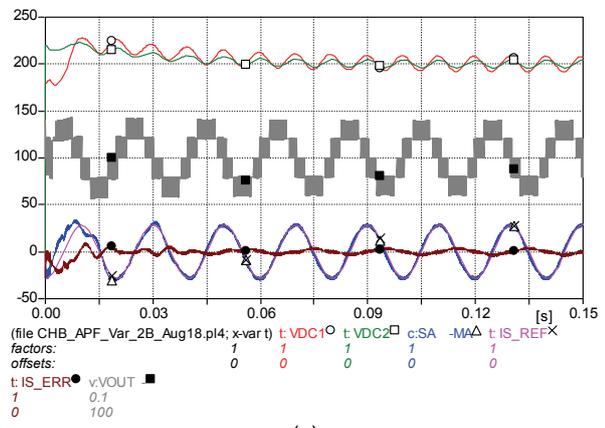


(a)

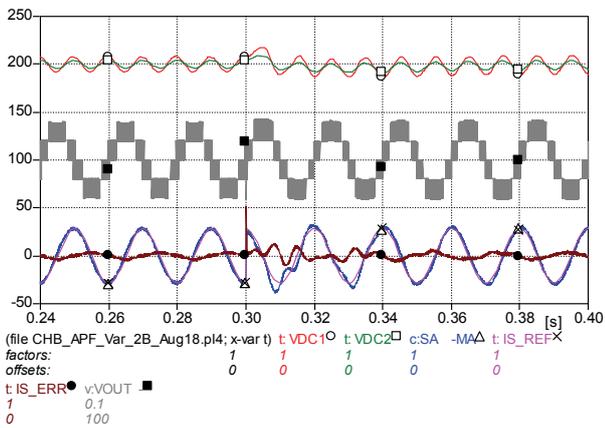


(b)

Fig.16 The simulation results of the CHB-DSTATCOM when $R_{dc2}=100\Omega$. (a) The convergence process after system start-up; (b) Transient response from inductive mode to capacitive mode.



(a)



(b)

Fig.17 The simulation results of the CHB-DSTATCOM when $R_{dc2}=100\Omega$ and $C_{dc2}=4000\mu F$. (a) The convergence process after system start-up; (b) Transient response from inductive mode to capacitive mode.

VII. Experimental Results of the Prototype System

To reconfirm the validity of the devised control scheme, a hardware prototype system is built, the floating-point digital signal processor (DSP) from Texas Instrument (TI) (TMS320C6726) is adopted to implement the algorithm. The cyclone FPGA is used for the A/D sampling, protection, soft-start, and pulse width modulation (PWM) generation for the CHB-DSTATCOM. The circuit parameters of the experimental set-up is the consistent with the simulation: $L_g=50\mu H$, $R_g=20m\Omega$, $L=1.5mH$, $R=50m\Omega$, and the nominal dc-link parameters are: $C_1=C_2=2000\mu F$, $R_1=R_2=39000\Omega$, sampling time $T_s=100\mu s$.

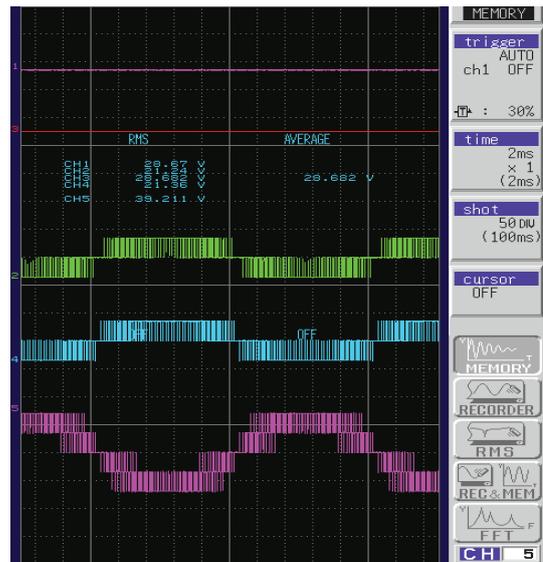


Fig.18 The synthesized five-level voltage of the CHB-DSTATCOM.

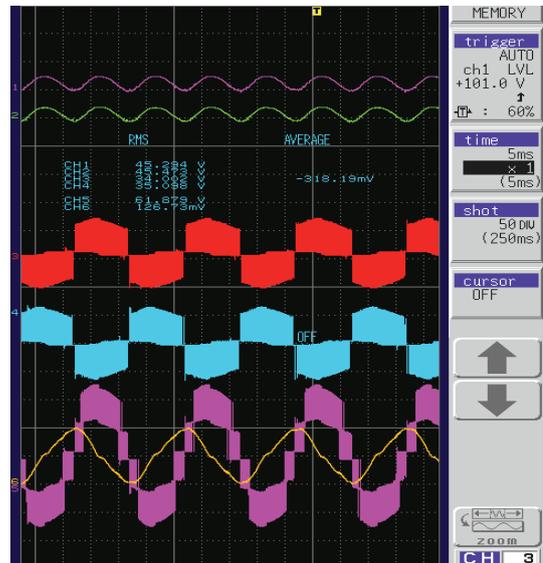


Fig.19 The capacitive mode of the multilevel CHB-DSTATCOM.

Fig.18 shows the experimental results of the synthesized multilevel output voltage ' v_{aN} ', and the dc-link voltages of the CHB-inverter at no load conditions. It can be observed that the dc-link voltages (ch-1, ch-3) are about 28.6V, and the output voltages of each inverter (ch-2, ch-4) are about 21V, which are phase-shifted by 90 degree in the PWM

carriers. And the five-level output voltage (ch-5) can also be observed in Fig.18.

Fig.19 shows the capacitive mode of the DSTATCOM. The rms value of the dc-link voltages (ch-1, ch-2) are about 45V and the waveforms show perfect matching with each other. The rms values of the output voltages v_{a1} and v_{a2} (ch-3, ch-4) are about 35V. Besides, the grid current (ch-6) is leading the multilevel voltage v_{aN} 90 degree, indicating that the CHB-DSTATCOM is injecting capacitive reactive power to the grid. Fig.20 shows the inductive mode of the DSTATCOM. The rms value of the dc-link voltages (ch-1, ch-2) are about 45V and the waveforms show perfect matching with each other. The rms values of the output voltages v_{a1} and v_{a2} (ch-3, ch-4) are about 32V. Besides, the grid current (ch-6) is lagging the multilevel voltage v_{aN} 90 degree, indicating that the DSTATCOM is absorbing capacitive reactive power from the grid. It is interesting to notice that the waveforms recorded from the experimental prototype system match the simulation waveforms quite well, under both the capacitive and inductive mode, which demonstrates the validity of the devised control algorithm.

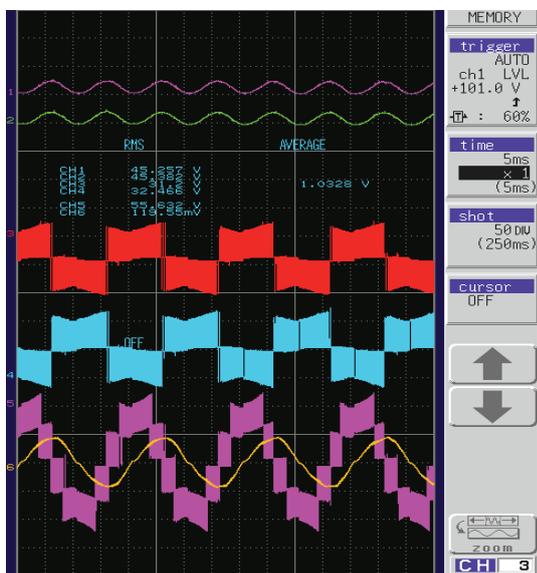


Fig.20 The inductive mode of the multilevel CHB-DSTATCOM.

VIII. Conclusions and Future Work

This paper presents an effective control scheme for the cascaded H-bridge (CHB) DSTATCOM. The principle of multilevel carrier-shifted pulsewidth modulation (CSPWM) and the mechanism of power balancing among individual H-bridges inverters are presented. The controller synthesis of the CHB-DSTATCOM is provided, which consists of current tracking controller design, the average dc-link voltage controller (AVC) and voltage balancing controller (VBC), which are devised from the devised power balance mechanism.

The simulation results obtained from the Alternative Transient Program (ATP) are presented for verification, where the effect of power-stage parameter variations is also taken into consideration. The robustness of the devised control scheme is verified by the simulation results. Finally, the experimental results of the prototype system are presented, which confirms the effectiveness of the control scheme.

The presented dc-link voltage balancing scheme can be extended to other grid-connected CHB-inverters, such as multilevel active rectifiers, active filters, etc. The results of these applications would be reported in the near future.

REFERENCES

- [1] Han Y., Xu L., Yao G., Zhou L., Khan MM, Chen C., Flicker mitigation of arc furnace load using modified p-q-r method, *Przeglad Elektrot.*, 85(2009), n.1, 225-229.
- [2] Han Y., Xu L., Yao G., Zhou LD., Khan MM., Chen C., A novel modulation scheme for dc-voltage balancing control of cascaded H-bridge multilevel APF, *Przeglad Elektrot.*, 85(2009), n. 5, 81-85.
- [3] Sergio V., Jose IL., Juan M.C., Leopoldo GF., etc., Analysis of the power balance in the cells of a multilevel cascaded H-bridge converter, *IEEE Trans. Ind. Electron.*, 57(2010), n.7, 2287-2296.
- [4] Stala R., Pirog S., Baszynski M., Mondzik A., Penczek A., Czekonski J., Gasiorek S., Results of investigation of multicell converters with balancing circuit-Part I, *IEEE Trans. Ind. Electron.*, 56(2009), n.7, 2610-2619.
- [5] Han Y., Xu L., Yun WJ., Yao G., Zhou LD., Khan MM., Chen C., Power quality enhancement for automobile factory electrical distribution system-strategies and field practice, *Przeglad Elektrot.*, 85(2009), n. 6, 159-163
- [6] Han Y., Xu L., Yao G., Zhou LD., Khan MM., Chen C., Power system harmonic estimation scheme based on Affine projection adaptive filter theory, *Przeglad Elektrot.*, 85(2009), n. 11, 45-50.
- [7] Han Y., Xu L., Yao G., Zhou L., Khan MM, Chen C., A Robust Deadbeat Control Scheme for Active Power Filter with LCL Input Filter, *Przeglad Elektrot.*, 86(2010), n.2, 14-19.
- [8] Han Y., Xu L., Khan MM, Chen C., Yao G., Zhou L., Modelling and controller synthesis of a hybrid-LCL APF for power quality conditioning applications, *Przeglad Elektrot.*, 86(2010), n.9, 326-333.
- [9] Grandi G., Rossi C., Ostojic D., Casadei D., A new multilevel conversion structure for grid-connected PV applications, *IEEE Trans. Ind. Electron.*, 56(2009), n.11, 4416-4426.
- [10] Barrena J., Marroyo L., Vidal M., Apraiz J., Individual voltage balancing strategy for PWM cascaded H-bridge converter-based STATCOM, *IEEE Trans. Ind. Electron.*, 55(2008), n.1, 21-29.
- [11] Han Y., Khan MM, Yao G., Zhou L., Chen C., A novel harmonic-free power factor corrector based on T-type APF with adaptive linear neural network (ADALINE) control, *Simul. Model. Pract. Theory*, 16(2008), n.9, 1215-1238.
- [12] Cirrincione M., Pucci M., Vitale G., Miraoui A., Current harmonic compensation by a single-phase shunt active power filter controlled by adaptive neural filtering, *IEEE Trans. Ind. Electron.*, 56(2009), n.8, 3128-3143.
- [13] Filho RMS, Seixas PF, Cortizo PC, Torres LAB, Souza AF. Comparison of three single-phase PLL algorithms for UPS applications, *IEEE Trans. Ind. Electron.*, 55(2008), n.8, 2923-2932.
- [14] Han Y., Xu L., Khan MM, Yao G., Zhou L., Chen C., A novel synchronization scheme for grid-connected converters by using adaptive linear optimal filter based PLL (ALOF-PLL), *Simul. Model. Pract. Theory*, 17(2009), n.8, 1299-1345.
- [15] Han Y., Khan MM, Xu L., Zhou L., Yao G., Chen C., A novel control strategy for active power filter using synchronous reference frame (SRF) ADALINEs, *International Review of Electrical Engineering-IREE*, 3(2008), n.4, 629-645.
- [16] Han Y., Xu L., Yao G., Zhou L., Khan MM, Chen C., State-Space Averaging (SSA) Technique for Modeling of the Cascaded H-Bridge Multilevel DSTATCOMs and Active Filters, *International Review of Electrical Engineering-IREE*, 4(2010), n.5, 744-760.

Authors: Dr. Yang Han is with the Department of Power Electronics, School of Mechatronics Engineering, University of Electric Science and Technology of China (UESTC), No.2006 XiYuan Road, West Park of Chengdu Hi-Tech Zone, 611731, Chengdu, P.R.China, E-mail: hanyang_facts@hotmail.com; All the co-authors are with the department of electrical engineering, Shanghai JiaoTong University, #800 DongChuan Road, 200240, Shanghai, P.R.China.