Guanghui TAN[1], Yi TANG[1], Bingtuan GAO[1], Xinghe FU[1], Yanchao JI[2]

Southeast University (1), Harbin Institute of Technology (2)

Soft-switching AC module inverter with flyback transformer for photovoltaic power system

Abstract. *This paper presents an AC module inverter for photovoltaic (PV) power system. The PV inverter employs a Buck-Boost converter on the DC side and a flyback inverter on the AC side. Based on capacitive idling (CI) techniques and peak current control method, the proposed inverter shows low current distortion, high power factor, small power decoupling capacitor and soft-switching operation. Analysis and experimental results are provided to demonstrate these excellent features.*

Streszczenie. *W artykule zaprezentowano modułowy przekształtnik AC zastosowany w systemach fotowoltaicznych. Przekształtnik wykorzystuje konwerter Buck-Boost po stronie DC i konwerter typu flyback po stronie AC. Układ bazuje na jałowym biegu pojemnościowym i kontroli wartości szczytowej prądu. (**Modułowy przekształtnik AC z transformatorem typy flyback w systemie fotowoltaicznym**)*

Keywords: flyback inverter, soft-switching, capacitive idling (CI), photovoltaic (PV).
Słowa kluczowe: przekształtnik flyback, systemy fotowoltaiczne.

Introduction

In recent years, the number of grid-connected systems using photovoltaic (PV) has increased considerably [1-3]. The improvements of reliability, power conversion efficiency, lifetime and production cost of small power PV inverters have grown further concern. The new technology on this subject is the so-called "AC Module" [4,5] ranging from 50W to 1kW. An AC Module is the integration of the inverter and PV module into one electrical device. It includes the possibility of an easy enlarging of the system due to the modular structure, and the opportunity to become a "plug-and-play" device.

A flyback inverter suitable for AC Module has been proposed [6]. The circuit is made up around a single-transistor flyback converter, with a high-frequency center-tapped transformer. To optimize the PV system performance, a sensorless current MPPT method for the flyback inverter was presented [7]. Although the flyback inverter is small and cost-effective, high-frequency switching mode transitions trend to decrease the actual efficiencies of the power conversion process. Efforts to reduce the high-frequency switching power losses in the high-frequency flyback inverter have been reported [8-10].

In the case of single-phase grid-connected inverters, an electrolytic capacitor with large capacitance has been connected to the DC input side in order to decouple the power pulsation cause by single-phase power generation to the AC grid. The large electrolytic capacitor has a large volume and a relatively short lifespan [2], which may harm the AC Module concept. In [11-13], the need for a large decoupling capacitor is avoided by adding a Buck-Boost converter to the flyback inverter, but high-frequency hard-switching to turn off reduces the actual efficiency of the power conversion process.

In this paper, a single-phase flyback inverter with four active switches for PV power system is proposed. Based on capacitive idling (CI) technique [14,15], Buck-Boost converter topology is introduced into the proposed inverter to realize soft-switching and independent control of input and output currents without the need for additional circuitry. In addition, the power pulsation on DC bus is converted into the voltage pulsation on a power decoupling capacitor, such that the low-frequency ripple current on the DC bus can be reduced. To verify the validity and effectiveness of the proposed inverter, the experimental results based on a 100W laboratory prototype are provided.

Circuit configuration and operation principle

The CI DC-DC converter derived from the Buck-Boost and Sepic topology is shown in Fig. 1, which allows soft commutation of power switches without the need for additional circuitry, and makes it possible to increase the switching frequency while maintaining high efficiency [16]. With the addition of idling operating state, independent control of input and output currents can be obtained to improve its bandwidth.

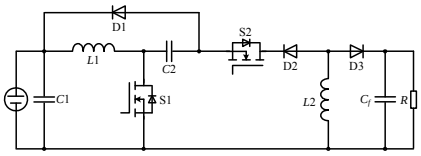

Fig.1. Capacitive idling (CI) DC-DC converter

Fig. 2 shows the proposed soft-switching flyback inverter, which is derived from the CI DC-DC converter and single-phase flyback inverter. This new topology still reserves the excellent properties from the CI technique, such as no-pulsating voltage and current waveforms at the input and the output, low component count and the ability to encompass soft-switching techniques. Unlike the CI DC-DC converter which only operates under DC condition, the topology proposed here can operate as an inverter producing the AC power.

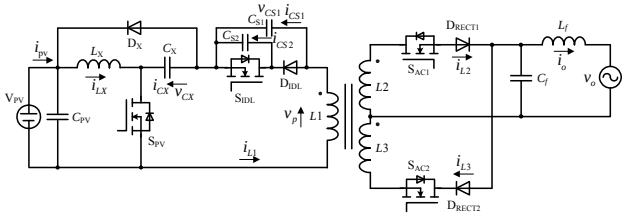

Fig.2. The proposed soft-switching AC module inverter

There are two high-frequency switches S_{PV} and S_{IDL}, two line-frequency switches S_{AC1} and S_{AC2}, two inductors L_X and L_f, four diodes D_X, D_{IDL}, D_{RECT1} and D_{RECT2}, three capacitors C_{PV}, C_X and C_f, two snubber capacitors C_{S1} and C_{S2}, and a high-frequency flyback transformer with center-tapped secondary winding ($L1$, $L2$ and $L3$) in the proposed inverter. Because the power pulsation with twice the line-frequency is converted on the power decoupling capacitor C_X, the low-frequency ripple current on the DC bus is reduced remarkably, so that the need for a large decoupling

capacitor is avoided. The CI switch S_{IDL} is controlled and the peak value of the inductor current i_{L1} is prescribed to track the desired current command. Therefore, pure sinusoidal output current with unity power factor is drawn into the AC grid.

Due to the snubber capacitors CS1 and CS2 parallel with switch SIDL and diode DIDL, the proposed flyback inverter still reserves soft-switching property based on the CI technique. For convenience in analysis, only the positive half cycle of the output voltage is considered. The secondary-side switches SAC1 is on and SAC2 is off. The theoretical waveforms of the adopted inverter are shown in Fig. 3, where there are seven operating stages during one switching cycle. To simplify the analysis, following assumptions are used: the circuit is operating in steady state; the switches, diodes and all the components are ideal.

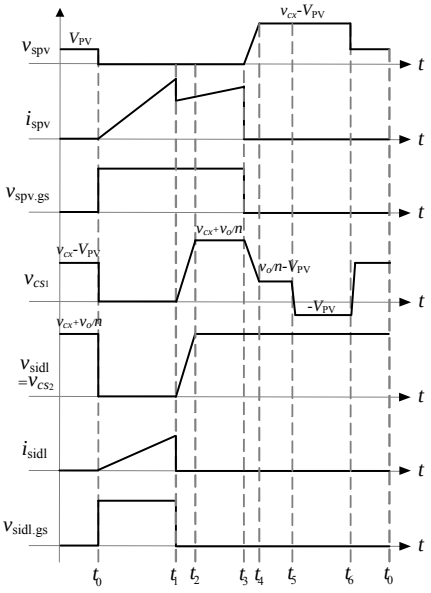

Fig.3. Main waveforms of the proposed flyback inverter

Stage 1 ($t_0<t<t_1$): In this stage switches S_{PV} and S_{IDL} are turned on. The input voltage V_{PV} is short-circuited by the input inductor L_X and the transformer primary voltage $v_p = v_{CX}$. The voltages $v_{spv}=v_{sidl}=0$. The input inductor current i_{LX} increases linearly and is expressed as:

$$i_{LX}(t) = i_{LX}(t_0) + \frac{V_{PV}}{L_X}(t - t_0) \tag{1}$$

The primary current i_{L1} also increases linearly and is given as:

$$i_{L1}(t) = i_{L1}(t_0) + \frac{V_{CX}}{L_1}(t - t_0) \tag{2}$$

Because of discontinuous conduction mode (DCM) operation, the initial currents $i_{LX}(t_0)=i_{L1}(t_0)=0$, so soft-switching operation with ZCS for the high-frequency switches S_{PV} and S_{IDL} is realized. The secondary voltage $v_m=-nv_{CX}$ so that diode D_{AC1} is turned off. Switch currents $i_{spv}=i_{LX}+i_{L1}$, $i_{sidl}=i_{L2}$, and $i_{S3}=0$. In this stage the input energy is stored in input inductor L_X and primary-side inductor $L1$. The output current is supplied by the output filter capacitor. This stage ends when switch S_{IDL} is turned off at time $t=t_1$.

Stage 2 ($t_1<t<t_2$): This stage starts when switch S_{IDL} is turned off. In this stage switch S_{PV} is still turned on and the input inductor current i_{LX} increases linearly under the input voltage V_{PV}. The primary current flows through the snubber capacitors C_{S1} and C_{S2}, performing a zero-voltage commutation. The snubber capacitor voltages v_{CS1} and v_{CS2} are charged from 0V to $v_{CX}+v_o/n$. In this stage the primary voltage $-v_{CX}<v_p<v_o/n$ and the secondary voltage $-nv_{CX}<v_p<v_o$. Diode D_{AC1} is also turned off and switch current $i_{L2}=0$. The snubber capacitor voltages v_{CS1} and v_{CS2} and primary current i_{L1} can be expressed as:

$$v_{CS1}(t) = v_{CS2}(t) = v_{CX}(1 - \cos(\omega_1(t - t_1))) + i_{L1}(t_1)Z_1 \sin(\omega_1(t - t_1)) \tag{3}$$

$$i_{L1}(t) = i_{L1}(t_1)\cos(\omega_1(t - t_1)) + \frac{v_{CX}}{Z_1}\sin(\omega_1(t - t_1)) \tag{4}$$

where the resonant angular frequency ω_1 and characteristic impedance Z_1 are given by

$$\omega_1 = \frac{1}{\sqrt{L_1 \cdot C_{S1}//C_{S2}}},\ Z_1 = \sqrt{\frac{L_1}{C_{S1}//C_{S2}}} \tag{5}$$

Since the snubber capacitances C_{S1} and C_{S2} are very small, the capacitor voltages v_{CS1} and v_{CS2} are charged quickly and this time interval is very short. The snubber capacitor voltage and primary current in (3) and (4) can be approximately given as:

$$v_{CS1}(t) = v_{CS2}(t) \simeq i_{L1}(t_1)Z_1\omega_1(t - t_1) = \frac{i_{L1}(t_1)}{C_{S1}//C_{S2}}(t - t_1) \tag{6}$$

$$i_{L1}(t) \simeq i_{L1}(t_1) + \frac{v_{CX}}{Z_1}\omega_1(t - t_1) = i_{L1}(t_1) + \frac{v_{CX}}{L_1}(t - t_1) \simeq i_{L1}(t_1) \tag{7}$$

This stage ends when the snubber capacitor voltages v_{CS1} and v_{CS2} equals to $v_{CX}+v_o/n$ at time $t=t_2$, and the secondary-side diode D_{AC1} is turned on. The time interval for stage 2 can be expressed as:

$$\Delta t_{12} = t_2 - t_1 \simeq \frac{(v_{CX} + v_o/n)}{i_{L1}(t_1)} \tag{8}$$

Stage 3 ($t_2<t<t_3$): At time $t=t_2$, the primary voltage v_p equals v_o/n and the secondary-side diode D_{AC1} is turned on, so the energy is transferred into the secondary winding to generate output current. The input inductor current i_{LX} increases linearly and can be given as:

$$i_{LX}(t) = i_{LX}(t_2) + \frac{V_{PV}}{L_X}(t - t_2) \tag{9}$$

The switch currents $i_{spv}=i_{LX}$, $i_{sidl}=0$, and $i_{sac1}=i_{L2}$. In this stage the input energy is stored in the input inductor L_X. The stage ends when switch S_{PV} is turned off at the time $t=t_3$.

Stage 4 ($t_3<t<t_4$): At the beginning of this interval, switch S_{PV} is turned off, and the input inductor current i_{LX} flows into capacitor C_{S1}. The snubber capacitor voltages v_{CS1} and v_{CS2} and input inductor current i_{LX} are expressed as:

$$v_{CS1}(t) = V_{PV} + (v_{CS1}(t_3) - V_{PV} + v_{CX})\cos(\omega_2(t - t_3))) + i_{LX}(t_3)Z_2 \sin(\omega_2(t - t_3)) \tag{10}$$

$$v_{CS2}(t) = v_{CX} + v_o/n \tag{11}$$

$$i_{LX}(t) = i_{LX}(t_3)\cos(\omega_2(t - t_3)) + \frac{(V_{PV} - v_{CX} - v_{CS1}(t_3))}{Z_2}\sin(\omega_2(t - t_3)) \tag{12}$$

where the resonant angular frequency ω_2 and characteristic impedance Z_2 are given by

$$\omega_2 = \frac{1}{\sqrt{C_{S1}(L_X + L_1)}},\ Z_2 = \sqrt{\frac{L_X + L_1}{C_{S1}}} \tag{13}$$

The interval ends when the snubber capacitor voltage v_{CS1} equals to v_o/n-V_{PV} to turn on diode D_{RECT1}. In this stage voltage v_{spv} increases from 0V to v_{CX}-V_{PV} to perform zero-voltage turn-off operation.

Stage 5 ($t_4<t<t_5$): At time $t=t_4$ diode D_X conducts the input inductor current i_{LX}, through L_X and C_X. In this stage current i_{LX} charges the capacitor voltage v_{CX} and the output current is supplied by the energy stored in the secondary winding. This stage ends when the secondary current i_{L2} is zero and diode D_{AC1} is turned off.

Stage 6 ($t_5<t<t_6$): In this stage the secondary current i_{L2} is zero, and switch S_{AC1} and diode D_{AC1} are always off. The output current is supplied by the filter capacitor C_f. Current i_{LX} charges the capacitor voltage v_{CX} until i_{LX}=0 at time $t=t_6$ because of DCM operation.

Stage 7 ($t_6<t<t_0$): During this interval, all of the switches and diodes are off and currents $i_{LX}=i_{L1}=i_{L2}=i_{L3}=0$. The output current is also supplied by filter capacitor C_f. When switches S_{PV} and S_{IDL} are turned on, the switching cycle is completed.

Improved power decoupling

Power decoupling is normally achieved by means of an electrolytic capacitor and the lifetime of the PV inverter is mostly determined by this component. However, it is difficult to design a single-phase inverter without at least one capacitor for power decoupling between the PV module and the AC grid. Thus, they should be kept as small as possible and preferably substituted with film capacitor.

For single-phase grid-connected PV inverter with unity power factor, the AC grid voltage and current can be expressed as:

$$v_o = V_o \sin \omega_o t \tag{14}$$

$$i_o = I_o \sin \omega_o t \tag{15}$$

where V_o is the peak grid voltage, I_o is the peak output current, and ω_o is the line angular frequency. Thus, there is a large amount of power pulsation P_o with twice the line-frequency, which is given as:

$$P_o = \frac{1}{2} V_o I_o (1 - \cos 2\omega_o t) \tag{16}$$

In the proposed single-phase flyback inverter, the low-frequency power pulsation is converted into the voltage pulsation on capacitor C_X, such that the voltage of the DC input capacitor C_{PV} is kept constant and its capacitance can be reduced to a very small value. From the law of energy conservation and assuming that the converter has 100% efficiency, the energy stored in capacitor C_X can be expressed as a function of capacitor voltage v_{CX} at any given time and it will have a sinusoidal shape superimposed on a DC offset. According to energy balance principle, the total energy stored in capacitor C_X can be calculated as:

$$\frac{1}{2} C_X v_{CX}^2 = \frac{1}{2} C_X V_{\mathrm{dc}}^2 + \int_0^t (P_i - P_o) dt \tag{17}$$

where v_{CX} is the capacitor voltage on C_X, V_{dc} is the DC component of the capacitor voltage, P_i is the input power (assumed constant), P_o is the output power. Evaluating the integral component, expression (17) can be rewritten as:

$$\frac{1}{2} C_X v_{CX}^2 = \frac{1}{2} C_X V_{\mathrm{dc}}^2 + P_i t - \frac{1}{2} V_o I_o t + \frac{1}{4\omega_o} V_o I_o \sin 2\omega_o t \tag{18}$$

where $P_i t$ represents the input energy, $\frac{1}{2} V_o I_o t$ describes the average output energy and the final sinusoidal term describes the periodic energy variation. In steady operating condition, the energy stored in the CI capacitor C_X at the end of one line cycle is equal to the initial value stored in the capacitor at the beginning of the line cycle, so we have:

$$P_i t = \frac{1}{2} V_o I_o t \tag{19}$$

And thus expression (18) can be simplified as:

$$\frac{1}{2} C_X v_{CX}^2 = \frac{1}{2} C_X V_{\mathrm{dc}}^2 + \frac{1}{2\omega_o} P_i \sin 2\omega_o t \tag{20}$$

The value of the capacitor voltage can be calculated from equation (20) at maximum point as:

$$v_{CX\max} = V_{\mathrm{dc}} + V_{CX\mathrm{ripple}} = \sqrt{V_{\mathrm{dc}}^2 + \frac{1}{\omega_o C_X} P_i} \tag{21}$$

where $V_{CX\mathrm{ripple}}$ is the amplitude of the voltage ripple. Thus the capacitance of C_X can be given as:

$$C_X = \frac{P_i}{\omega_o (V_{CX\mathrm{ripple}}^2 + 2 V_{dc} V_{CX\mathrm{ripple}})} \tag{22}$$

A capacitor of 20 μF is required as a power decoupling capacitor at 200V with ripple amplitude of 40V according to (22) when P_i=100W. The power decoupling operation discussed above results in the following effects:

(1) The DC input inductor current i_{LX} has a sawtooth waveform with a constant peak value, and then the low frequency ripple in the input inductor current is somewhat decreased;

(2) The DC input energy is stored in capacitor C_X, and the AC output energy is supplied from the same capacitor. Consequently, the low frequency power pulsation caused by the AC power is transferred into capacitor C_X, and the voltage on DC input capacitor C_{PV}, which is the same as that of the PV module, is kept constant;

(3) Because the capacitor voltage v_{CX} is much higher than the DC input voltage V_{PV}, energy transfer would also occur when the voltage fluctuation on C_X increases.

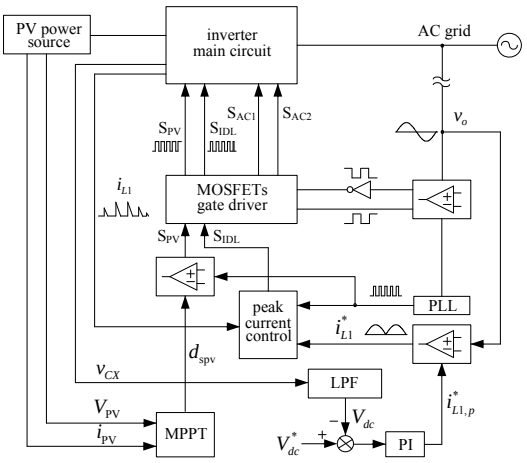

Fig.4. Control block

Control method

To synchronize the flyback inverter operation with improved power decoupling based on CI technique, a peak current mode control scheme is employed. Because the energy stored in C_X has a sinusoidal shape superimposed on a DC offset, that is, voltage v_{CX} doesn't keep constant. And there is a non-linear relationship between the PWM pulse width and the primary current i_{L1} in the whole line cycle. To generate the sinusoidal output current i_o, the primary current i_{L1} has to be controlled to make the peak current tracking sinewave line.

Fig. 4 gives the control block of the proposed single-phase flyback inverter, which is composed of voltage and current measurements, phase locked loop (PLL), MPPT

controller, peak current mode controller, PI controller and MOSFETs gate driver, etc. The input energy is calculated with PV source voltage and current detection, so that the duty-cycle of switch S_{PV} can be regulated to realize the MPPT function based on incremental conductance technique (ICT) [17].

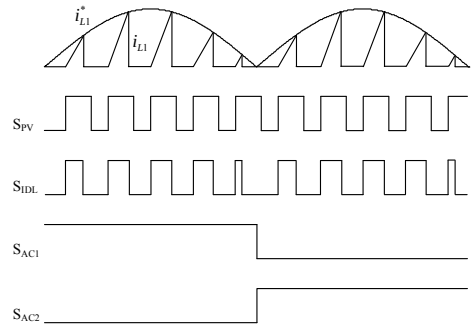

Fig.5. PWM generation

Fig. 5 shows the PWM signals for the four power switches in the proposed inverter. The primary current i_{L1} is detected and used to compare with AC grid synchronous reference signal. The primary peak current is related directly to the secondary peak current and the output current, so that the output current is controlled to follow a sinusoidal shape. In addition, the active switch S_{PV} is prescribed to operate with high-frequency at constant duty-cycle under steady state. The other active switches S_{AC1} and S_{AC2} are turned on or off during each of half line cycle to generate positive or negative output current with sinusoidal waveform.

Experimental results

The design process of the proposed PV inverter is considered in this section and experimental results are given based on a experimental prototype converter. The voltage stress of switch S_{PV} is expressed as:

(23) $$v_{spv,\max} = v_{CX,\max} - V_{\mathrm{PV}}$$

where $v_{CX,\max}$ is the peak voltage of capacitor C_X. The peak current of switch S_{PV} is approximately equal to

(24) $$i_{spv,p} = i_{LX,p} + i_{L1,p} = \sqrt{2}\sqrt{\frac{P_i}{L_X f_s}} + 2\sqrt{\frac{P_i}{L_1 f_s}}$$

where f_s is the switching frequency, $i_{LX,p}$ and $i_{L1,p}$ are the peak currents across the inductors L_X and $L1$, respectively. The voltage of switch S_{IDL} at the transformer primary-side is given as:

(25) $$v_{sidl,\max} = v_{CX,\max} + \frac{V_o}{n}$$

where n is the turns ratio between the secondary and primary windings. The peak current of switch S_{IDL} is expressed as:

(26) $$i_{sidl,p} = i_{L1,p} = 2n\sqrt{\frac{P_i}{L_1 f_s}}$$

The switch stresses of switches S_{AC1} and S_{AC2} are given as:

(27) $$v_{sac1,\max} = v_{sac2,\max} = 2V_o$$

(28) $$i_{sac1,p} = i_{sac2,p} = 2\sqrt{\frac{P_i}{L_1 f_s}}$$

To ensure the DCM operation for switch S_{IDL}, the following function must be satisfied.

(29) $$\frac{L_1 i_{L1,p}}{v_{CX,\min}} + \frac{L_2 i_{L2,p}}{V_o} < \frac{1}{f_s}$$

where $i_{L2,p}$ is the peak current across the inductor $L2$. So when $L_1=L_2$, we have

(30) $$L_1 < \frac{1}{4P_i f_s \left(\frac{n}{v_{CX,\min}} + \frac{1}{V_o}\right)^2}$$

where $v_{CX,\min}$ is the minimum voltage of capacitor C_X. The input inductor current must be also controlled to operate in DCM, so

(31) $$L_X < \frac{1}{2P_i f_s \left(\frac{1}{V_{\mathrm{PV}}} + \frac{1}{v_{CX,\min}}\right)^2}$$

In order to realize normal operation of the proposed inverter, the duty-cycle of S_{PV} must be greater than the maximum one of S_{IDL}, which can be given as:

(32) $$\frac{L_X i_{LX,p}}{V_{\mathrm{PV}}} > \frac{L_1 i_{L1,p}}{v_{CX,\min}}$$

Expression (32) can be simplified as:

(33) $$\frac{\sqrt{L_X}}{V_{\mathrm{PV}}} > \frac{\sqrt{2L_1}}{v_{CX,\min}}$$

The system parameters of the designed circuit are: (1) the input DC voltage V_{PV}=30V; (2) AC grid voltage v_o=100V(rms); (3) rated output power P_o=100W; (4) switching frequency f_s=20kHz. The average capacitor voltage reference is selected as V_{dc}^* =200V. The selected turns ratio between the secondary and primary windings is n=1 in order not to operate the circuit as a rectifier. The proposed single-phase flyback inverter with soft-switching operation has been verified by experimental results.

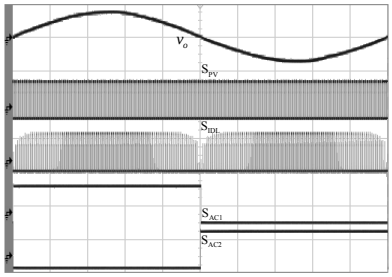

Fig.6. Experimental results of AC grid voltage and PWM signals(v_o: 200V/div.; S_{PV}, S_{IDL}, S_{AC1}, S_{AC2}: 20V/div.; time: 2ms/div.)

Fig. 6 shows the experimental results of the AC grid voltage and PWM signals of power switches S_{PV}, S_{IDL}, S_{AC1} and S_{AC2}. The duty-cycle of high-frequency switch S_{IDL} is controlled to follow a sinusoidal shape in phase with the AC grid voltage. Switches S_{AC1} and S_{AC2} are on or off in each of half line cycle.

Fig. 7 illustrates the measured capacitor voltage v_{CX}, AC grid voltage v_o and output current i_o. It can be seen that as predicted, the capacitor voltage v_{CX} has an approximately sinusoidal shape with twice the line-frequency superimposed on a DC offset. The measured output current is a sinusoidal wave with nearly unity power factor. The power factor of the output current is 0.991 based on the power meter measurement.

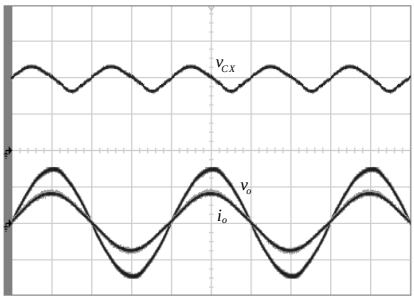

Fig.7. Idling capacitor voltage, output voltage and current [v_{CX}: 100V/div.; v_o: 100V/div.; i_o: 2A/div.; time: 5ms/div.]

The soft-switching dynamics of the high-frequency switches S_{PV} and S_{IDL} are measured and shown in Fig. 8 and Fig. 9, respectively. The two high-frequency switches are all turned on at ZCS due to DCM operation and turned off at ZVS based on capacitive idling technique. As a result, the power conversion efficiency is improved. The maximum conversion efficiency of the proposed inverter is 92.5% at the rated output power, and the transformer and MOSFETs are responsible for most of the power loss.

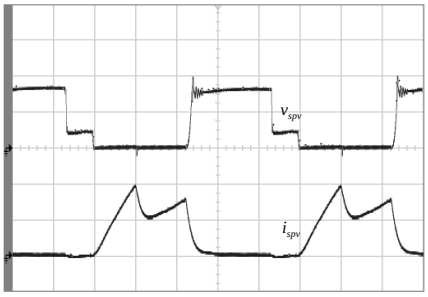

Fig.8. Voltage and current waveforms of S_{PV} [v_{spv}: 100V/div.; i_{spv}: 4A/div.; time: 10 μs /div.]

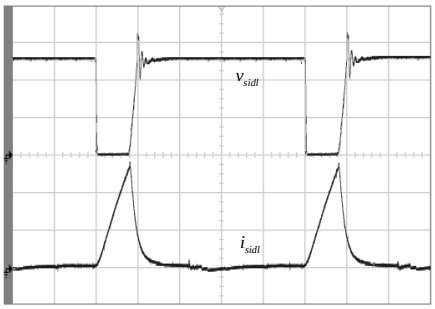

Fig.9. Voltage and current waveforms of S_{IDL} [v_{sidl}: 100V/div.; i_{sidl}: 4A/div.; time: 10 μs /div.]

Conclusions

A novel single-phase grid-connected flyback inverter for PV applications is proposed in this paper. Two high-frequency switches are used in the front-stage to achieve soft-switching at ZCS or ZVS based on capacitive idling technique, and the other two line-frequency switches in the flyback-stage are used to generate positive and negative output current. Furthermore, the power pulsation on the DC bus is converted into the voltage pulsation on a film capacitor with small capacitance, such that the low-frequency ripple current on the DC bus is reduced to obtain enhanced power decoupling. Peak current mode control scheme is employed to draw a sinusoidal output current into the AC grid. The experimental results show good output current waveform with nearly unity power factor and low current harmonics. According to the theoretical analysis and measured results with the adopted control algorithm, the proposed inverter has the properties of high power factor, low current distortion, small power decoupling capacitor and soft-switching operation.

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***Authors**: dr.Guanghui TAN, School of Electrical Engineering and Automation, Southeast University, Nanjing, 210096, China, E-mail: tanguanghui@seu.edu.cn; prof. Yanchao JI, School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin, 150001, China, E-mail: powerstar@163.com.*