

A compact cap-free headphone driver

Abstract. This paper proposes a compact structure to generate high rejection power supplies for proposed class AB amplifier (abamp). A NMOS-based low drop out regulator that does not require external compensation is utilized to provide a positive power supply. A regulated negative charge pump is utilized to provide a negative power supply. Chopper technology is utilized in the abamp to lower noise and offset. The driver could provide high power supply rejection (88dB at 217 Hz), high fidelity (74 dB total harmonic plus noise), low noise (7 μV) and low offset (1 mV) audio signals.

Streszczenie. W artykule zaproponowano kompaktową strukturę zasilacza ze sterownikiem o wysokiej skuteczności eliminacji szumów. W zasilaczu zastosowano tranzystor typu NMOS i sterowaną przetwornicę napięcia oraz chopper w celu redukcji szumów oraz offset-u. (Kompaktowy, bezkondensatorowy sterownik słuchawek).

Keywords: Headphone driver, NMOS LDO, negative charge pump, chopper

Słowa kluczowe: sterownik słuchawek, NMOS LDO, przetwornica napięcia, chopper

Introduction

Recent years have witnessed a growing market demand for audio amplifiers in multimedia equipment such as computers, mobile phones and other wireless equipments. The design of audio drivers in such environments must meet several challenging requirements: high audio fidelity, low noise (including electro magnetic interference, EMI), and strong immunity to noise (such as RF noise) [1]. High audio fidelity is required to support music playback at near-CD quality. Low noise and strong immunity is required to lower the interference to or from other devices.

Generally, two classes of power amplifiers are utilized for this application: Class D amplifier and Class AB amplifier (abamp). Class D amplifier provides the advantage of power efficiency at the cost of slightly reduced performance (especially noise and distortion) and a level of switching noise. It might, in some cases, interfere with RF functions such as the signal reception of mobile phone, GPS or FM radio. Owing to above reasons, an abamp that has the advantage of higher audio fidelity and no switching noise generation is preferred for headphone applications [2].

Normally, external high pass filters are used to cut-off the common mode voltage at the output of amps. Such filters, made of external capacitors of a few hundred of micro farads, are huge and expensive [3]. To avoid the use of output common-mode filter, a negative charge pump (NCP) is utilized to generate a negative power supply, so as to develop a cap-free abamp that is supplied by a symmetrical (positive/negative) voltage and has a ground common mode, as shown in Fig. 1. Due to the utilization of negative power supply, this type (cap-free) of headphone driver has a worse noise performance and power supply rejection (PSR) ability which is one of the most important characteristics for an audio amplifier, especially in mobile phone [4]. That makes an headphone driver has a weak immunity to interference within the audio band. For example, the 217 Hz transmit bursts in GSM phones may modulate the battery voltage and affect the audio performance if the driver has limited PSR.

Power supply noise could be suppressed by improving power supply rejection ratio (PSRR) of the abamp. Cascaded multi-stage configurations are mostly utilized to boost PSRR of abamp [5]. These architectures would difficult the compensation technology of abamp since they would boost the gain at same time [6]. A worse case is that the PSRR decreases quickly as frequency increases, and even no PSRR improvement because of device mismatch. Commonly used method to improve PSRR of cap-free headphone driver is inserting a PMOS LDO after battery supply (V_{CC}) and another LDO after the NCP [7]. The PSRR

of abamp is boosted by the high PSR power supplies provided by two LDOs. This method is very expensive since the PMOS LDO needs external compensations, which require additional cost on capacitances, pins, bonding wires, pads and die size.

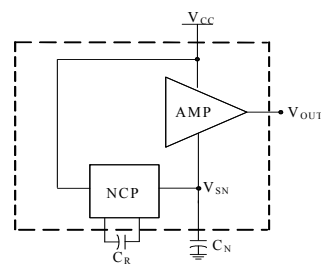


Fig. 1. A conventional cap-free headphone driver

This paper proposes a compact structure to generate high PSR positive and negative power supplies for a proposed amps, so as to generate a high PSRR (88 dB at 217 Hz), high fidelity (74 dB total harmonic plus noise, THD+N), low noise (7 μV) and low offset (1 mV) output audio signal. The cost is decreased since no external compensation is required. Section II describes the architecture of proposed headphone driver. Section III describes a NMOS based LDO for generating a positive power supply and a regulated negative charge pump for generating a negative power supply. Section IV describes the circuitry of structure of an abamp. The experimental results are shown in Section V. Finally, conclusions are drawn in Section VI.

Architecture

The block diagram of the headphone driver is shown in Fig. 2. The headphone driver comprises a cap-free (NMOS based) LDO to generate a high PSR positive power supply, a negative charge pump to generate a high PSR negative power supply, and two abamps utilizing chopper technology to lower the noise and offset. Due to the high PSR power supplies, PSRR of output audio signal is boosted.

A. Cap-free LDO

LDO voltage regulator is especially suitable to attain a high PSR power supply since it is easy to design and has no switching action during operation. PMOS power transistors are the natural choice but the resulting LDO regulator presents several drawbacks. Exemplary, with respect to the use of NMOS, PMOS-based voltage regulators have lower maximum output current (for the same area) and require complex frequency compensation

schemes with a large external capacitor for closed-loop stability. Recently, NMOS-based LDO regulators have been presented. To obtain the low drop-out feature, the power MOS gate of the NMOS-based LDO is raised above the supply voltage [8].

Fig. 3 illustrates a block diagram of proposed cap-free LDO shown in Fig. 2. It comprises of a voltage reference (V_{REF1}), a low gain error amplifier (EA1), a current source I_1 sunk by a NMOS M_1 , a power MOS (M_N) and a $2\times$ charge pump made up of capacitors C_F and C_S and switches S_0 – S_3 .

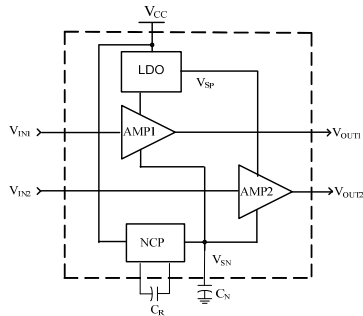


Fig.2. Proposed headphone driver

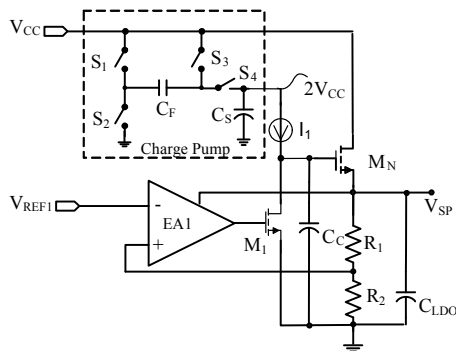


Fig.3. Block diagram of proposed cap-free LDO

Specifically, referring to the $2\times$ charge pump, during phase 1, switches S_2 and S_3 are closed and the voltage across C_F is charged to V_{CC} . Conversely, during phase 2, S_1 and S_4 are closed, and the voltage on C_F is added to V_{CC} , so as to obtain a $2\times V_{CC}$ voltage level at the output end of the charge pump. C_F and C_S are in parallel during phase 2 and the charge is redistributed between the two capacitors. After reaching the steady state, the voltage $2\times V_{CC}$ is stored across capacitor C_S and it serves as a voltage source.

The EA is supplied by the output voltage (V_{SP}) of the LDO itself, instead of battery voltage V_{CC} . It increases the PSRR of EA1 and further increases the PSRR of the cap-less LDO. For this reason, there is no need to consider the PSRR of EA1 when analysis the PSRR of presented LDO.

A feedback loop regulates V_{SP} around a constant voltage decided by R_1 , R_2 and V_{REF1} . A high PSR power supply voltage is obtained since V_{SP} is substantially not affected by V_{CC} . A capacitor C_C is utilized to compensate the dominate pole on the gate of M_N . The control loop is stable as long as the unity gain frequency (UGF) of the loop is smaller than the output pole. In a simplified calculation, the control loop has a phase margin of at least 60 degrees when the following condition is satisfied [9]:

$$(1) \quad 2 \times \frac{R_1}{R_1 + R_2} \times A_V \times \frac{G_{M1}}{C_C} < \frac{G_{MN}}{C_{LDO}}$$

where: A_V – gain of EA1, G_{M1} –transconductance of M_1 , G_{MN} –transconductance of M_N .

B. Negative Charge Pump

Fig. 4 illustrates a block diagram of the regulated NCP shown in Fig. 2. It comprises an open loop charge pump made up of C_R and C_N and switches S_5 – S_8 , two voltage references (V_{REF2} and V_{REF3}), a voltage divider and an operational error amplifier (EA2).

Specifically, referring to the charge pump, during phase 1, switches S_8 and S_7 are closed and the voltage across C_R is charged to V_{CC} . Conversely, during phase 2, S_5 and S_6 are closed, one terminal of the C_R is coupled to ground through S_5 , and a negative V_{CC} is obtain on the other terminal since the voltage between two terminals can not change immediately. C_R and C_N are in parallel and the charge is redistributed between the two capacitors. After reaching the steady state, the voltage $-V_{CC}$ is stored across capacitor C_N that serves as a voltage source.

The output of NCP is easy to be affected by the V_{CC} or load current when NCP runs in open loop. So, EA2 is utilized to control the on resistance/current of switch S_2 to obtain a regulated output voltage that is give as

$$(2) \quad V_{SN} = \frac{R_3 + R_4}{R_3} \times V_{REF3} - \frac{R_4}{R_3} \times V_{REF2}$$

When the negative voltage V_{SN} increases, the output of EA2 also increases to reduce the on-state resistance of switch S_2 or to increase the charge current. Thus the negative voltage V_{SN} falls off. The negative voltage V_{SN} is regulated by the feedback loop and is independent from the input voltage V_{CC} . And nearly no change may occur on the negative voltage V_{SN} when the input voltage V_{CC} is changed. Therefore, high PSR negative power supply is obtained.

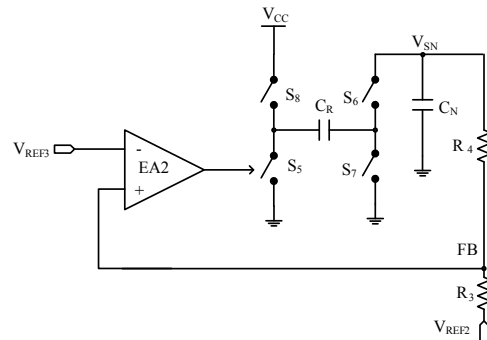


Fig.4. Block diagram of proposed NCP

C. Class AB amplifier

Fig. 5 illustrates a block diagram of the amp shown in Fig. 2. The amp comprise an input stage utilizing chopper technology to lower noise and offset, an output stage to drive the headphones and to filter high frequency noise.

A conventional CMOS amplifier has a typical input-referred noise spectrum. At relative low frequency range, the noise power is increasing almost linearly with decreasing frequency and is therefore commonly called $1/f$ noise. For rather high frequency range, the noise can be considered as frequency independent or white. This is usually called the thermal noise floor. The frequency at which the $1/f$ noise becomes dominant over the white noise is called the noise corner frequency f_c . Although offset is usually modelled as a time-invariant voltage source, it may change as aging or temperature variations. This implies that it has a certain bandwidth and can therefore be considered as a very low-frequency noise source [10].

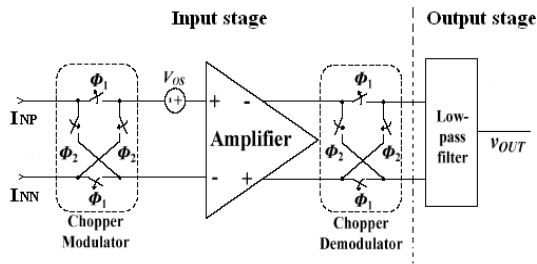


Fig.5. Block diagram of proposed abamp

The principle of the chopper technique is shown as follows. The chopper modulator modulates the differential input signals from audio frequency bands (20-20K Hz) to a higher chopping frequency ($10\times$ larger than 20K), and the chopping frequency is determined by the biphasic non-overlapping control signals Φ_1 and Φ_2 . The amplifier amplifies both the modulated differential input signals (I_{NP} and I_{NN}) and its combined input-referred noise and offset (V_N+V_{OS}). The chopper demodulator subsequently demodulates the amplified input signal back to its original low frequency but modulates the amplified noise and offset to the chopping frequency. So, the respective frequencies of the amplified input signal and the amplified V_N+V_{OS} are effectively separated. Finally, the low-pass filter recovers the amplified input signal and attenuates the noise and offset [11].

III. Realization of power supplies

To test and prove this theory, power supplies employing the proposed cap free LDO and NCP is designed to supply two abamps.

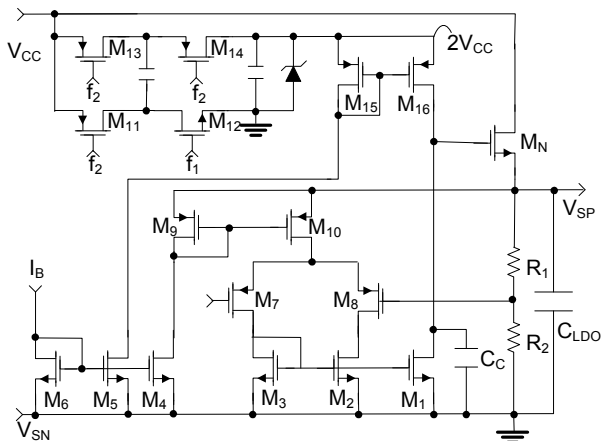


Fig.6. Schematic circuit of proposed cap-free LDO

A. Realization of cap-free LDO

Fig. 6 illustrates a schematic circuitry of the cap-less LDO shown in Fig. 2 and Fig. 3.

Switches S_1 , S_3 and S_4 of the charge pump are implemented with PMOS transistors M_{11} , M_{13} and M_{14} respectively while S_2 is implemented with NMOS transistors M_{12} . A pair of converse clock f_1 and f_2 is used to turn on/off above transistors. An enough dead time should be reserved to prevent punching through. Bulk of M_{13} is connected to one terminal of C_R instead of V_{CC} , and bulk of M_{14} is connected to $2\times V_{CC}$. A Zener diode with 7.5 V breaking down voltage is connected to $2\times V_{CC}$ to protect devices from

being damaged. For example, $2\times V_{CC}$ is clamped around 7.5 V instead of rising to 10 V even V_{CC} is up to 5V.

M_1 , M_2 , M_3 are matched NMOS, the same as M_4 , M_5 , M_6 . M_7 is matched with M_8 , same as M_{15} and M_{16} . M_{10} is 2 times of M_9 . So, M_1 and M_{16} have same current I_B during steady state. M_1 pushes up voltage on gate of M_N when V_{SP} is lower than a predetermined level; conversely, M_1 pulls down voltage on gate of M_N when V_{SP} is higher than the predetermined level.

According to (1), the lowest phase margin occurs at the situation of minimum load current. It is always possible to make G_{MN} larger than G_{M1} since tail current of the EA1 is part of the current through M_N . It makes the system stable for all load currents including the worst case no load situation.

B. Realization of the regulated NCP

Fig. 7A illustrates a schematic circuitry of regulated NCP shown in Fig. 2 and Fig. 4. The NCP comprise a PMOS transistor E_1 to implement switch S_8 , three NMOS transistors $E_2\sim E_4$ to implement switches $S_5\sim S_7$, an inverter comprising E_5 and E_6 , an error amplifier EA2 to amplify the difference between V_{REF2} and a feedback voltage (FB), and a buffer to enhance load ability of the amplifier EA2. The schematic circuitry of amplifier EA2 and the buffer are shown in Fig. 7B and Fig. 7C.

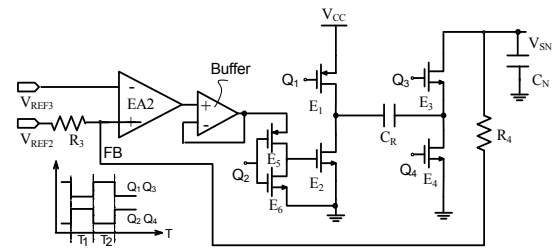


Fig. 7A. Schematic circuitry of proposed regulated NCP

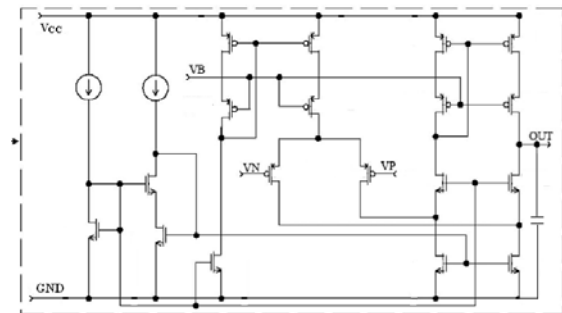


Fig. 7B. Schematic circuitry of proposed EA2

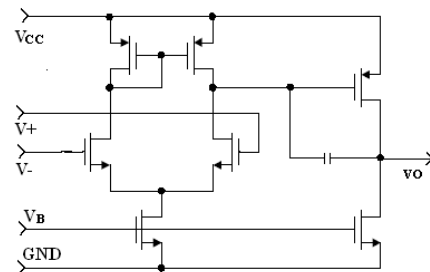


Fig. 7C. Schematic circuitry of proposed buffer

Normally, V_{REF2} equals to ground voltage level. So, PMOS input transistors are utilized in EA2. EA2 also utilizes folded-cascode architecture to get better PSR performance.

The detail introduction is abbreviated hereby since it is a commonly used architecture.

The buffer also utilizes a common used two stage amplifier with miller compensation. The output stage utilizes PMOS transistor to provide enough load ability.

The gate of transistors E_1 , E_2 , E_3 and E_4 are controlled by control signals Q_1 , Q_2 , Q_3 and Q_4 that are shown in Fig. 8A. At the first period T_1 , control signals Q_1 and Q_3 are at low level while Q_2 and Q_4 is at high level. As a result, transistors M_1 and M_4 turn on while E_2 and E_3 turn off. The power supply voltage V_{CC} charges the capacitor C_R . At the second period T_2 , control signals Q_1 and Q_3 are at high level while Q_2 and Q_4 are at low level. So transistor E_1 and E_4 turn off while E_2 turn on. E_3 is regulated by the output signal of the amplifier EA2. During this period, E_3 is configured to be a voltage-controlled current source or a voltage-controlled resistor. Thus, the capacitor C_R charges capacitor C_N at period T_2 when the charging current is controlled by the regulating signal E_2 from the error amplifier EA2. So a regulated V_{SN} is obtained.

IV. Realization of the amp

Fig. 9A shows a schematic circuitry of the amp shown in Fig. 2 and Fig.5. The amp has two stages: a folded cascode input stage configured to provide a voltage gain, and a class-AB output stage configured to provide the headphone driving capability. The specific circuit of the bias circuit of the amp shown in Fig. 8A is shown in Fig. 8B.

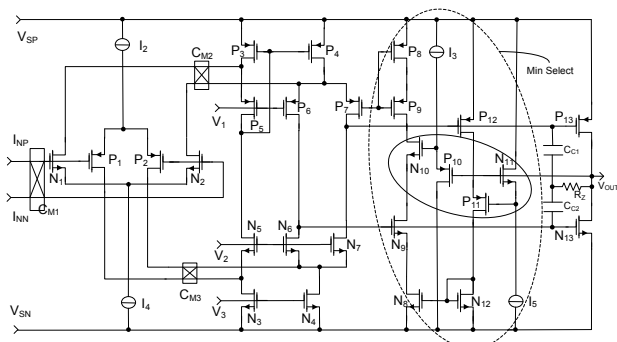


Fig. 8A. Schematic circuitry of proposed abamp

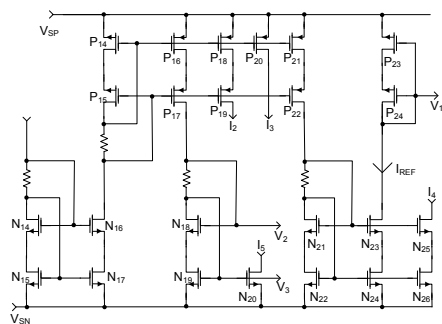


Fig. 8B. Bias circuitry of proposed abamp

A. Input stage

Due to the strong noise immunity ability, differential input signals gain more and more popular. For an application with differential input signal, input voltage would runs widely, even near the power supply rail. As the input voltage is rail to rail, we need an input stage that can operate under voltage from V_{SN} to V_{SP} . That is realized by using complementary pairs (P_1 , P_2 , N_1 , and N_2) that will conduct between the whole input common mode levels.

The chopper modulator C_{M1} is located after input signal while C_{M2} and C_{M3} are located after input transistors. Selection the size of the chopper modulator switches should

consider the compromise between charge injection and thermal noise. A larger size reduces thermal noise while increases charge injection conversely. Herein, minimum size is adopted since they have little effect to total noise and offset. The chopping frequency needs to be optimized to obtain a good compromise between noises and offset. The specific trade-off is that while a higher chopping frequency reduces noise (particularly flicker noise), it conversely increases the offset that is induced by charge injection and clock-feed through at the chopper modulator. Herein, 250K is adopted.

B. Output stage

To make sure the stability of the amp, the output utilizes miller capacitance C_{C1} , C_{C2} and resistor R_Z configured to compensate the loop. The output stage also works as a low pass filter for reducing the modulated offset and noise from the input stage.

The output stage of the abamp incorporates a minimum current selector (N_8 , N_9 , N_{12} , P_{12}) in a feedback loop [12]. The bias current of the output transistors is determined by the current mirror ratio between the minimum current selector and the output transistors.

Specifically, P_8 , P_9 , P_{23} and P_{24} are matched device. Assuming they are working in saturation region, they share the same reference current I_{REF} if the gate voltage of P_8 and P_9 are equal to V_1 . The current summing branch (N_4 , N_6 , N_7 , P_4 , P_6 , P_7) forms an amplifier, which regulates the quiescent current of the abamp output stage (N_{13} , P_{13}) together with the minimum current selector. Thus, the output current of the minimum current selector flowing through P_{12} is regulated to be equal to the reference current I_{REF} by this amplifier. N_8 and N_9 are matched to N_{12} , but are biased in such a way that they serve as a composite transistor with half the effective aspect ratio of P_{14} in a quiescent state. Hence, the quiescent current of the output transistors (P_{13} , N_{13}) is equal to

$$(3) \quad I_Q = 2 \times I_{REF} \times \frac{W_{P13} \times L_{P12}}{W_{P12} \times L_{P13}}$$

When P_{13} sources a large output current from the load, a large current flowing through P_{12} and N_{12} pulls the voltage level on the source of N_9 down to the V_{SN} . N_9 and N_{13} now operate as a current mirror, and the current on N_{13} is scaled down from the current on N_9 according to the mirror ratio between N_{13} and N_9 . This means that the minimum standby current flowing through the output transistor (N_{13}) is half of the quiescent current. On the other hand, when the output transistor (N_{13}) sinks a large output current to the load, the drain-to-source voltage of N_8 will be sufficiently high, so that N_8 enters into the saturation region. Then, N_8 and N_{12} form a current mirror, and the drain current of P_8 and P_9 are equal to that of P_{12} . This sets the minimum standby current of the output transistor (P_{13}) to be also half the output stage quiescent current.

N_{10} , N_{11} , P_{10} , and P_{11} are provided to reduce the channel length modulation effect of P_{12} and N_8 .

V. Measurement results

The driver prototype was fabricated in HHNEC 1.2um BCD technology. The die photograph marked with essential circuit components is shown in Fig. 9. The total layout area occupied 2.25 mm² (1500 μm×1500 μm).

Fig. 10 shows a test result of the THD+N as a function of output power. The V_{CC} is 5V, input signal is set at 1 kHz, and the load is 32Ω. For small output amplitude cases, THD+N are limited by the noise and hence decreases as the output power increases. The max power for each channel with 32Ω load is about 100mW.

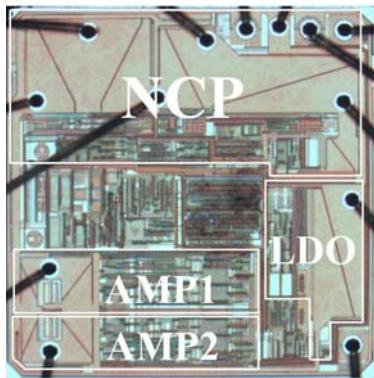


Fig. 9. Layout micrograph of proposed headphone driver

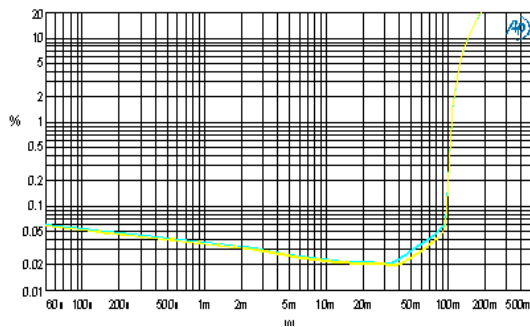


Fig. 10. THD+N Vs output power with 32Ω headphone

Fig. 11 shows a test result of the PSRR as a function of frequency. The DC PSRR is about 90 dB. Specially, at 217 Hz, which stand for GSM emission perturbation, PSRR is above 88 dB.

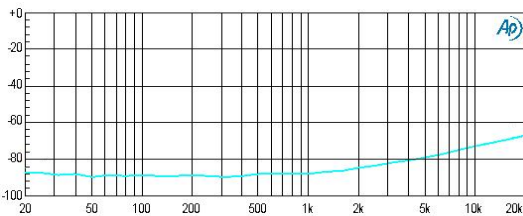


Fig. 11. PSRR Vs frequency

Fig. 12 shows measured FFT of output signal with zero input condition. Total noise (20~20K Hz) is about 7μV.

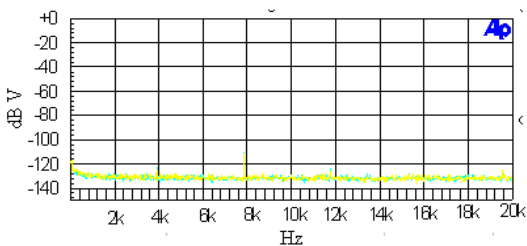


Fig. 12. FFT analysis of noise floor

Fig. 13 shows the distribution (Y axis is sample quantity and corresponding percent) of output offset with zero input condition. The offset is distributed between -1 mV to 1 mV.

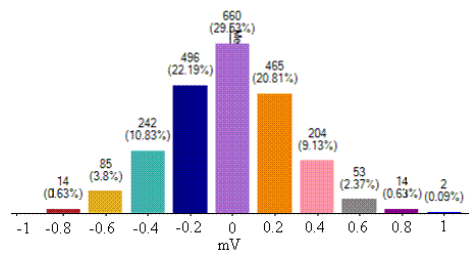


Fig. 13. Offset distribution

VI. Conclusion

A NMOS-based LDO regulator that does not require external compensation and a regulated negative charge pump are utilized to generate a symmetrical supplies for headphone driver. Chopper technology is utilized to lower the noise and offset of an amp. Test results show that the driver could provide a high power supply rejection ratio (88 dB at 217 Hz), high fidelity (74 dB total harmonic plus noise), low noise (7μV) and low offset (1mV) output audio signal with low quiescent current consumption (2mA per channel).

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