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Improvement of Input Power Factor in PWM AC Chopper by Selecting the Optimal Parameters

***Abstract**. A technique for selecting the element values of the PWM AC chopper circuits to improve the input power factor is presented. This technique analyzes the phase angles of input current, output current and voltage for selecting the optimal value of the filter capacitance. This produces the phase angle of input current in phase with that of input voltage. Therefore, the PWM AC chopper can operate at unity input power factor. The simulation by PSpice program and experimental results are used to verify the proposed technique.*

***Streszczenie.** Zaprezentowano metodę selekcji elementów choppera PWM AC w celu poprawy wejściowego współczynnika mocy. Metoda polega na analizie kąta fazowego prądu wejściowego, prądu wyjściowego i napięcia w celu optymalizacji pojemności filtru. Dzięki temu chopper pracuje przy współczynniku mocy równym 1. (**Optymalny dobór elementów choppera PWM AC w celu poprawy wejściowego współczynnika mocy**)*

Keywords: Buck, boost, buck-boost AC choppers, capacitor filter, pulse width modulated (PWM) AC chopper, power factor
Słowa kluczowe: chopper PWM AC, optymalizacja, współczynnik mocy

Introduction

To variable AC voltage from fixed AC source, there are three basic techniques that have been widely used in AC power applications such as lighting control, industrial heating, soft start induction motor and speed controller for fans and pumps [1]. The first one is the auto transformer. Its winding ratio is controlled by servo motor or by manual regulation. Although, it offers some advantages such as durability and reliability, it has low voltage regulation speed and large size [2]–[4]. The second technique is the phase angle control. The output voltage average can be controlled by firing angle of thyristor [5]. It has some advantages such as simplicity of the control circuit and capability of controlling a large amount of economical power. However, the delay of firing angle causes discontinuation of power flow to appear at both input and output sides, and significant harmonics in load current. This causes a lagging input power factor (PF_i) to occur at the input side, especially, when the firing angle is high.

These problems can be solved by pulse width modulated (PWM) AC chopper technique [6]-[8]. In this technique, the AC line voltage will be chopped by PWM signal controller producing the output voltage. From this process, it produces the input-output current and output voltage to be near sinusoidal. Therefore, its total harmonic distortion THD is low, and the input power factor, PF_i, is high. Although, the PF_i of PWM AC chopper technique is higher than that of the phase angle control technique, the PF_i still depends on the load power factor. When the load power factor is low, the PF_i will be low as well. This concerned problem can be solved by two ways. The first way is to improve PWM process. The reference and triangular carrier signals were modified to shift the phase angle of output voltage [9]-[14]. This process results the phase angle of input current also shifted. Therefore, the PF_i is improved. Although, these techniques can improve the PF_i, they are difficult to implement and cause plentiful harmonics in load voltage. The second way is to select the element values of PWM AC chopper circuit. The estimation of the filter capacitance and inductance values by observing the experimental results was proposed [7]. However, this algorithm is difficult to be used in practical circuit design. The selecting the optimal value of the filter capacitance was proposed [15]. However, this technique considered the effect of the filter capacitance value on PF_i only.

Therefore, this paper proposes the technique for selecting the optimal value of the filter capacitance based on PWM buck, boost and buck-boost AC chopper topologies and also considers its effect on the output voltage ripple. This paper is organized as the following sections. Section 2 presents the fundamental operation of the PWM buck, boost and buck-boost AC chopper topologies. In Section 3, the phase angles of input current, output current and voltage are analyzed. Finally, in this section, we analyze the optimal value of the filter capacitance and show the designed step for unity input PF_i. Section 4 shows the simulation results by PSpice program. Section 5 shows the results by experiment. In the last section, the conclusion is presented.

PWM AC chopper operation

The PWM buck, boost and buck-boost AC chopper power circuits as shown in Fig. 1 consist of input voltage source V_i, inductor L, filter capacitor C and four power switches. Inductor L_f and capacitor C_f is an input filter to absorb high-order harmonic component.

The switching patterns are decided by the polarity of the input/output voltage as shown in Table 1. The switch S_1 and S_2 provide the energy storage in inductor and transfer the energy to the output load. While, the switches S_3 and S_4 are the freewheeling paths for continuous load current, whereas S_1 and S_2, respectively, are in the off-state. In buck topology, when the polarity of input voltage is positive, the switches S_2 and S_4 are fully turned on. While, the switch S_1 is turned on by controlling of the duty cycle, D, for transferring path. The energy from source will be delivered toward the output load. After the switch S_1 is turned off, the switch S_3 will be turned on by controlling of $1-D$ for freewheeling path. On the other hand, the polarity of input voltage is negative. The switches S_1 and S_3 are fully turned on while the switches S_2 and S_4 are controlled by D and $1-D$, respectively.

Table 1. PWM patterns of all switches.

Voltage	S_1	S_2	S_3	S_4
$V_i > 0*$	1	1	0	1
$V_o > 0**$	0	1	0	1
	0	1	1	1
$V_i < 0*$	1	1	1	0
$V_o < 0**$	1	0	1	0
	1	0	1	1

*, buck and buck-boost type; **, boost type

In the PWM boost AC chopper, the switching patterns are decided by the polarity of the output voltage. For the

PWM buck-boost AC chopper, the switching patterns are the same as the PWM buck AC chopper. All switches operate at a fixed switching frequency and a constant duty cycle.

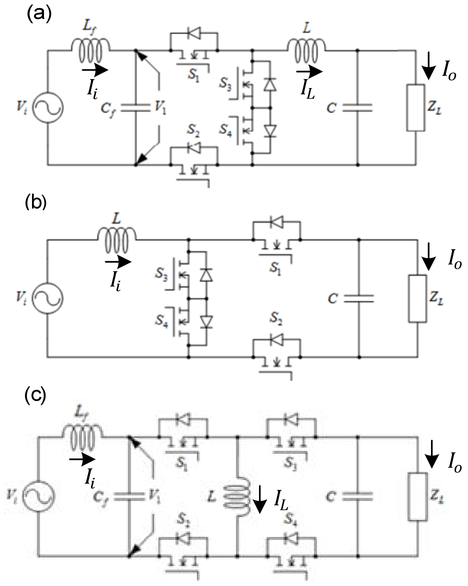

Fig.1. Topology of PWM AC chopper: (a) Buck type, (b) boost type and (c) buck-boost type.

System analysis and calculation

To facilitate the analysis and calculation, the following assumptions were made. All components are assumed ideal. The switching frequency f_s is much higher than the supply frequency f_i.

Buck type topology

In switching period, the input voltage V_i, the voltage across the capacitor C_f, V_1, and the output voltage V_o are considered to be constant. When, $V_i > 0$, the voltage across the inductor is obtained:

(1) $$V_L = \begin{cases} V_1 - V_o, & 0 < t < DT \\ -V_o, & DT < t < T \end{cases}$$

From Fig. 1a, the voltage across the capacitor C_f and the input current are found by

(2) $$V_1(s) = V_i(s) - sL_f I_i(s)$$

(3) $$I_i(s) = sC_f V_1(s) + DI_L(s)$$

Substituting (3) in (2), yields

(4) $$V_1(s) = \frac{V_i(s) - DsL_f I_L(s)}{(1+s^2 L_f C_f)}$$

In the average model of the switching period, the average voltage of the inductor is given by

(5) $$V_L(t) = D[V_1(t) - V_o(t)] - (1-D)V_o(t)$$

where $V_1(t)$ and $V_o(t)$ are the average input and output voltage respectively, and D is the duty ratio. When the input and output voltage are induced on the inductor by PWM switches in the high frequency switching, it is possible to estimate the average inductor voltage expressed as:

(6) $$V_L(t) = L\frac{di_L(t)}{dt}$$

From Eqautions (5) and (6), the following relation is obtained:

(7) $$DV_1(t) = L\frac{di_L(t)}{dt} + V_o(t)$$

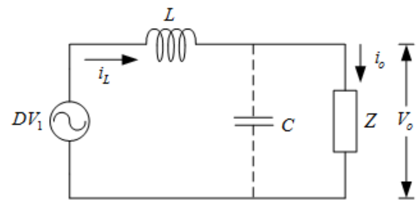

Fig.2. Steady-state equivalent circuit of PWM buck AC chopper.

The equivalent circuit of Eqaution (7) is shown in Fig. 2. The output filter is used to reduce the output voltage ripple and keep the current continuous conduction. The inductor current ripple Δi_L can be expressed as:

(8) $$\Delta i_L = \frac{1}{L}[V_{op}T(1-D)]$$

Therefore, the filter inductance L used to determine the maximum current ripple can be found by

(9) $$L = \frac{V_{op}T(1-D)}{\Delta i_L}$$

where T is a switching time. To limit the peak-to-peak value of the output voltage ripple below a certain value Δv_o, the filter capacitance value must be greater than

(10) $$C_{min} = \frac{(1-\mathrm{D})V_{op}}{8L\Delta v_o f_s^2}$$

where, V_{op} is the peak output voltage. From Equation (10), it shows that the filter capacitance value affects the output voltage ripple. In addition, it also affects the PF_i. In Fig. 2, the equivalent circuit is assumed without the filter capacitor C. Therefore, the inductor current i_L is equal to the output current i_o. This means that the phase angle of i_L is in phase with that of i_o. Consequently, the input power factor depends on the load power factor. This assumption is shown in Fig. 3. When the filter capacitor C is inserted into the circuit, the phase angle of input current θi_i will be closely shifted to the phase angle of the input voltage θv_i. Therefore, the capacitance value impacts the phase angle of input current θi_i. It causes leading or lagging input power factor.

As previously discussed, it was indicated that the capacitance value affects the output voltage ripple and PF_i. In some applications, low output voltage ripple may be required. Therefore, the large capacitance value is selected. This causes the PF_i to be low. While, in some applications, the power factor problem may be concerned. Therefore, the optimal capacitance value should be selected for converter operating at unity input power factor.

From the equivalent circuit of converter, it is assumed without the filter capacitor C and Z is the load impedance ($Z = R_o + j\omega L_o$). Therefore, the transfer function of the output voltage $V_o(s)$ with respect to the input voltage $V_i(s)$ is obtained as

(11) $$\frac{V_o(s)}{V_i(s)} = \frac{D(sL_o + R_o)}{b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$

where $b_3 = (LL_f C_f + L_o L_f C_f)$, $b_2 = R_o L_f C_f$, $b_1 = (L + L_o + L_f D^2)$, $b_0 = R_o$.

To find the optimal capacitance value, we need to know the difference between the phase angle of input and output voltage. From Equation (11), the phase angle between $V_o(s)$ and $V_i(s)$ is obtained as

(12) $$\theta v_{io} = tan^{-1}\omega\left(\frac{L_0}{R_0}\right) - tan^{-1}\omega\left(\frac{a_2\omega^2+a_1\omega+a_0}{R_0}\right)$$

where $a_2 = (LL_fC_f + L_oL_fC_f)$, $a_1 = R_oL_fC_f$, $a_0 = (L + L_o + L_fD^2)$

Boost type topology

In case of the boost AC chopper, the equivalent circuit as shown in Fig. 4 is found by Equation (13).

(13) $$\frac{V_i(t)}{(1-D)} = \frac{L}{(1-D)^2}\frac{di_o(t)}{dt} + V_o(t)$$

The boost inductor L used to determine the maximum current ripple is given by

(14) $$L = \frac{V_{ip}DT}{\Delta i_L}$$

While, the minimum value of the filter capacitance for determining the output voltage ripple Δv_o is given by

(15) $$C_{min} = \frac{I_{op}DT}{\Delta v_o}$$

where, V_{ip} and I_{op} are the peak input voltage and the peak output current. The equivalent circuit is assumed without the filter capacitor C. Therefore, the transfer function of the output voltage $V_o(s)$ with respect to the input voltage $V_i(s)$ can be expressed as

(16) $$\frac{V_o(s)}{V_i(s)} = \frac{sL_o(1-D)+R_o(1-D)}{s[L+L_o(1-D)^2]+R_o(1-D)^2}$$

From Eq. (16), therefore, the phase angle between $V_o(s)$ and $V_i(s)$ can be found:

(17) $$\theta v_{io} = tan^{-1}\omega\left(\frac{L_o}{R_o}\right) - tan^{-1}\omega\left(\frac{L+L_o+(1-D)^2}{R_o(1-D)^2}\right)$$

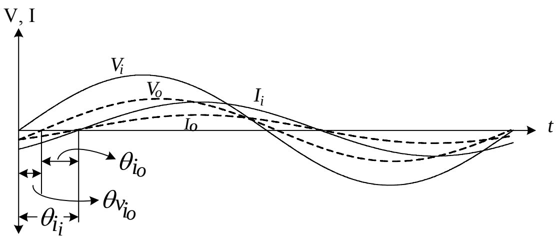

Fig. 3. Phase angles of equivalent circuit in Fig. 2 (without C).

Buck-boost type topology

Fig. 5 shows the equivalent circuit for buck-boost AC chopper that is generated by Equation (18). Because of its configuration, is similar to that of the boost converter. Thus, the values of inductor L and the filter capacitor can be obtained by Equations (14) and (15), respectively.

(18) $$\frac{DV_i(t)}{(1-D)} = \frac{L}{D(1-D)}\frac{di_L(t)}{dt} + V_o(t)$$

Assume that the equivalent circuit is without the filter capacitor C. Therefore, the transfer function of the output voltage $V_o(s)$ with respect to the input voltage $V_i(s)$ can be expressed as

(19) $$\frac{V_o(s)}{V_i(s)} = \frac{D(sL_o+R_o)}{b_3s^3+b_2s^2+b_1s+b_0}$$

where $b_3 = (LL_fC_f + L_oL_fC_f - L_oL_fC_fD)$, $b_2 = (R_oL_fC_f - R_oL_fC_fD)$, $b_1 = (L + L_o + L_fD^2 - L_oD)$, $b_0 = R_o(1-D)$.

From Equation (19), the phase angle between $V_o(s)$ and $V_i(s)$ is obtained as

(20) $$\theta v_{io} = tan^{-1}\omega\left(\frac{L_0}{R_0}\right) - tan^{-1}\omega\left(\frac{a_2\omega^2+a_1\omega+a_0}{R_0(1-D)}\right)$$

where $a_2 = (LL_fC_f + L_oL_fC_f - L_oL_fC_fD)$, $a_1 = (R_oL_fC_f - R_oL_fC_fD)$, $a_0 = (L + L_o + L_fD^2 - L_oD)$.

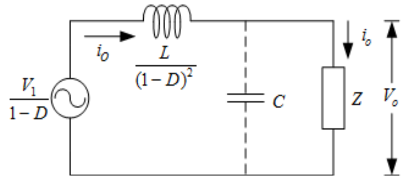

Fig. 4. Steady-state equivalent circuit of PWM boost AC chopper.

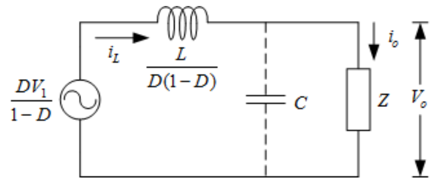

Fig.5. Steady-state equivalent circuit of PWM buck-boost AC chopper.

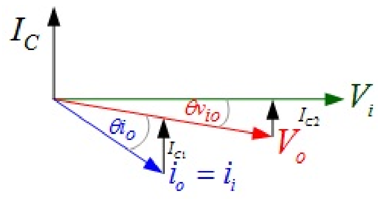

Fig.6. Phasor diagram n case of inductive load.

Optimal capacitance for unity input power factor

Some cases of the applications, the converter operates at fixed load impedance and a constant duty cycle. Therefore, the values of the circuit elements can be selected for unity input power factor. Considering Fig. 6, the input current i_i is equal to the output current i_o and the phase angle of input voltage leads that of the output voltage and current with θv_{io} and θi_o respectively. When, the filter capacitor C is connected in parallel with the output load. This produces the phase angle of input current θi_i shifted to the phase angle of output voltage θv_o by I_{C1} and then shifted to the phase angle of input voltage θv_i by I_{C2}. Therefore, if the optimal capacitance value is selected resulting the phase angles of the input current and input voltage are in phase. The optimal capacitance value for improving the input power factor can be obtained by

(21) $$C = C_1 + C_2 = \frac{Ptan\theta i_o}{\omega V_{orms}^2} + \frac{Ptan\theta v_{io}}{\omega V_{orms}^2}$$

Where, C_1 is the filter capacitor for producing the current I_{C1}, C_2 is the filter capacitor for producing the current I_{C2}, P is the real power of load and V_{orms} is the root mean square of output voltage.

Designing example

This sub session shows the guideline for designing the PWM buck AC chopper converter. The parameters are shown in Table 2. From this information, we design the converter parameters by the step as follows:

1. The output current is
$$I_{orms} = \frac{P}{V_{orms}cos\theta} = \frac{1{,}000}{110 \times 0.8} = 11.36\text{ A}$$

Therefore, the inductor current ripple, Δi_L is determined by

$$\Delta i_L = 0.071 \times 11.36 \times \sqrt{2} = 1.14\ \text{A}$$

2. The filter inductance and capacitance values are obtained:

$$L = \frac{\sqrt{2}V_o T(1-D)}{\Delta i_L} = \frac{155 \times 5 \times 10^{-5} \times 0.5}{1.14} = 3.4\ \text{mH}$$

$$C_{min} = \frac{(1-0.5) \times \sqrt{2} \times 110}{8 \times 3.4 \times 10^{-3} \times 1.1 \times (20 \times 10^3)^2} = 6.46\ \mu\text{F}$$

3. The phase angle between $V_o(s)$ and $V_i(s)$ using Eq. (12) is

$$\theta v_{io} = 5.09^{\text{o}}$$

4. Finding the optimal filter capacitance C using Eq. (21) is obtained as

$$C = 220\ \mu\text{F}$$

From the designed step, the optimal capacitance value for improving the PF_i is $220\ \mu\text{F}$, which is higher than C_{min}. This shows that it produces the unity PF_i and forces the output voltage ripple within designed value $\Delta v_o = 1\%$ (1.1 V). This designed step can be used in other topologies as well.

Table 2. The PWM AC chopper specifications

Parameters	Buck	Buck-Boost	Boost
Input Voltage	220 Vrms, 50 Hz		110 Vrms, 50 Hz
Duty Cycle	0.5		
Switching Frequency	20 kHz		
Inductor Filter	1 mH	1 mH	-
Capacitor Filter	1 μF	4.7 μF	-
Output Voltage Ripple	1 %		
Output Current Ripple	7.1 %		
Power	1000 W		
Power Factor	0.8 Lagging		

a)

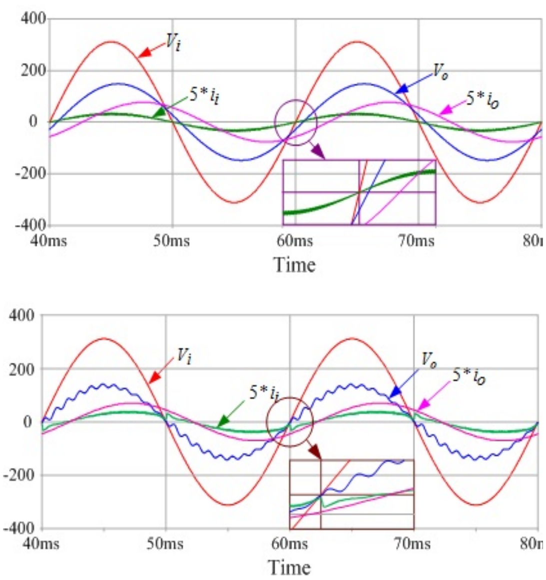

Fig.7. Wave forms of PWM buck AC chopper with: (a) optimal capacitor ($C = 220\ \mu\text{F}$) and (b) without optimal capacitor ($C = 6.46\ \mu\text{F}$).

Simulations

To show the feasibility of the proposed analysis method, PSpice program (Student version) was used. The design parameters of PWM AC chopper in the design example are used for simulation. The simulation results are shown in Fig. 7 to 17. Fig. 7 shows the waveforms of load current, output voltage, input current and input voltage in PWM buck AC chopper. From the results, the power factor at supply side is unity.

This is because the optimal capacitance value is selected as shown in Fig. 7a. The total harmonic distortion of output current/voltage is 0.026% and the input current is 0.205%. While, the minimum capacitance value used to meet the maximum output voltage ripple is $6.46\ \mu\text{F}$ (without the optimal capacitance value). As shown the waveforms in Fig. 7b, the total harmonic distortions of output current/voltage are 0.51% and the input current is 9.316%.

Because of the optimal capacitance value selected, the PF_i is unity. Therefore, if its value is higher or lower than $220\ \mu\text{F}$ resulting the lagging or leading input power factor as shown the results in Fig. 8. Figure 9 shows the PF_i as a function of D. It indicates that D little affects the PF_i if the optimal capacitance value is used.

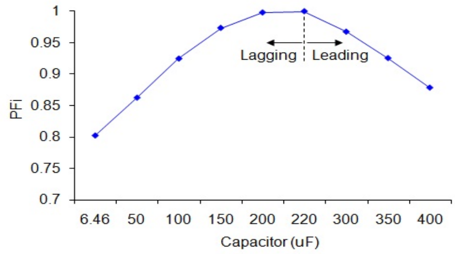

Fig.8. Input power factor versus capacitance of C (buck type).

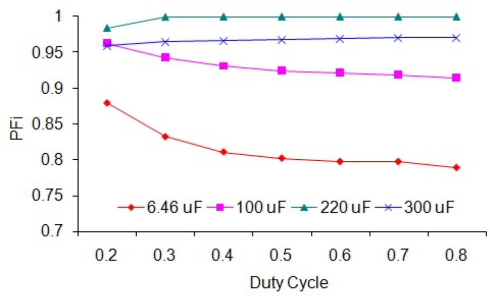

Fig.9. Input power factor versus duty cycle, D (buck type).

Fig. 10 shows the waveforms of PWM boost AC chopper topology. From the parameters as shown in Table 2, using the design step of the proposed method, the boost inductance value is $6.8\ \text{mH}$ and the optimal capacitance value is $60\ \mu\text{F}$. While, the minimum capacitance value designed to meet the maximum output voltage ripple is $114\ \mu\text{F}$. From the results, the power factor at supply side is unity because of the optimal capacitance value selected as shown in Fig.10a. While, the THD of output current/voltage is 0.026% and the input current is 0.101%. Fig. 10b shows the results without the optimal capacitance value. It shows the leading input power factor because the capacitance value is higher than $60\ \mu\text{F}$. Figure 11 to 12 shows the PF_i as a function of C and D. The parameters of PWM buck-boost AC chopper topology as shown in Table 2, using the design step, the inductor L is $3.9\ \text{mH}$ and the optimal capacitance value is $53\ \mu\text{F}$. Figure 13 shows the waveforms of load current, output voltage, input current and input voltage. From the results, the power factor at supply side is unity. While, the THD of output current/voltage is

0.815% and the input current is 6.99%. Figure 14 to 15 show the PF_i as a function of C and D.

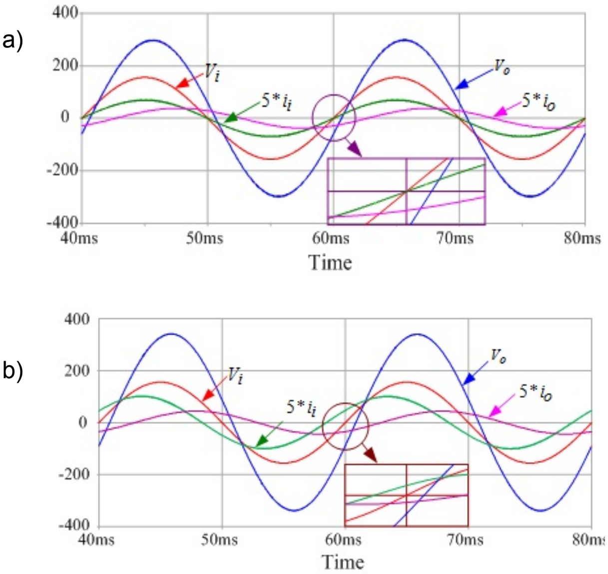

Fig.10. Wave forms of PWM boost AC chopper with optimal capacitor: (a) optimal capacitor $C = 60\,\mu F$ and (b) without optimal capacitor $C = 114\,\mu F$.

Based on the simulation results, the optimal capacitance value can produce the unity PF_i. However, it also affects the output voltage ripple. At low power of resistive load, high output voltage ripple will be appeared at the output side because of small capacitance value used. Assuming that the load power are 100 and 1000 W for buck topology, using the design step of the proposed method, the optimal capacitance values are calculated as $0.25\,\mu F$ and $25\,\mu F$ respectively. While, the minimum capacitance value used to meet the maximum voltage ripple is $6.46\,\mu F$ in case of 100 W. This causes the output voltage ripple is higher than the designed value as shown in Fig. 16a. However, when the load power increased at 1000 W the output voltage ripple is within designed value as shown in Fig. 16b.

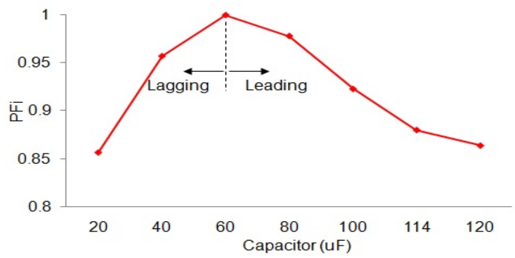

Fig.11. Input power factor versus capacitance of C (boost).

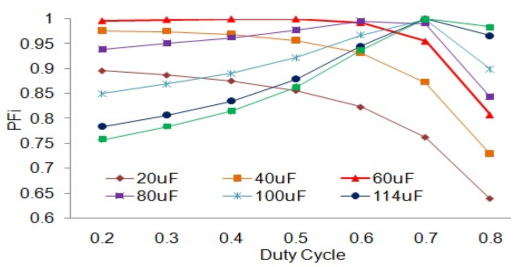

Fig.12. Input power factor versus duty cycle, D (boost type).

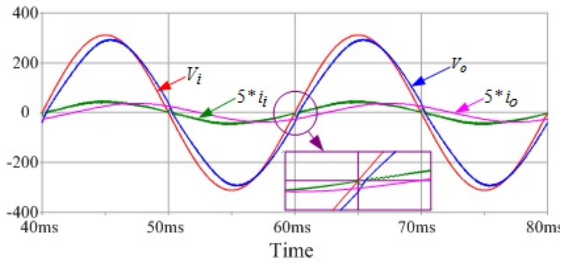

Fig.13. Wave forms of PWM buck-boost AC chopper with optimal capacitor.

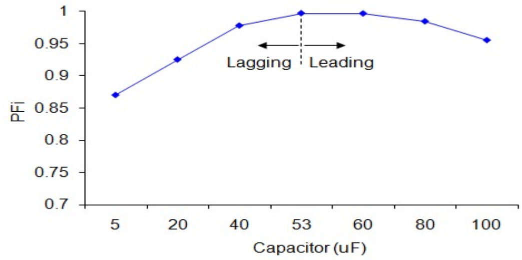

Fig.14. Input power factor versus capacitance of C (buck-boost).

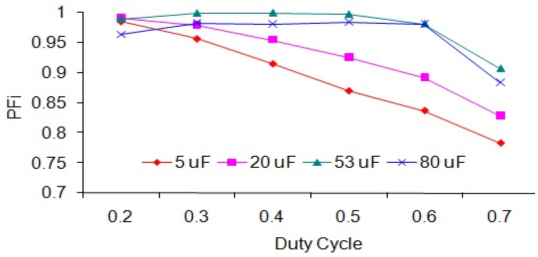

Fig.15. Input power factor versus duty cycle, D (buck-boost).

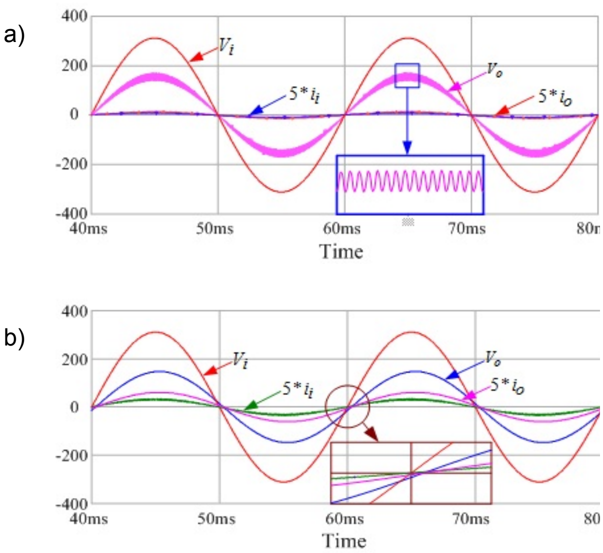

Fig.16. Wave forms of PWM buck AC chopper with optimal capacitor: (a) Load power 100 W and (b) Load power 1000 W.

Fig. 17 shows the output voltage ripple as a function of D at load power 100 and 1000 W, the optimal capacitance values are 0.25 and $25\,\mu F$ respectively. Their results indicate that the D affects the output voltage ripple. To reduce the output voltage ripple, the capacitance value should be increased. However, this causes the leading PF_i. Therefore, in designing the converter, the designer should consider the requirement of converter applications.

Some applications require low output voltage ripple, so the large capacitance value should be selected. Some applications are related PF_i so the optimal capacitance value should be used.

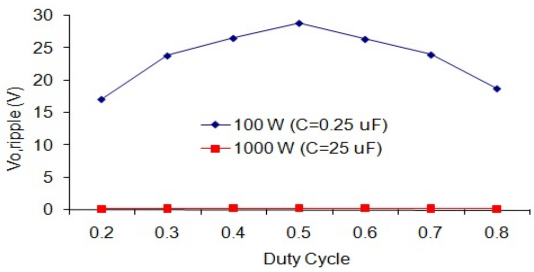

Fig.17. Output voltage ripple versus duty cycle, D.

Experiment

The experimental results of the PWM buck AC chopper topology is used to show the performance of the proposed technique. The power circuit of the experiment is shown in Fig. 1a. The system parameters used for experiment are as follows: $V_i = 110$ V, $f = 50$ Hz, $f_s = 20$ kHz, $C_f = 1$ μF, $L_f = 1.8$ mH, $D = 0.5$, $R_o = 50\,\Omega$ and $L_o = 220$ mH. Using the designed step of the proposed method, the values of filter inductance is 17.7 mH and the filter capacitance are 7.46 μF (selecting 8 μF) in case of resistive load and 32.09 μF (selecting 30 μF) in case of a resistive-inductive load (RL load). The implemented prototype in the laboratory is shown in Fig. 18.

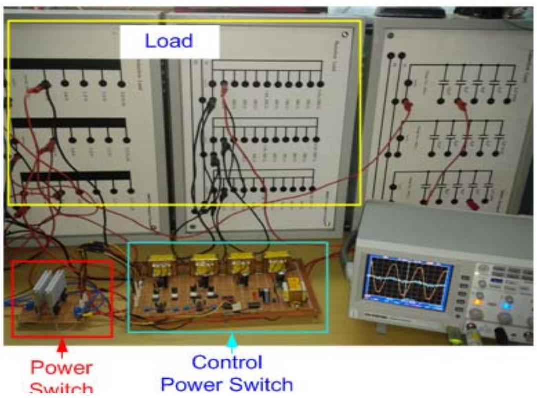

Fig.18. Experimental prototype.

Fig. 19 shows the simulation and experimental results in case of RL load. Fig. 19a and 19c show the waveforms of input current and input voltage. While, Fig. 19b and 19d show the waveforms of output current and output voltage. Fig. 20 shows the experimental results in case of resistive load where Fig. 20a shows the simulation results of load current, output voltage, input current and input voltage. While, Fig. 20b shows the experimental results of load current, output voltage, input current and input voltage of the experiment. According to the results, the experimental results are in consistent with the simulations. These results show that the phase angle of input current is in phase with that of input voltage source. Therefore, the power factor at supply side is nearly unity and the output voltage ripple is within the designed value.

a)

b)

c)

d)

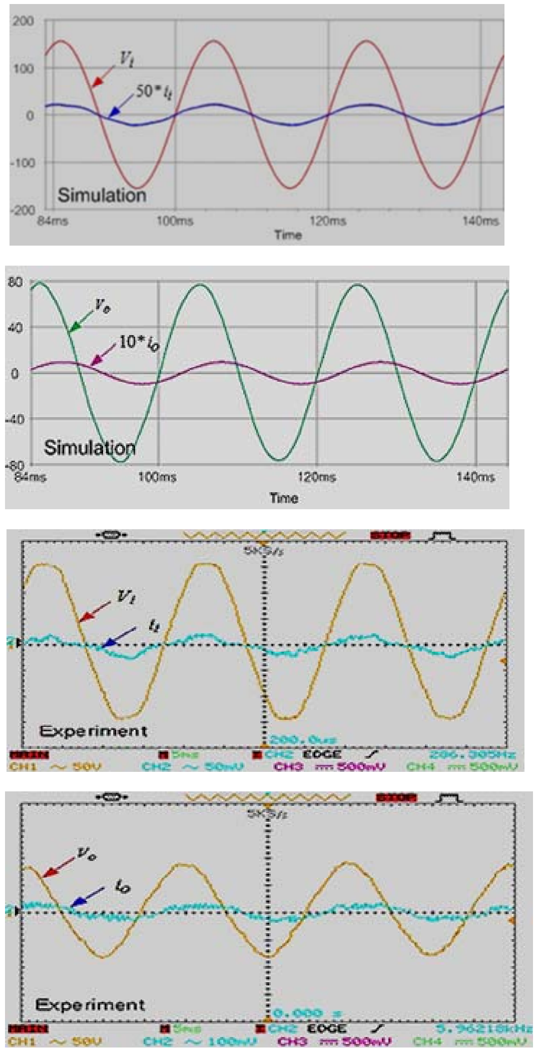

Fig.19. Simulation and experiment results of PWM buck AC chopper (RL load): (a), (c) waveforms of input current and voltage and (b), (d) waveforms of output current and voltage (voltage, 50 V/div,current, 50,100 mA/div, 5 ms/div).

a)

b)

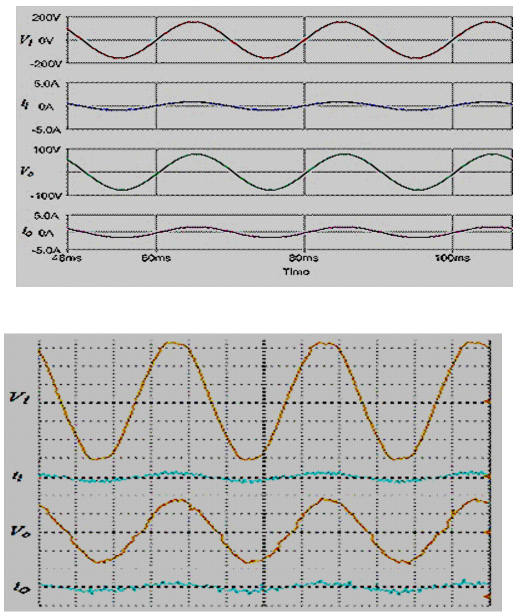

Fig.20. Waveforms of input current/voltage and output current/voltage (R load): (a) simulation results and (b) experiment results (voltage, 50 V/div, current, 500 mA/div, 5 ms/div).

Conclusion

In this paper, we proposed the new design technique to obtain the optimal value of the filter capacitance of PWM buck, boost and buck-boost AC chopper circuits for improving the input power factor. This results the phase angle of input current in phase with that of input voltage and the output voltage ripple within designed value. According the simulation and experimental results, we conclude that the filter capacitance value affects the performance of PWM AC chopper as follows:

1. The filter capacitance value affects the PF_i and output voltage ripple.
2. The optimal value of the filter capacitance can produce the unity PF_i.
3. If the filter capacitance value is lower or higher than the optimal value, it results leading or lagging PF_i.
4. The duty cycle little affects the PF_i if the optimal capacitance value is used.

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