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Low Offset, High PSRR, CMOS Bandgap Voltage Reference

Abstract. *A CMOS Bandgap Voltage Reference (BVR) with the characteristics of low offset and high power-supply rejection ratio (PSRR) is presented. In order to reduce the effect of offset of operation amplifier (OPA), the voltage difference of base-emitter junctions of substrate bipolar transistors is maximized; meanwhile the factor of offset voltage could be minimized. The feedback loop constructed by proportional to absolute temperature (PTAT) current source and an OPA is employed to improve the PSRR. The circuit was designed and simulated in a standard 0.35-μm CMOS process, with a power supply of 3 volt. The relative accuracy is increased by 5 times compared with conventional circuit. PSRR of the circuit is ～108dB at low-frequency. Furthermore, temperature coefficient (TC) of 17ppm/℃ over a wide temperature range of －40～115℃.The whole circuit including the OPA draws only 22 μA from supply voltage. Silicon area is 0.037mm2.*

Streszczenie. *Opisano pasmowy wzorzec napięcia w technologii CMOS charakteryzujący się małym pełzaniem zera i dużym współczynnikiem usuwania składowej zasilającej. Układ zaprojektowano w technologii 0.35μm z napięciem zasilania 3V. (**Pasmowy wzorzec napięcia z małym pełzaniem zera i dużym współczynnikiem PSRR**)*

Keywords: Offset, PSRR, CMOS, Bandgap voltage reference, PTAT.
Słowa kluczowe: wzorzec napięcia, technologia CMOS

Introduction

Bandgap voltage references are basic functional circuit blocks that provide a temperature and supply insensitive output voltage. High precision voltage references are widely used in many integrated circuit (IC) chips, such as, power management, temperature sensors, dynamic random access memory (DRAM), flash memories, analog-to-digital converters (ADCs), and digital-to-analog converters (DACs).

Bandgap voltage references are required to be stabilized over temperature variations, process, and supply voltage. Traditionally, bandgap voltage reference, with low temperature sensitivity is generally obtained as the sum of a voltage that is proportional to absolute temperature (PTAT) and a voltage with negative temperature coefficient, which is complementary to absolute temperature (CTAT) [1].The PTAT voltage is the voltage difference of two base-emitter junctions of substrate bipolar transistors. The CTAT voltage is usually obtained from the voltage across a forward biased p-n junction or the base-emitter voltage (V_{BE}) of a diode connected bipolar junction transistor (BJT) as illustrated in Fig.1.The term V_T indicated in this figure is the thermal voltage and equal of kT/q, where k is the Boltzmann constant, T is the Kelvin temperature and q is the electron charge.

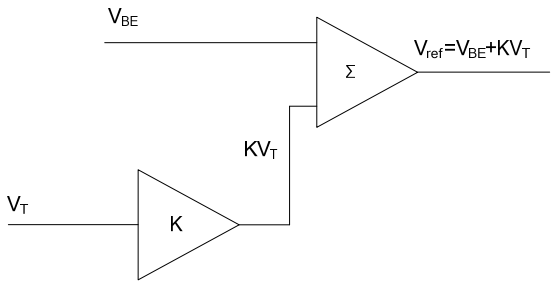

Fig.1. Block diagram of a BVR

In addition to temperature variations, the accuracy of Bandgap voltage is affected by OPA offset. Offset results from the inherent random offset in MOSFETs transistors gate source voltages which arises from the mismatches in threshold voltages, W/L ratios, and electron and hole mobility [2]. Several techniques for low offset could be found in the literatures or books [3, 4].The supply noise injected to the output of Bandgap reference circuit also significantly influence the accuracy of Bandgap voltage. Much work on improving PSRR has been done in [5, 6].

In Sect.2-5, the proposed design methodology and circuit implementation are presented. Layout design and simulation results are discussed in Sect.6 and conclusions are explained in Sect.7.

Conventional CMOS Bandgap Voltage Reference

The core of a Conventional BVR circuit is shown in Fig.2. It is assumed that the offset voltage is V_{OS}, according to the feedback principle of the amplifier, the voltages at the nodes X and Y are equal, so the current of I_2 is $(\Delta V_{EB} + V_{OS})/R_1$, The current of I_3 is mirrored from M_2, hence the output voltage will be:

$$V_{ref} = V_{EB3} + M \cdot \frac{R_2}{R_1}[\Delta V_{EB} + V_{OS}] \quad (1)$$

where M is a constant, V_{EB3} is a CTAT voltage, ΔV_{EB} is (V_{EB1}-V_{EB2}) equal to $V_T \ln N$, V_T is a PTAT voltage. By proper choosing the value of M, R_2/R_1, and N, the Bandgap output voltage with zero temperature coefficients can be achieved in a specified temperature of T_0.

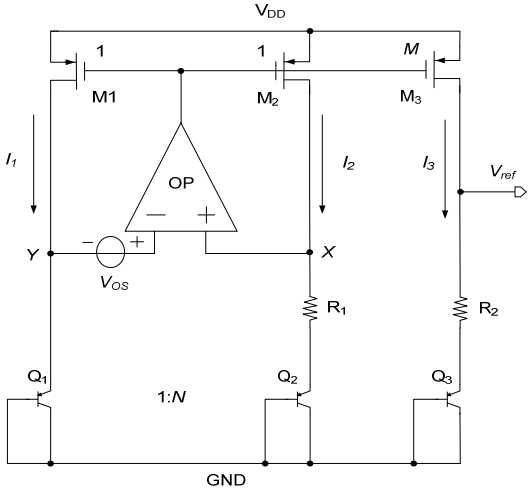

Fig.2. The conventional BVR with offset

However the offset voltage V_{OS} is amplified by a factor $M \cdot R_2/R_1$.As a result the reference voltage precision may be affected, especially in CMOS process [7].Therefore, the OPA offset voltage is the prevailing source of process induced error in CMOS BVR architecture similar to Fig.2.

The method to reduce the effect of offset is setting the ratio of collector current densities of Q_1 and Q_2 is M and stacking another two bipolar transistors above Q_1 and Q_2 respectively[1].Thus the Bandgap reference V_{ref} with offset will be:

$$V_{ref} = 2V_{EB} + M \cdot \frac{R_2}{R_1}[2V_T ln(P \cdot N) + V_{OS}] \tag{2}$$

The effect of offset can be reduced as factor $M \cdot R_2/R_1$ has been degraded. However the problem is the output of V_{ref} is about 2.5V, it is difficult to produce such a voltage in low supply voltage environment.

Improved CMOS Bandgap Core

Based on equation (1), if the factor ΔV_{EB} is maximized, then the offset voltage V_{OS} could be minimized, the Vref with least effect of offset will be acquired.

Fig 3 shows the Bandgap Core circuit of the low offset Bandgap reference. OPA A_V, PMOS transistor M_1 and M_3 comprise one feedback loop to force the voltages at the inverting and non-inverting inputs of AV equal. Another feedback loop is composed of OPA A_V, PMOS transistor M_2, BJT Q_1, Q_2, Q_3 and Q_4 and impedance R_1, R_2, R_3 and R_4, this loop outputs reference voltage and keep the output stabilize.

As the stacked BJT Q_1, Q_3 and Q_2, Q_4 have different emitter areas, a PTAT voltage about $2\Delta V_{EB}$ is provided. From Fig.3 given

$$\left(\frac{W}{L}\right)_{M_2} = \alpha \cdot \left(\frac{W}{L}\right)_{M_1} = \alpha \cdot \left(\frac{W}{L}\right)_{M_3} \tag{3}$$

where α is a constant. Then

$$V_Y = V_{EB1} + I_{B1}R_4 + V_{EB3} \tag{4}$$

$$V_X = V_{EB2} + (I_{B2} + I_2) \cdot R_3 + V_{EB4} \tag{5}$$

$$I_{B1} = I_{B2} = \frac{I_1 + I_2}{\alpha \cdot \beta} \tag{6}$$

In which, β is the current gain of BJT Q_1, Q_2, Q_3 and Q_4,V_Y and V_X are respectively the voltages of OPA A_V inverting input and non-inverting input. I_{B1} and I_{B2} is respectively the base current of BJT Q_1 and Q_2, I_1 is the current across impedance R_1; I_2 is the current across impedance R_2. Indeed, since in Fig.3 $V_X = V_Y$, then

$$I_2 = \frac{\Delta V_{EB12} + \Delta V_{EB34}}{R_3} = \frac{2\Delta V_{EB}}{R_3} \tag{7}$$

$$\begin{aligned} V_{ref} &= V_{EB4} + (R_2 + R_3) \cdot I_2 \\ &= V_{EB4} + 2\lambda \Delta V_{EB} \end{aligned} \tag{8}$$

Where λ=(1+ R_2/R_3).Under the situation of considering offset of OPA, the voltage of output of is expressed as

$$V_{ref} = V_{EB4} + 2\lambda \Delta V_{EB} + \lambda V_{OS} \tag{9}$$

It is noticed that in the above equations the effect of current I_{B1} and I_{B2} are not considered because of large values of α and β.Compared with equation (2), in equation (9) the factor of λ could is a smaller value, and the effect of offset of OPA has been reduced significantly. The Bandgap reference voltage is directly outputted from the feedback loop, in which the mismatch of current mirror is avoided.

To minimize the amplifier offset, the size of transistors must be selected large enough to reduce its offset below an acceptable value [8].

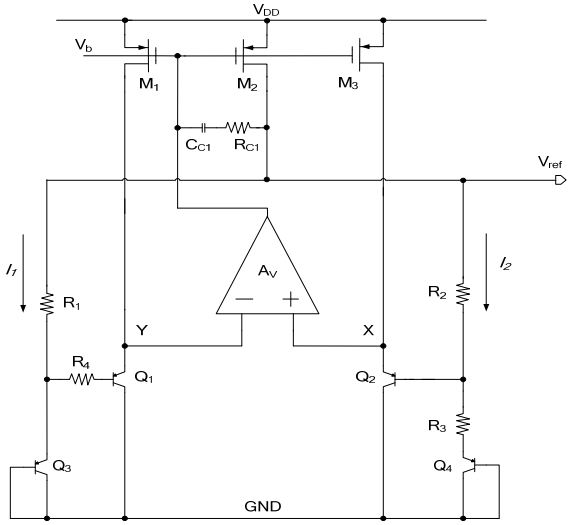

Fig.3. Improved CMOS Bandgap Core

Start-up circuit and Buffer circuit

The Start-up circuit used in this design shown in Fig.4.The start-up circuit operates as following: if the current in the p-channel current sources M_1, M_2, M_3, and M_4 is zero, The gate of M_{S1} is then pulled down to ground, hence injecting a current into M_{S4} to make M_{S3} turn on, and then the gate of M_1, M_2, M_3, and M_4 is pulled down to ground. Once the circuit starts up, current in M_{S2} and M_{S5} will cause the gate potential of M_{S4} to decrease and approach GND, which, in turn, turns off the startup circuit.

The Bandgap voltage output has fairly high impedance. Thus, it needs to be buffered for further use. The Buffer circuit is composed of M_{B1}～M_{B8}, impedance R_{C2}, R_5 and R_6,capacitance C_{C2} and C_O. R_5 and C_O constitute a low pass filter. The filter isolates capacitance load and feedback loop meanwhile improves the power supply rejection ratio of the circuit at the outside of low pass filter bandwidth. The output voltage of buffer circuit $V_O = V_{ref} \cdot R_6/(R_5+R_6)$.Based on the resistive division technique, a fraction of the Bandgap voltage is obtained by proper choice of resistors R_5 and R_6.

High PSRR Mechanism

For the Bandgap Core circuit shown in Fig.4, High PSRR is obtained by applying these strategies:

1. The feedback loop including OPA, M_2, BJT Q_1, Q_2, Q_3 and Q_4 is applied. The higher the loop gain, the higher will be the rejection of the variations in the main power supply. A large open-loop gain of the OPA will improve PSRR performance of BGR circuit. According to what was mentioned above, a simple low voltage amplifier with NMOS input transistors was design for OPA. The designed amplifier is cascade structure, as shown in Fig.4. The amplifier is comprised of M_7～M_{15}.

2. In order to suppress the effect of variation on tail current source M_7, the current generated by Bandgap reference core circuit itself is used to bias the OPA block in this design. Stimulation study shows that using self-biasing scheme, the PSRR can be reduced by 20dB, compared to the Bandgap reference circuit with the OPA biased traditionally [9].

3. As shown in Buffer circuit, RC low pass filter composed by R_5 and C_O also improved PSRR performance.

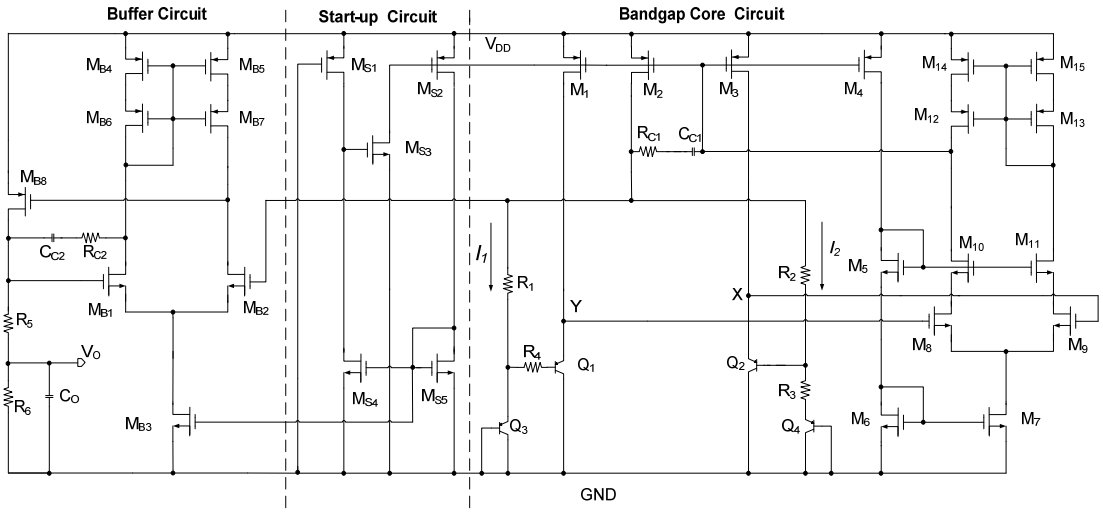

Fig.4. Bandgap Voltage Reference circuit

Layout design and experimental results

Fig.5 shows the microphotograph of the whole Bandgap voltage reference circuit and silicon area is 0.037mm^2.It is known that mismatches of resistors, current mirror and bipolar transistors may seriously affect its performances [10]. In order to minimize mismatches, a group of parallel resistors with identical geometries are used. Current mirror and bipolar transistors are respectively in symmetrical array.

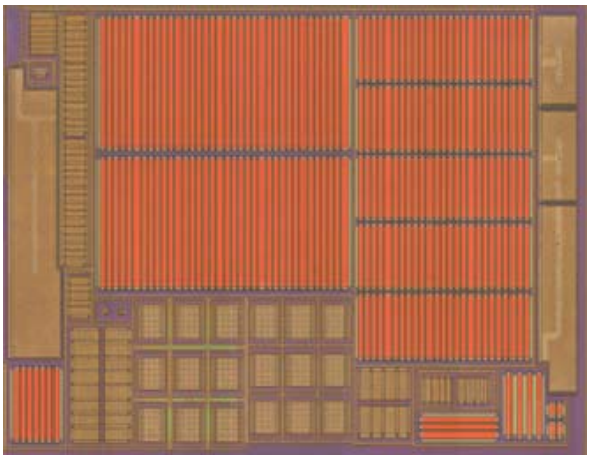

Fig.5. Microphotograph of the BVR

The parasitic parameters of the BVR layout are extracted, and simulation based on standard 0.35-μm CMOS process has been carried out. Fig.6 shows the curve of Bandgap voltage reference versus temperature characteristics over the range from －40～115℃,it can be seen that the peak-to peak variation is 1.38mV,the temperature coefficient (TC) 17ppm/℃. The PSRR of the BVR versus frequency is shown in Fig.7. The PSRR is -108dB at a low frequency of less than 100Hz. Table.1 summarizes the performances of the BVR.

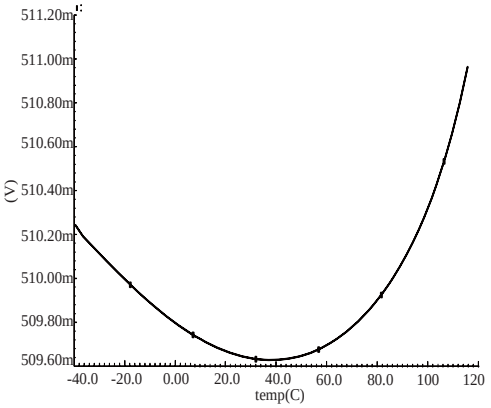

Fig.6. Output reference VO versus temperature

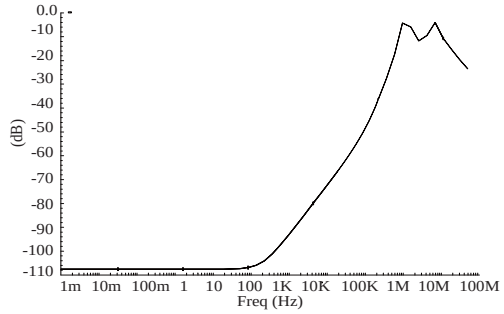

Fig.7. Output reference PSRR versus frequency

In order to observe the effect to restrain offset voltage of improved BVR. Given the stochastic error of current mirror and different pair aroused by arts is ±2％.The simulation results of improved circuit and conventional circuit is contrasted in Table.2. The error of output voltage in Conventional circuit is not less than 26.69mV. However, it is only 5.4mV in improved BVR. The relative accuracy is increased by 5 times compared with conventional circuit; the result shows improved circuit significantly restrains the effect of offset voltage.

Table.1 Summery of performances of BVR

Parameter	Supply voltage	Power dissipation	Area	TC	PSRR@DC	PSRR@100K
Value	3V	66μW	0.037mm^2	17ppm/℃	108dB	55dB

Table.2 Influence of various mismatches for output voltage

	Conventional circuit		Improved circuit	
Error item	-2%	+2%	-2%	+2%
Current mirror	-13.003mV (-1.69%)	+0.533 mV (+0.07%)	+2.5 mV (+0.49%)	-2.8 mV (-0.55%)
Different pair	+0.128 mV (+0.17%)	+13.683 mV (+1.78%)	-2.9 mV (-0.57%)	+2.3 mV (+0.45%)

Conclusion

This paper has presented a low offset and high PSRR Bandgap voltage reference, which generates an output voltage of 510mV.The circuit features PN in series and appropriate layout to achieve low offset, in addition, feedback loop, self-biased OPA and RC low pass filter for high PSRR. Stimulation result shows that the BVR circuit achieved the reported high PSRR of -108dB at low frequency. Furthermore, TC of 17ppm/℃ over a wide temperature range of －40～115℃.The whole BVR circuit occupies 0.037mm^2 silicon areas, and consumes 22μA current. It can be used in many applications such as lighting and ballast ICs [11-14].

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