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The Research on Effect of Zero Order Holder and First-order Lag to High Performance Digital Arc-welding Power Supply

Abstract. *Digital control become more attractive because of their stable control precision and flexible control strategy in welding occasions. In this paper, the impact of zero order holder and first-order lag to system performance is analyzed firstly and it is conclude that zero order holder and first-order lag will reduce the stability of the system. Also, the trend of stability will change with damp PF-FB power supply in both voltage loop control and current loop control. Based on those conclusion, the control parameters are set based on unload state when the system in voltage loop and short-circuit state in current loop, it maximally improves the system steady and dynamic performance, especially, it reduces the excessive short-circuit current. Simulation and experiment verifies the results.*

Streszczenie. *W artykule wykazano, że podtrzymanie zerowego rzędu i opóźnienie pierwszego rzędu ograniczają stabilność układu. Bazując na tym założeniu określono parametry układu sterowania w stanie nieobciążonym oraz właściwości statyczne i dynamiczne, szczególnie w celu redukcji dodatkowego prądu zwarcia. (**Badania wpływu podtrzymania zerowego rzędu i opóźnienia pierwszego rzędu na układ cyfrowego zasilania systemu spawania łukowego**)*

Key words: Arc-welding; Zero order holder; First-order lag; Short-circuit current
Słowa kluczowe: spawanie łukowe, prąd zwarcia, system zasiilania

Introduction

The arm of inverter model arc-welding power supply control system design is to obtain the required outer characteristic, adjustment characteristic and dynamic characteristics through the current and voltage feedback loop adjustment [1]. With the super-scale integrated circuit technology development and the microprocessor performance improvement, cost price decline, power device of switch model with full digital control is increasing, the analog control has gradually replaced by digital control. However, at the same time, there are some special problems in digital control system due to the limited development of microprocessors, such as the error produced in sampling and quantization process, which shortens the performance of the system, the digital processor sampling and calculation delay, which constrains maximum duty cycle, and the digital realization of traditional analog control scheme inferior to analog control, these problems have hampered the digital control performance improvement in power supply [2].

Digital sampling, zero order and first-order lag to the effect of the controlled objects in digital inverter power supply have been researched in some literatures [3][4][5], however, there is not further discussion about it in the phase shift full bridge (PS-FB) power supply.

This paper analyzes the main reason of system performance decline in digital process in arc-weld cutting power supply. The system control parameter is designed based on unload state when the system working in voltage loop and short-circuit state when system working in current loop, and the system performance is improved by pole-zero assignment. The simulation and experiment both verify that the dynamic characteristic and steady characteristic meet the arc-welding power supply requirement well.

The analysis of the effect of digital control on system performance

A. The effect of Zero order holder to PS-FB system performance

The main topology of arc-welding power supply is showed as Fig. 1 and the equivalent circuit frame of digital FS-FB closed loop system is showed as Fig.2.

The transfer function of duty cycle to output voltage for PS-FB in continuous field is:

$$(1)\quad G_{vd}(d)=NV_i\frac{R}{LCRs^2+(R_dRC+L)s+R_d+R}=NV_i\cdot k_L\cdot\frac{\omega_n^2}{s^2+2\zeta s+\omega_n^2}$$

where, $\omega_n=\sqrt{(R+R_d)/(LCR)}$, $\xi=(R_dRC+L)/(2LCR\omega_n)$, $k_L=1/(R+R_d)$

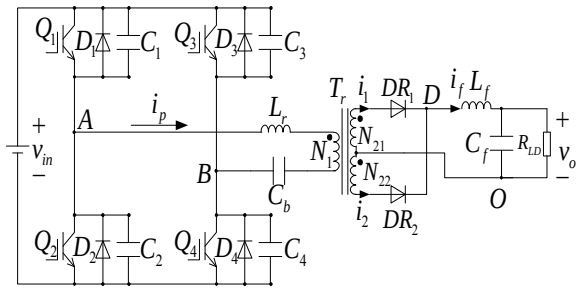


Fig.1. Main topological of arc-welding power

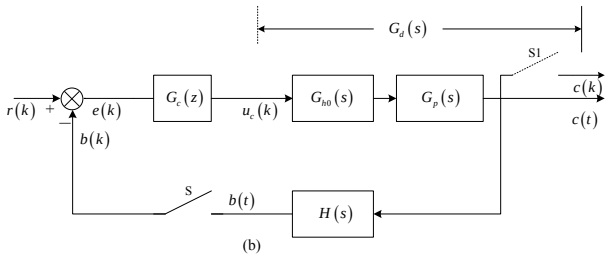


Fig.2. Equivalent circuit frame of digital FS-FB closed loop system

The transfer function of duty cycle to output voltage for PS-FB in continuous field is:

$$(2)\quad G_{id}(d)=NV_i\frac{1}{LCRs^2+(R_dRC+L)s+R_d+R}=NV_i\cdot k_L\cdot\frac{\omega_n^2}{s^2+2\xi s+\omega_n^2}$$

Where $\omega_n=\sqrt{(R+R_d)/(LCR)}$, $\xi=(R_dRC+L)/(2LCR\omega_n)$, $k_L=1/(R+R_d)$

In formula (1) and (2), it is obvious that the output voltage and output current mathematic models could be both equivalent to typical two-order system, which promises a way to analysis and design based on typical two-order system.

In Fig. 2, the factor Gh0 (s) is inserted into the loop due to the zero-holder import, which is equivalent as the change of control object from Gp(s)→ Gh0 (s) Gp(s). Then the z field model after discretization is:

(3) $$G_d(z) = (1-z^{-1})Z(\frac{G_p(s)}{s}) = (1-z^{-1})Z(\frac{1}{s}\cdot k_b k_L \frac{\omega_n^2}{s^2+2\xi\omega_n s+\omega_n^2})$$

Assume the poles of the control object is S1,2, so s2+2ξωn+ωn 2=(s-s1)(s-s2), then

(4)

$$G_d(z)=k_b k_L \frac{\omega_n^2}{s_1 s_2(s_1-s_2)}\cdot\frac{(s-s_1)(z-e^{s_1T})(z-e^{s_2T})+s_2(z-1)(z-e^{s_2T})-s_1(z-1)(z-e^{s_1T})}{(z-e^{s_1T})(z-e^{s_2T})}$$

$$=\frac{c_1 z+c_2}{z^2+b_1 z+b_2}$$

Where, b1,b2,c1, c2 is the function of s1,s2,T,k. The continuous model of PS-FB will increase one zero due to the zero-holder import and the transfer function of the system is not only relevant with the system parameters but also the sampling cycle.

The closed loop characteristic equation of closed loop transfer function as Fig. 2 is:

(5) $$1+G_c(z)\cdot Z\left[G_h(s)G_p(s)H(s)\right]=0$$

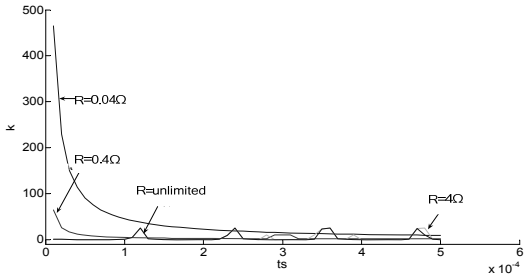
To simplify the analysis, the proportion controller simplified most to inspect the effect of zero order-holder to open loop gain in system stability zone. Hence, we set Gc(s)=k, H(s)=1 and the control object is used as normalized unit model, set kb =1 to make sure the effect from the change of dc input voltage Ud and feedback coefficient H（s）could be corrected as the change of open loop gain. kL is not normalized based on the consideration of voltage loop and current loop stability. [6]

The corresponding closed loop characteristic equation is:

(6) $$1+k\cdot k_L\cdot G_d'(z)=0$$

The trend of stability will change with damp PF-FB power supply. The effect of sampling cycle to voltage loop control and current loop control stability when the load changing is showed in Fig. 3.

a)



b)

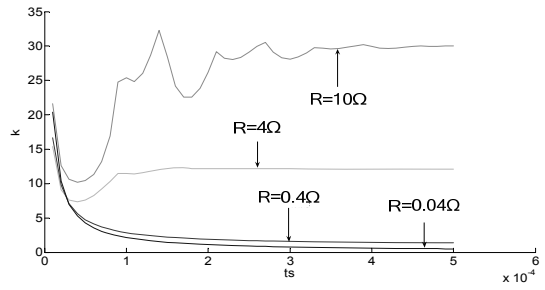
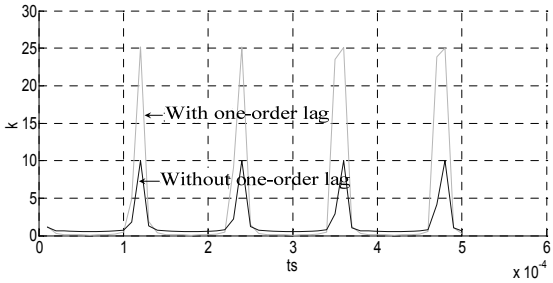


Fig.3. The effect of zero order holder to FS-FB stability: (a) voltage loop control; (b) current loop control

In Fig. 3, the relationship between the PS-FB stability and load is: the trend of stability changes with the sampling cycle under different PF-FB loads. In voltage loop control as Fig. 3(a), when the system load is infinite, the critical open loop gain is surging at ωn with sampling cycle increase, and when the frequency points of nωn, the open loop peak appears, when the frequency is not at the points of nωn, the open loop gain is 0. As the load decline, the open loop gain attenuates monotonously to 1 with sampling cycle increase. There is less minimum stability zone with the load increase. Contrarily, there is larger minimum stability zone with the load decline, and there is larger stability zone at high sampling frequency. In current loop control as Fig. 3(b), when the load is large the critical open loop gain of the system is damped oscillation at the cycle of ωn, and stabilizes to fixation finally; when the load is small, the critical open loop gain of the system attenuates monotonously and stabilizes to fixation finally.

a)



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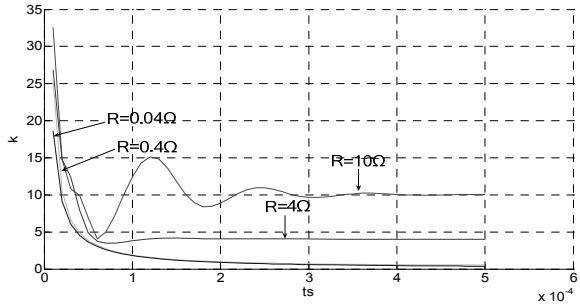

Fig. 4 . The effect of first-order lag to system performance: (a) the effect of first-order lag to system in voltage loop; (b) the effect of first-order lag to system in current loop.

B. The effect of first-order lag to the PS-FB system performance

First-order lag control is equivalent as the delay unit imported to the control object:

(7) $$G_h(z)=\frac{1}{z}$$

The closed characteristic equation is:

(8) $$z+G_c(z)\cdot Z\left[G_h(s)G_p(s)H(s)\right]=0$$

The analysis method is the same to the zero order holder, we use proportion adjustor and unit feedback to inspect the effect of first-order lag to stability zone of open loop gain. From the formula (8), the system stability condition is Figured out. The curves of critical open loop gain of the closed loop system changing with sampling cycle variation when the parameters changing is showed in Fig. 4.

In Fig. 4, when the system is in the unload voltage loop, k is surging at the ωd with T increase, and achieves the maximum in nTd (n=1,2v…) during one period. And the stability zone of the system with the first-order lag is reduced compared to the system without the first-lag. For the system working in load current loop, if the sampling frequency is lower than some fixed value, K will increase with the load

increase and it will stabilize finally. And when the load is small, the critical open loop gain will attenuate monotonously and the system will stabilize finally.

In summary, high frequency sampling system stability zone will increase with the decline of the load because the PS-FB power supply works in the under-damping unload state. So the design of voltage loop needs to be based on unload state.

Under the same sampling frequency, when the load changes, the stability will become less with the load decline. So the design of current loop needs to be based on minimum load.

Design of current loop & voltage loop

In this paper, the parameters of PF-FB arc-welding power supply is showed in table1.

Table .1 System Parameters

Parameters	Value
Filter inductor L	0.09mH
Filter capacitor C	4uF
Number of turns N	4:13
Input voltage V_{in}	540V
Equivalent resistance of arc	0.373 Ω
Equivalent resistance of short circuit	0.04 Ω

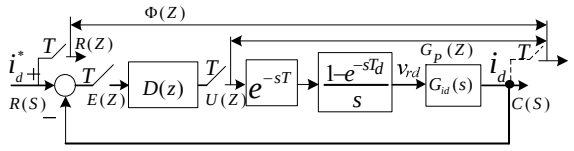

Fig .5. The current loop model with zero order holder and first-order lag imported calibration unit

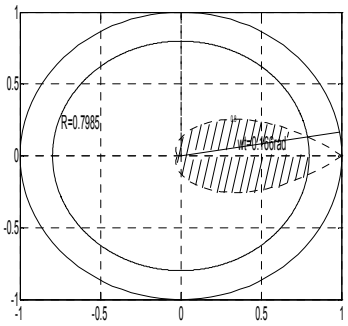

Fig .6. Characteristic root rang to stable performance system

The transfer function G_{id} of duty cycle d to output current i_o is shown as formula (2).

The bode diagram of arc-welding power supply with zero order holder and first-order lag is showed in Fig. 5. In Fig. 5(a), the amplitude-frequency curve moves up and the phase-frequency move down. The frequency characteristic of arc-welding power transfer function changes with the load. If the control transfer function design is based on normal load, the open loop system phase margin would reduce with the load decline. Conversely, if the control transfer function design is based on small load, the damp coefficient would be too large for arc-welding power supply in the most work cases, leading to a long time for the dynamic transition process. So, if the current loop is designed based on short-circuit state, the system would have little overshoot and fine speediness. At the arc-burning time, the load resistance increase, and the stability zone increase; the phase margin increase, the damp coefficient increases, which contributes to the arc-burning. In Fig. 6, the conclusion is drawn as follows: (1) The amplitude-frequency characteristic changes little in three cases. (2) The phase-frequency characteristic changes little in the lower frequency zone(<1kHZ). (3)Zero order holder leads delay to system in the middle frequency zone, even to be unstable, and first-order lag leads more weak performance to the system. So it needs to be digital calibration in discrete field. [8][9].

A .The current loop design

The current loop model with zero order holder and first-order lag imported calibration unit is showed as Fig. 5. System open loop transfer function is:

$$G_i(z)=\frac{1}{z}*(1-\frac{1}{z})Z(\frac{1}{s}*\frac{NV_i/R}{s^2LC+s(L/R+R_dC)+R_d/R+1}) \tag{9}$$
$$=\frac{84.15z+0.2464}{z(z^2-0.8335z+9.254\times10^{-17})}$$

By zero-pole eliminate, the system characteristics equation is:

$$\Delta(z)=z^3-z^2+84.15(K_P+K_IT)z \tag{10}$$
$$+0.2464(K_P+K_IT)=0$$

The sum of the characteristic root is 1 according to vida theorem, a zero characteristic root is placed for the overshoot requirement.

According to Fig. 6, the three roots is placed: 0,0.5+j0.084,0.5-j0.084,so Kp=0.00254 and Ki=10.174. The unit response curve is showed as Fig. 7. σ%=1.5%,ts=0.5ms.It meets the requirement well.

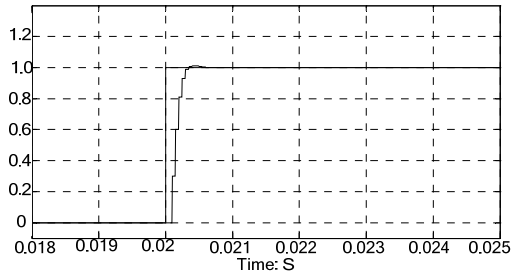

Fig. 7. Unit response in current loop

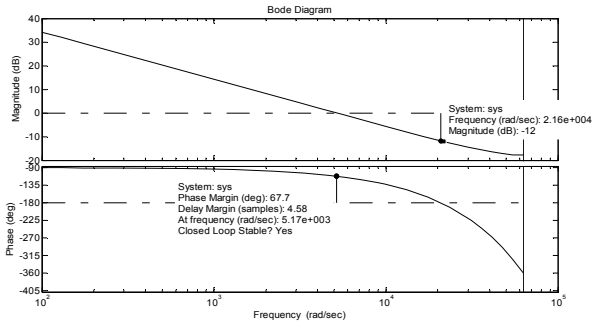

Fig.8. Bode diagram after calibration

The bode diagram after calibration according to the requirement parameters is showed as Fig. 8. It is seen that the closed loop system is stable. The phase margin is 66.7 degree and the amplitude margin is 12db.

The maximum work resistance is R=0.373Ω.The bode diagram is Figured out with resistance variation in Fig. 9. In Fig. 9, it is seen that the system phase margin increases, the

amplitude margin never change, the stabilization bound is wider. In words, it satisfies the load variation in welding occasion.

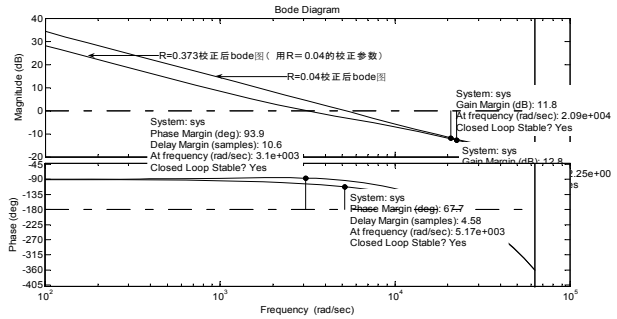

Fig .9. Bode diagram with resistance variation

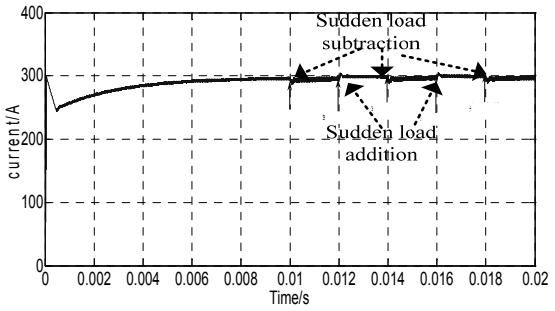

Fig. 10. The simulation sudden addition and subtraction

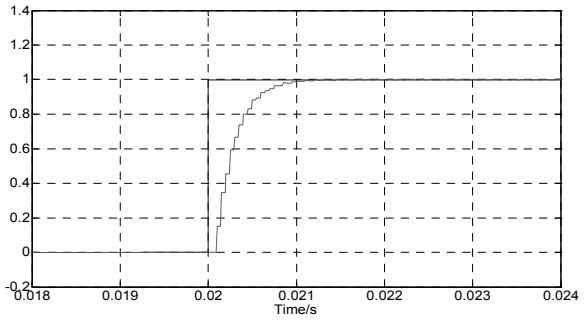

Fig.11. Unit response in voltage loop

The simulation sudden addition and subtraction load between 0.04Ωand 0.0106Ω in 300A output current is showed in Fig. 10.

In Fig. 10, it is seen that the output current can stabilize in 200us in the sudden addition and subtraction load. The dynamic performance is fine. In this situation, the gain declines, so the stability errors increase.

B. The Voltage loop design

The transfer function Gvd (s) of $\hat{d}(s)$ to $\hat{v}_o(s)$ is:

(11)
$$G_{vd} = \frac{NV_i}{s^2LC + s(\frac{L}{R} + R_dC) + \frac{R_d}{R} + 1}$$

In voltage loop, R=∞.

(12)
$$G_{vd} = \frac{NV_i}{s^2LC + sR_dC + 1}$$

(13)
$$G_{vd}(s) = \frac{NV_i}{s^2LC + sR_dC + 1} = NV_i \cdot k_L \cdot \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

where， $\omega_n = \sqrt{1/LC}$, $\xi = R_d/2L\omega_n$, $k_L = 1$.

The same to the current loop design, the unit feedback of PI adjustor to inspect the effect of first-order lag to open loop gain stability zone is adopted, the parameters: Kp=0.0002, Ki=20.24 are derived under unload condition. The unit response curve is showed in Fig. 11. In Fig. 11,σ%=1%,ts=1.4ms.It meets the requirement well.

Experimental results

The startup voltage waveform at unload is showed in Fig. 12, the peak-peak value is 400mv.the voltage waveform after the interrupt to voltage loop (input voltage power off for 800ms) is showed in Fig.13. It is seen that the voltage can stabilize quickly.

The transition waveform from voltage loop to current loop at resistance load is showed in Fig. 14. It is seen that the voltage waveform is steady in voltage loop, at the transition into current loop, no overshoot current occurs and the track error is small. All the process takes about 1.5ms for the fine dynamic performance. The unload-short circuit-load current waveform in the weld occasion is showed in Fig.15, the weld current is 100A (current sampling proportion 0.0015V/A), but the short-circuit current is only 180A.The short-circuit current rise speed is moderate. The moderate short-circuit current not only avoid big splash but also make sure short-circuit fluid bridge transiting successfully, which promise perfect weld quality.

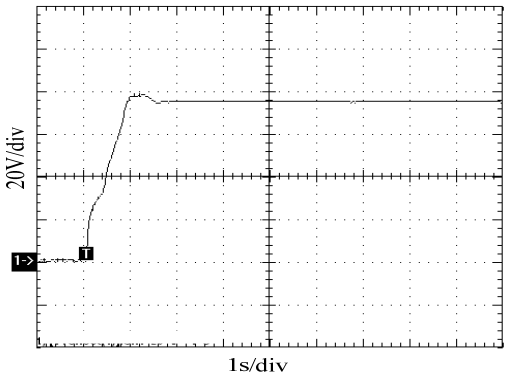

Fig.12. Unload voltage waveform in voltage loop

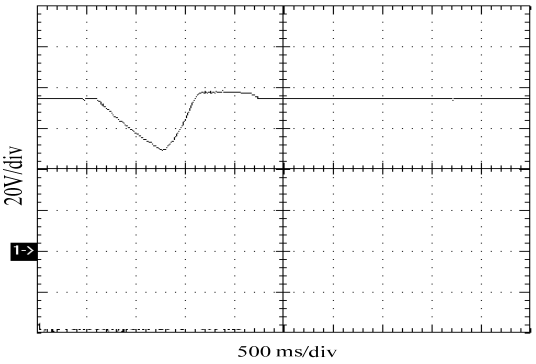

Fig.13.The voltage interrupted waveform in voltage loop

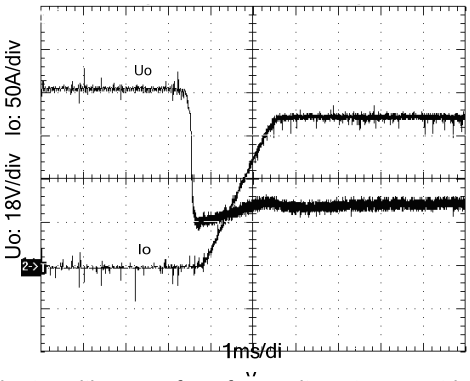

Fig.14. The transition waveform from voltage to current loop when resistance load

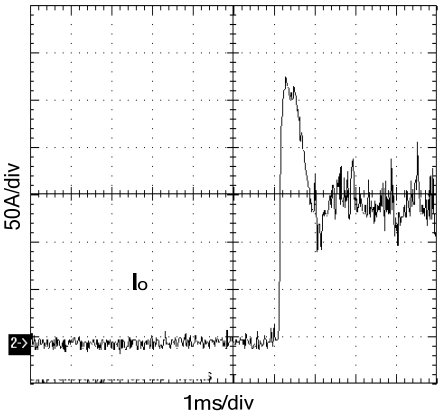

Fig.15. The transition of unload---short circuit----load current when welding

Conclusion

The effect of digital sampling, zero order holder and first-order lag to PS-FB is:

(1)zero order holder alters the open loop frequency characteristic of the power supply, leading to the damp of under-damping system oscillating periodically with the sampling cycle variation, and the damp of over-damping system attenuating monotonously with the sampling cycle variation; (2)the main effect of sampling cycle to frequency characteristic is enlarging the phase delay, which alters the closed loop system stability but do little to margin character;(3)first-order lag alters the closed loop system stability of PS-FB power supply, and the effect to the trend of stability changes with sampling frequency.

To meet the dynamic and steady performance, it is practicable to design control parameter based on unload state in voltage loop and short-circuit state in current loop. It is difficulty to meet the system performance by the control with zero order holder and first-order lag ,and the method of pole-zero placement can improve the system steady and dynamic performance, especially for overshoot, which promises short-circuit current loop controlled well in the process of weld short-circuit.

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