Vedat KIRAY, Meirambek K. ZHAPAROV

Turgut Ozal University, Suleyman Demirel University

FPGA Based Digital Electronic Education, Clock-Calendar Design

Abstract. *The clock calendar design is a case study produced in a project called FPGA based Digital Electronic Education Project (FPGA_b_deep.) The aim of the project is to develop case studies named "instructive and attractive examples" for Project Based Learning (PBL) to obtain high performance at Digital Design Education for electronics/computer engineering students or new digital circuit designers. The clock-calendar Design is second one from the instructive and attractive examples series and it is aimed students to enhance their skills of using counter, multiplexer, comparator and decoder while completing this design. The design of the clock calendar is completed considering the level of students and tested, then divided into three main blocks considering the criteria towards education. Graphic design is preferred for better understanding instead the design with HDL.*

Streszczenie. *W artykule opisano proponowane zajęcia projektowe dla studentów elektroniki i inżynierii komputerowej. Zadanie polega na zaprojektowaniu zegarka i kalendarza z wykorzystaniem układu FPGA. Projekt ma na celu zaznajomienie uczestników zajęć z zagadnieniami projektowania układów logicznych. W projekcie wykorzystywany jest tryb schematyczny. (**Nauka elektroniki cyfrowej z wykorzystaniem układu FPGA – projektowanie układu zegarka i kalendarza**).*

Keywords: Digital Electronics**,** FPGA, Calculator, Engineering Education, PBL.
Słowa kluczowe: elektronika cyfrowa, FPGA, kalkulator, edukacja inżynierska, PBL.

Introduction

FPGAs (Field Programmable Gate Arrays) have become one of the most useful devices of design laboratories due to the specialty of reconfiguration and free service of the design simulator programs. Therefore, they have a special place in teaching electronics engineering. Nowadays, in addition to engineering application, FPGAs are widely used as an education material by many Electronics and Computer Engineering Departments at universities in all over the world. In the first several years of FPGA technology, its educational usage was limited with several studies. Some of them are given at reference part [1-7]. After that, lots of study was presented about FPGA usage at electronics courses as an education material. Especially those researchers who work on project based learning (PBL) found FPGAs as very useful education devices. One of them was from Rey Juan Carlos University, Madrid, Spain. Researchers from that university studied on Project Based Learning Experience in VHDL Digital Electronic Circuit Design [8]. This study can be accepted as the most similar study to our study. FPGA_b_DEEP aims also to get high performance at Digital Design courses by using FPGAs but differences from the study mentioned above are that FPGA_b_DEEP focus on developing case studies (instructive and attractive examples) such as clock-calendar, calculator, and basic CPU design. At the PBL applications, it is important to divide projects in the proper steps in term of better understanding and suitability to team studies. In the same way, the special examples are divided into the small blocks and these blocks constitute steps from basic to complex at the FPGA_b_DEEP. Another difference is that Graphic design is preferred to HDL design for educational purposes. Some other related studies, from [9] to [12], are given at references part also. The example named "A Simulator Core Design for ADC" was the first completed and published example from the instructive and attractive examples series [13]. The second example is introduced at this study. The third example named "Data entry organization for a calculator" was completed and published [14]. The Clock-Calendar Design primarily is developed to teach how to use counters, comparators, decoders and multiplexers together. Instead of using ready components for counters, counter module units have been redesigned so that instructive capacities of examples have been increased. This part is presented in section 3. The other most crucial instructive part takes place in the setting block. In this part, students have got much more opportunity for adding their thoughts and inspirations to the design according to the other blocks. This block is presented in section 4. The block where BCD to seven segments takes place is presented in section 5 and finally in section 6 the unity of blocks is presented. Altera–DE2 educational board is used as an application board.

Adapting The Example to Digital Electronics (DE) Courses

This example should be used after completing the fundamental DE subjects and spared 3 weeks in the curriculum. The hours per week should be at least four hours. The place of the example in the course plan and completion time is decided with the experience gained at the process after 2007 in which FPGA _b_DEEP project has started. The designed example is divided into three sub block as counting, setting, and display and one week is given for each. The example is designed in a way that it can be completed with in-class or out-of-class studies. The blocks presented in this study are designed for in-class studies and simplicity is considered to increase their instructive character. Additionally, the students are expected to improve their designs by setting them goals and guiding them, in their studies after courses. The most important feature that makes the example attractive is that the students are designing their own clock calendar. This is important for the students to gain self-confidence.

Counter Block

In this block, the students have a chance to experience how to produce a counter, how to build blocks from circuits and putting different blocks together to get new blocks. The steps given at table-1 are prepared for classroom/laboratory works.

Table-1: Important Steps for Classroom work

a	See the relationship between a pulse divider circuit and a counter circuit to understand the logic of the counters. There must be 4 output pins at the counter circuit to drive a seven segment display
b	Design a comparator using exclusive-or (xor) gate function and compare Max_value with counter output value. Obtain the C_{out} value and reset the counter when equality is provided
c	See the simulation results and evaluate performance
d	Try to get better simulation results by adding flip flops (dff) to suitable places of the circuit and understand the

	function of system clock (sys_clk) pulse
e	Convert the circuit to a counter block counts till to 9. Obtain a new block counts till 60. Then obtain clock block consist of second, minute and hour blocks.
f	Obtain a calendar block as a new separate block by making small changings on the clock block. Take into consideration that counter limits are different for days and months

Simulation Details

It is important for students to interpret simulation results of design at each step. There are simulation results in Fig. 1b obtained from that circuit seen in Fig -1a. While selection input is “up” position, counter value reaches 9, it resets and starts from 0 again. Because Vset value was arranged to 9. While selection input is at “down” position, down counting goes on till number 9, it resets and starts from 15. Xnor_out value reaches to “1111” when counter output value is equal to maximum value. Delay in reset can be decreased by increasing sys-clk frequency.

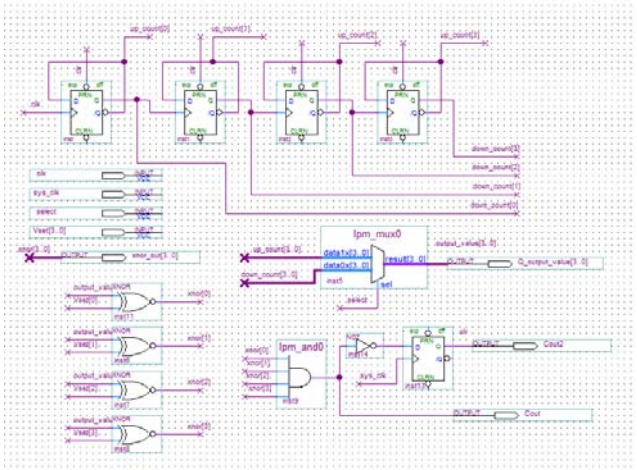

Fig. 1a: Main counter block which counts to 10.

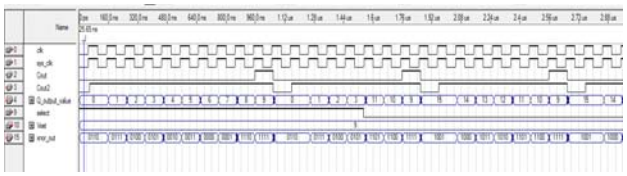

Fig. 1b: Simulation result for main counter block.

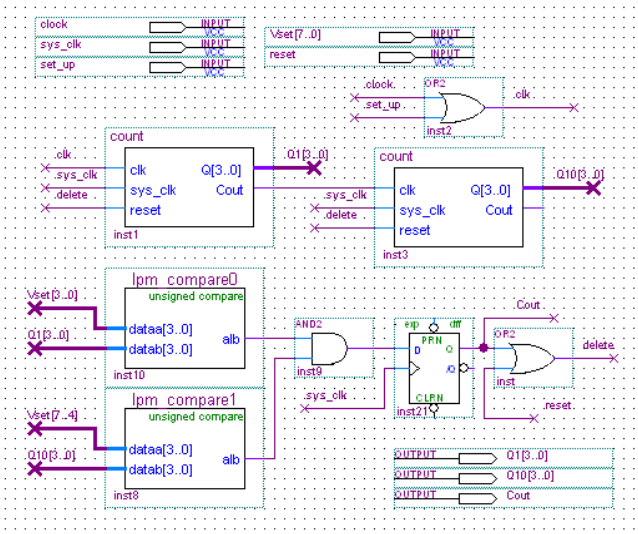

Fig. 2a: The counter circuit which counts till 99 and comparing operation

Targets For Out-of-Class Studies

The target studies to be requested from the students related to this block is grouped in two. First one is the studies that can be done on the main counter, second one is the design of new small blocks to be generated after using the main counter block certain times.

In the first group of study, usage of available component should be requested for operations such as comparison and resetting and synchronized counter model for more sensitive study. In the second group of study, it should be requested to form clock (second, minute and hour) and calendar (day, month, and year) blocks by using main counter block for certain times and adding the comparators that will form the limitations. Two designs are prepared to guide the students at this stage. In Fig 2a-2b, it is presented how two counter block that counts till 9 can be combined to build a counter block that can count till 99 and how this counter is reseted when it reaches 60.

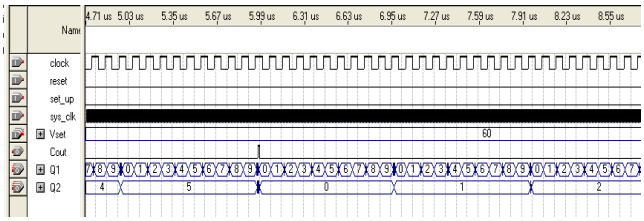

Fig. 2b: The simulation results for counting till 60 and resetting

At the design in Fig 3a, it is shown how the counter blocks that count till 60 can be combined as a new block. This block can be used as a clock or a calendar. The only difference between the clock and the calendar is that C_{out} signal of the clock block is sent to calendar block as input pulse. Simulation results of the clock circuit can be seen in Fig 3b.

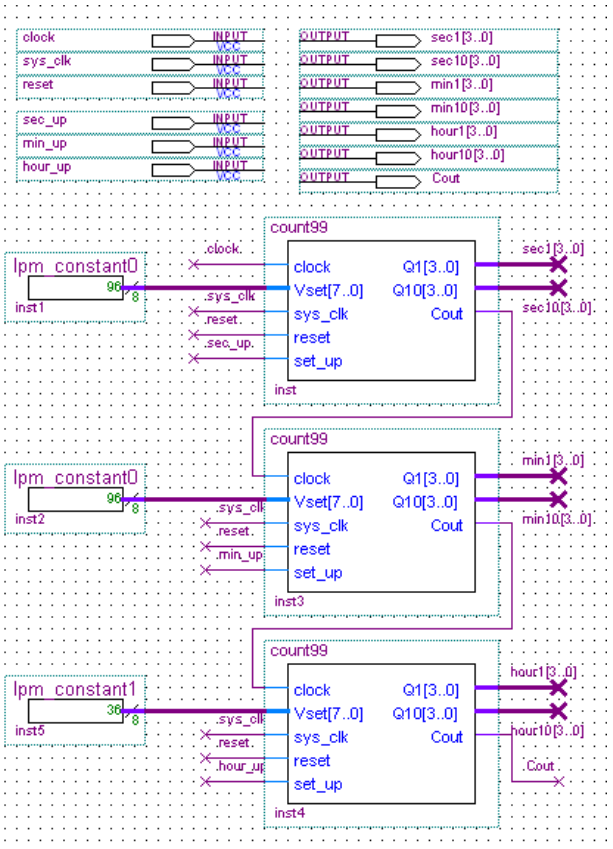

Fig. 3a: The Full counting circuit can be used clock or calendar

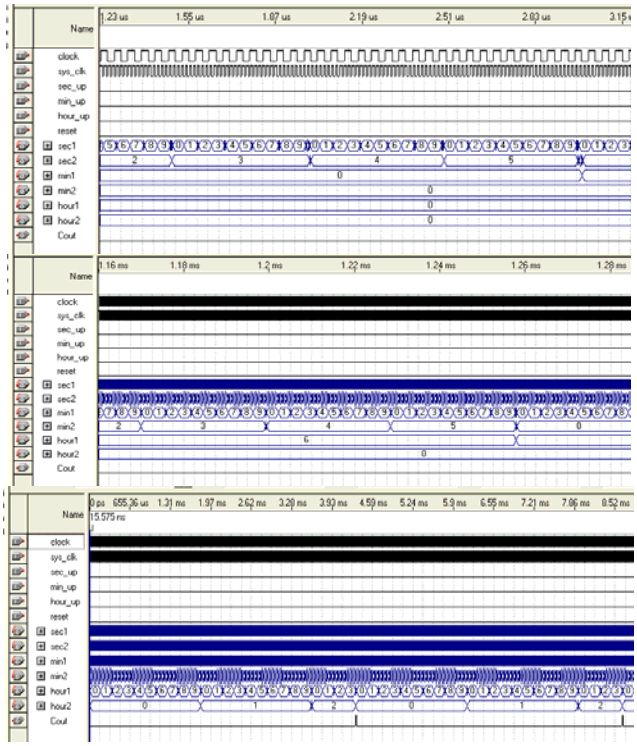

Fig. 3b: The Full counting circuit can be used for clock or calendar

Setting Block

In this block, students have got much more opportunity for adding their thoughts and inspirations to the design according to the other blocks. Because there are lots of design alternatives for students. Recommended classroom Work steps are given at table-2. Although step (a) is theoretical, we need this step in order to help students understand the function of the block better.

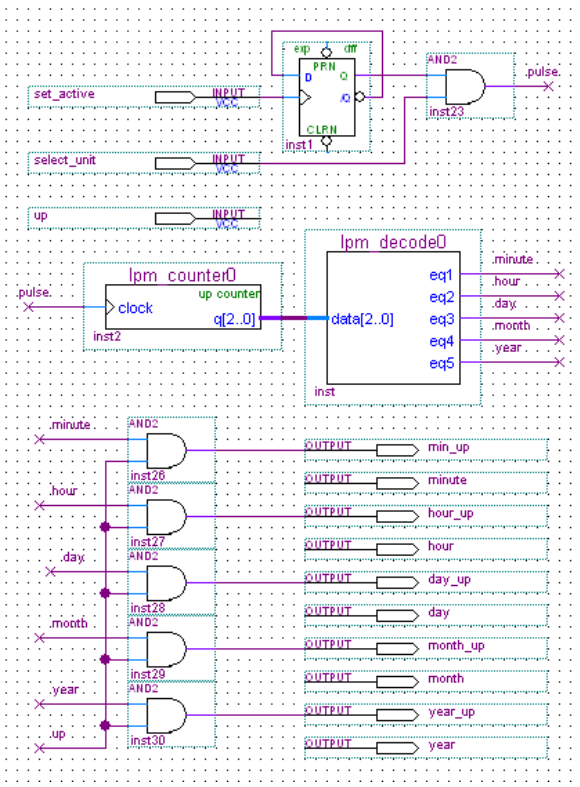

Fig 4a: Setting block

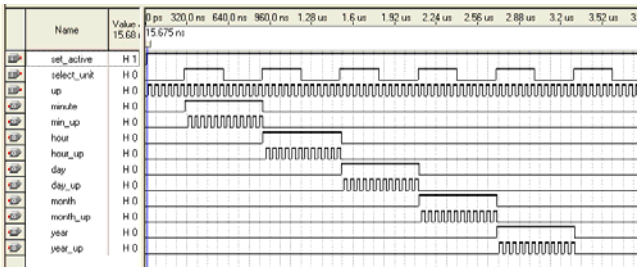

Fig. 4b: Simulation result for setting block

Table-2: Important Steps for Classroom work

a	Select the buttons to be used in setting work, and determine functions to be given to buttons. Example: Button 1: Selection of clock or calendar, Button 2: Activating setting process, Button 3: Selection of unit (min, hour, month, year), Button 4: Up process for selected unit.
b	Use a mux for choosing clock or calendar
c	Use a counter and decoder in selecting unit
d	Send the selected unit signal at the output of the decoder and the signal received from up-button to the related counter block using 'AND gate.'

In Fig 4a, the unit belonging to setting process is presented. After Set is activated, setting (selection of unit) can be done as min, hour, day, month, and year. Setting function can only be done as up-count for the selected unit. Here, students' attention is required to be drawn to the usage of AND gate, whose function is very important and very easy to use. In Fig 4b, simulation results are illustrated to show how units are selected in turn, and how up-count process is performed.

Targets for Out-of-Class Studies

At the example provided at Fig 4a, the set process brings the counter to the desired point by always making it count upwards. This causes difficulty in usage and waste of time. The students are requested to solve this problem.

Display Block

The most difficult part for students while designing the display block is the process of flashing the displays at intervals of a second for indicating the selected unit of setting block. Recommended classroom Work steps are given at table-3.

Table-3: Important Steps for Classroom work

a	Unite the drivers for each 7 segment displays.
b	Unite total 12 bits clock bus related to 'second, and minute' with total 12 bits calendar bus carrying day, month and year input, and connecting related bus input to the display block according to the selection in setting block.
c	In order to follow the selected unit on the display, related digits must be turned on and off at intervals of a second and multiplexers must be used.

In Fig 5(at appendix part), the display block is seen. First multiplexer row is used for clock-calendar selection and the united selection bits on DE2 FPGA board must be controlled by button-1. Second multiplexer row is used during setting operation to turn the displays on and off. Each multiplexer has two inputs. First inputs carry the clock-calendar date which will appear at displays, and second inputs carry the data which make the displays passive by turning all display LEDs off. When we change the multiplexer selection bits' signal with an interval of a second, flasher working appears on displays. By this way, we can understand if the clock calendar is at normal working or at set working position. The simple circuit to create turn on/off for selected unit takes place on the upper part of the Fig 5.

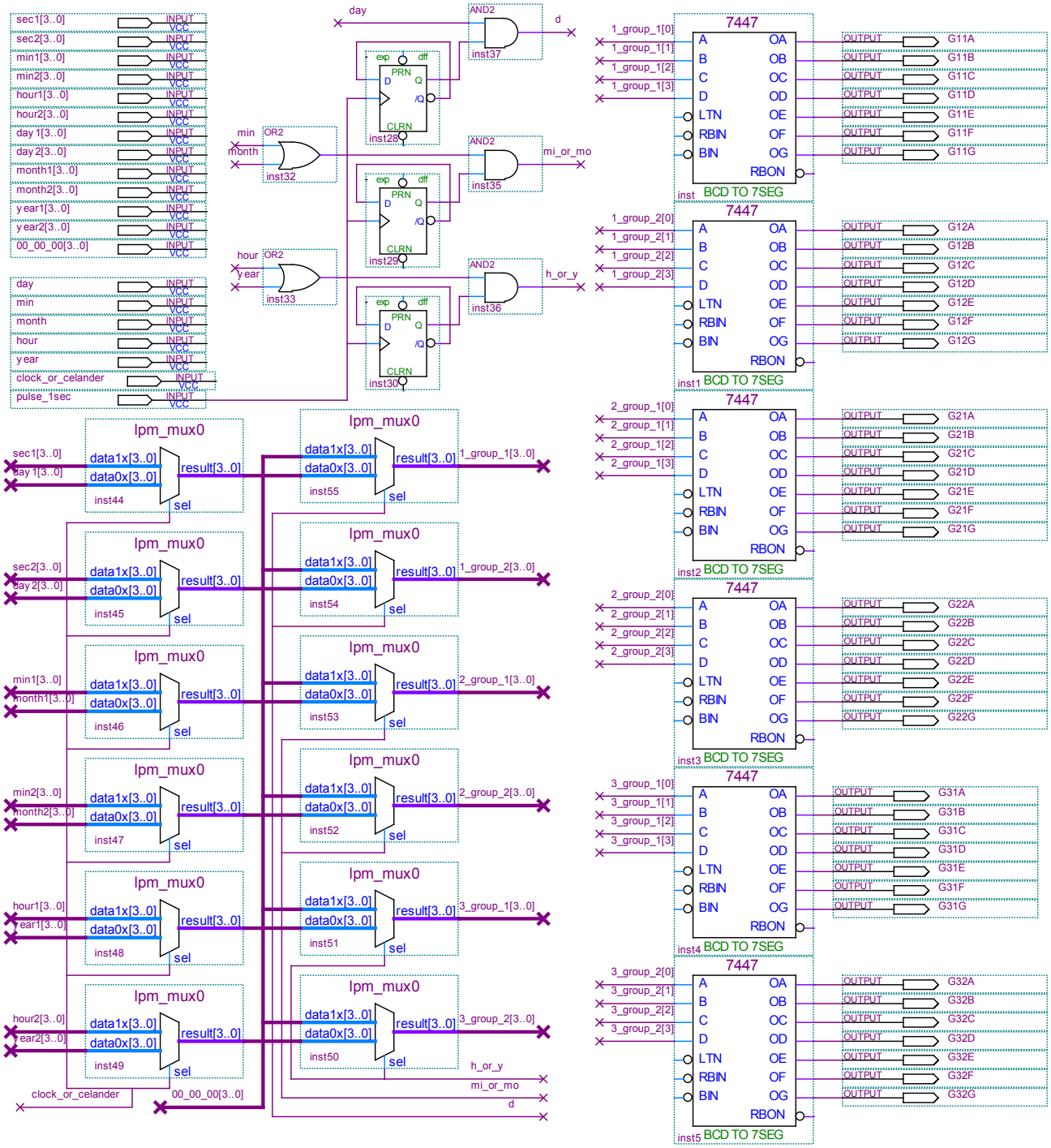

Fig. 5: Display block

Targets for Out-of-Class Studies

Some extra studies for bright students like the use of LCD display, automatic setting of leap month or years, i.e., months having 28, 29, 30 and 31 days, adding down-count characteristics to up-count setting function are designated.

Union of the Blocks

Main clock-calendar block is made up of three basic blocks. They are counter block, setting block and display block. Every block has its own sub blocks. The blocks given in Figs 3a, 4a and 5 must be united to obtain the main block. In addition to three basic blocks, one more block having a frequency of 1 MHz is required. This block includes one counter which gives an output pulse (C_{out}) in a second. Because of its simple structure, the block design is left to students. At the end, all of the basic blocks must be connected to each other.

Discussion

In FPGA based Digital Electronics Education Project, primarily digital electronic education is aimed, therefore graphic design is preferred. The example can be redesigned using HDL codes. and used as an effective example at the transition period from graphic design to HDL design. Even though students accept that HDL is more practical, they also realize the importance of digital electronic knowledge consolidated by graphic design. When special examples are divided to stages and prepared to provide the use of some components, as presented in this study, positive effects of these special examples were

seen clearly on the students. By the help of these examples the students can get the chance to repeat and combine the subjects they learned stage by stage. It was also seen that these examples have psychologically positive effects on the students. This effect is proved by the students who spent a lot of time to study even out of the class. The fact that students are able to make their own designs of clock calendars and calculators gives them self- confidence and motivation.

Conclusion

In this paper, we present a study outlining the benefits of a FPGA based Digital Electronics Education for electronics/computer engineering students or new designers. Through the design and implementation of a FPGA based clock-calendar project, the students enhance their skills of using counter, multiplexer, comparator and a decoder together. A graphic design allows the students to see the outcomes of their projects immediately. Our experiences have shown that FPGA based Digital Electronics Education enables the students and new designers to learn the material quickly and thoroughly. Our goal is to move on the same path and present calculator and basic CPU projects as the 3rd and 4th examples in this instructive and attractive example series soon.

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Autors

Vedat KIRAY, PhD (Corresponding author.) : He graduated from Institute of Science, PhD-Electronics Engineering Department of Sakarya University in Turkey.

E-mail: vkiray@turgutozal.edu.tr Tel.: +90-312 551 50 54, Fax: +90-312 551 54 20.

Mairambek ZHAPAROV : E-mail:meirambek.zhaparov@gmail.com