Dominik KRASOWSKI, Bolesław KUCA

Warsaw University of Technology, Poland

Computer Simulations of Protection Devices for Proper Overvoltage Protection Creation

Abstract. *The paper deals with protection of electrical and electronic equipment of a structure against lightning overvoltages penetrating its installation. The protection is assumed to be performed according to the concept of lightning protection zones (LPZ) [4], [6]. In order to recognize the conditions for efficient selection, location and coordination of overvoltage protection measures, adequate laboratory tests and computer simulations in PSpice computer program of overvoltages in different arrangements have been developed. Obtained results have been in the paper presented and discussed*

Streszczenie. *Artykuł dotyczy ochrony elektrycznego i elektronicznego wyposażenia obiektu przed przepięciami atmosferycznymi, wnikającymi do instalacji obiektu. Zakłada się, że ochrona ta ma być realizowana zgodnie z koncepcją stref ochrony odgromowej (LPZ) [4], [6]. Aby rozeznać warunki skutecznej selekcji, lokalizacji i koordynacji środków ochrony przeprowadzono odpowiednie badania laboratoryjne i symulacje komputerowe przepięć w różnych układach przy zastosowaniu programu PSpice. W artykule przedstawiono i omówiono uzyskane wyniki. (**Symulacje komputerowe urządzeń ochrony przepięciowej wykorzystywane do tworzenia prawidłowej ochrony przepięciowej**)*

Keywords: lightning overvoltages, induced voltages, electromagnetic coupling, Surge Protective Device (SPD)
Słowa kluczowe: przepięcia piorunowe, napięcia indukowane, sprzężenie elektro-magnetyczne, urządzenie do ograniczania przepięć (SPD)

Introduction

It is important to know, how significant is not only coordination between SPDs and devices to be protected, but also the coordination between all other protective measures involved to protect these devices with their circuits. Consequently, the progressive concept of up-to-day protection against lightning overvoltages should take into consideration not only conditions accepted for present International Standards [2], [3], [4], [5], [6] but also the conditions resulting from the nature, configuration and parameters of the circuits with their loads, what has been ignored in the Standards. Every structure with its equipment has specific features, which may modify significantly the overvoltage conditions for different circuits.

Cases of overvoltage occurrence

The lightning channel, down conductors, earth terminations, ends of incoming lines and circuits connecting these lines with devices of the structure equipment to be protected belong to main elements of real arrangement under consideration. The tests have been focused to the measuring of voltages in the points located at the beginning and at the end of the circuits connecting the incoming lines with the devices to be protected. The voltages in these points depend not only on their initial sources but also on the circuit features and parameters as well as on the applied protection measures.

Basic protective measures consist of surge protective devices (SPD) [2], [3]. In order to look consciously for the suitable SPD positioning [1] one should recognize all locations of the lightning, at which overvoltages may appear. These locations, according to the standards [4], [5], are following: the LPS (lightning protection system) of the structure, the structure surroundings, the lines entering the structure, and the surface near to the lines.

In the first location the overvoltages arise on the LPS earthing resistance and are transmitted through the bonding bar and SPDs to the protected circuits and to the incoming lines. Moreover additional overvoltages may appear due to magnetic coupling of lightning channel with internal circuits to be protected.

In the second location the overvoltages may appear in internal circuits due to their magnetic coupling with lightning channel. Resistive coupling through the ground and buried conductive parts are not excluded.

In the third case of location the appearing overvoltages are limited to the level of line insulation withstand voltages and to the level of voltage drops caused on the way of lightning current to the ground. Additional overvoltages may also appear in the internal circuits to be protected due to their magnetic coupling with lightning channel.

In the last (fourth) case of location the overvoltages may be induced both in the incoming line and in the internal circuits to be protected.

Arrangements and procedures

Two arrangements presented schematically in Fig. 1 and in Fig. 2 have been taken into account.

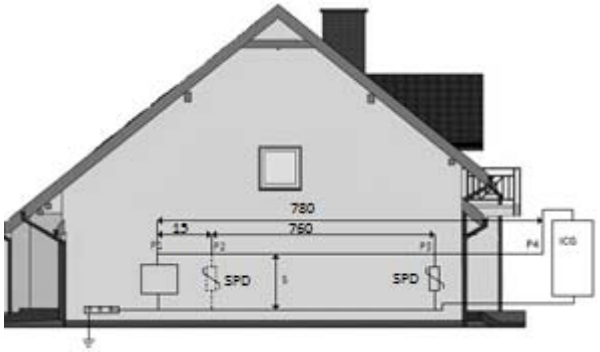

Fig. 1. Investigated arrangement (dim. are given in cm)

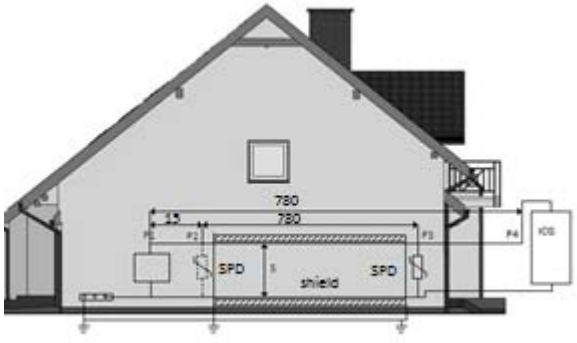

Fig. 2. Scheme of investigated shielded arrangement

The circuit of first arrangement (Fig. 1) is without shield and has been selected for laboratory tests only in order to assess the influence of induced voltages. The second arrangement (Fig. 2) is equipped with metallic shield in order to eliminate influences of inductive voltages and this

arrangement has been just used for PSpice computer simulations.

PSpice Simulations

For PSpice computer simulations the arrangement of Fig. 2 with varistor SPD [7], [8] has been replaced by the scheme as shown in Fig. 3. It consists of the current generator, the connecting line with terminals AB for devices to be protected and the SPD at its entrance.

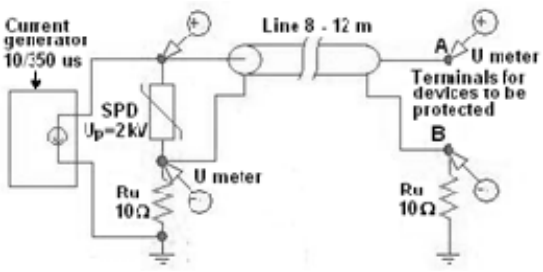

Fig. 3. Scheme of shielded arrangement with spark-gap used for PSpice simulations

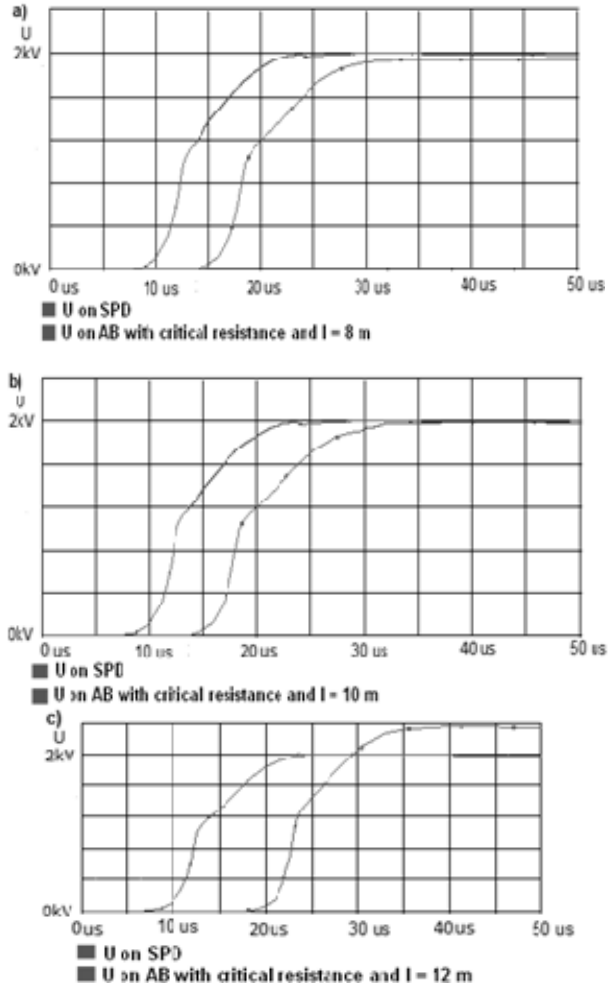

Fig. 4. An example of simulation: residual voltage on varistor for three different length of the wires between SPD and protected device (R = 10 Ω) : 6a) 8m, 6b) 10m and 6c) 12m.

Wave shapes of the current for the first and subsequent strokes simulated by the impulse generator of the scheme (Fig. 3) have been described by Heidler relation:

$$i = \frac{I}{k}\frac{(t/\tau_1)^{10}}{1+(t/\tau_1)^{10}}\exp(-t/\tau_2) \tag{1}$$

where: I - current peak value; k - correction factor; t – time; τ_1 - front time constant; τ_2 - tail time constant.

Three line lengths have been assumed: 8, 10 and 12 m. For the length of 10 m the critical value of loading resistance R = 10 Ω connected between AB terminals has been applied. For SPDs at the line entrance the protection level of 2 kV has been assumed. Simulation results are shown in Fig. 4

Simulations show that the distance between SPD and the protected device as well as its resistance are very important. Successive diagrams in Figure 4 show that the distance is coordinated with critical value of loading resistance. When the resistance value is greater than critical one the overvoltage on the device terminals increases and additional SPD is needed. It is easy to state that the length of 10 meters is a critical value for this arrangement, when the protected device is free from overvoltages.

Laboratory tests

In order to confirm the simulation results and to investigate the meaning of induced voltages the laboratory tests have been undertaken in accordance with the arrangements given in Fig. 1 and in Fig. 2. The test scheme has been explained in Fig. 5. Current generator produces impulses with the shape close to 10/350. Such impulses were injected in point P_4 (Fig. 1 and 2) to the circuit connecting the incoming line or impulse generator with the device to be protected. This circuit is of different length. 780 cm long and the distance between its parallel horizontal conductors (with 0,3 cm diameter) is equal 5 cm. It is connected to the protected device, which parameters (R= 0,9 Ω and L = 10 μH) have been so selected that the possible reflections could be limited to a minimum. The reflections might be a reason for voltage increase at terminations of protected device. The conductors in SPD branches were as short as possible. They were inserted to the circuit alternatively in points P2 and P3 (Fig. 1). The voltage drops on these conductors could also increase the voltages at the terminations of the protected device.

SPD being a single varistor with protection level 0,8 kV have been selected for investigation, located at the end (p. P_2) and alternatively at the beginning (p. P_3) of the circuit.

Impulse currents have forced every time the voltages in point P_1 and alternatively in points P_2 or P_3 according to the sequence resulting from items 1) and 2). In this way it was possible to observe the changes of voltages appearing on the protected device, when the SPD was located in greater and smaller distances from this device. Measurements of these voltages (in points: P_1, P_2 and P_3) have been performed according to the impulse generator scheme presented in Fig. 5.

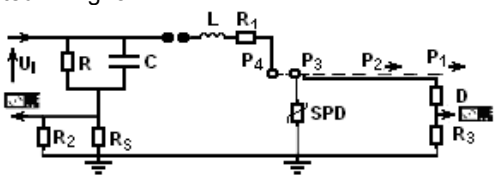

Fig. 5. Scheme of impulse current generator with measuring sets

Among basic data of impulse generator parameters there are: main capacity of the current impulse generator C = 0,8 mF; parallel resistance R = 1,05 MΩ; inductance of discharge circuit L = 23 nH; resistance of discharge circuit R_1 = 13,5 Ω; the range of loading voltage U_l could be changed within the limits up to 10 kV.

The components assigned for measurements contained two their sets: current measuring set and voltage measuring set. The current measuring set consisted of the shunt R_s =

2,1 mΩ with fitting resistance R_2. Measured impulses taken from the shunt were sent to the digital oscilloscope. The voltage measuring set consisted of voltage divider D (Fig. 5) with the fitting resistance R_3 = 75Ω. The voltage ratio of the divider was defined as δ = 200. Measured voltage impulses, taken from the divider, were sent also to the digital oscilloscope and allowed to register the voltage changes and to form the archives.

For voltage measurement in different points of the relevant arrangement, namely in points P_1, P_2 or P_3, the divider was switched over from one of these point to another according to the program of investigations. The voltages measured in these points have been distinguished by corresponding symbols: U_{P1}, U_{P2}, and U_{P3}.

The loading voltage U_l was changed during the measurements within the limits from 1 kV to 6 kV

Test results and comments

The case of unshielded arrangement of Fig. 1 is considered. Due to impulse currents injected in point P_4 the voltages appeared in points P_1 and P_2 as well as in points P_1 and P_3 of the circuit and they were measured in due sequence. Obtained results consist of a set of voltage values and registered their curves. The values obtained for all investigated arrangements have been specified in table 1. Comparing these values one can easily state that the voltages on the protected device (U_{P1}) are strongly dependent on the distance to the protecting SPD. The way of its installation and the values of loading voltages are also important.

Table 1. A set of results obtained for arrangement with varistor

Loading voltage U_1 [kV]	Arrangement and measured voltages			
	At the end		At the beginning	
	U_{P2} [kV]	U_{P1} [kV]	U_{P3} [kV]	U_{P1} [kV]
3,0	0,84	0,86	0,84	1,60
3,5	0,84	0,88	0,85	1,80
4,0	0,86	0,90	0,85	1,85
4,5	0,88	0,90	0,88	1,90
5,0	0,88	0,95	0,88	1,92

Analyzing obtained voltages one can state unexpectedly that voltages U_{P2} and U_{P3} are greater than U_{P1} (see item 1 at U_1 = 3,5 kV and item 2 at U_1 = 1,5 kV).

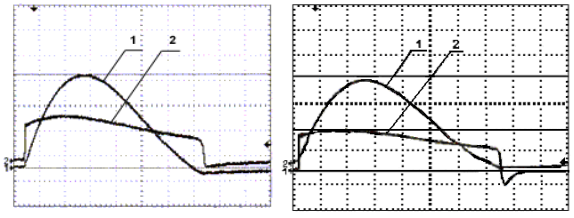

Fig. 6. Curves of voltages: a) U_{P1}, b) U_{P3}, registered in arrangement item 1) at beginning and U_1 = 3 kV

Two examples of registered voltages are shown in Fig. 6. They have been selected to compare the change of voltages on the protected device at different SPD locations for U_1 = 3 kV. Fig. 6 allows comparing the voltages U_{P1} and U_{P3} for arrangement equipped with one varistor SPD. The curves are different and obtained voltage values are different. The voltage U_{P1} is above 30 % greater than U_{P3}.

Shielded arrangement was almost the same, but the circuit was placed in metallic pipe grounded on both ends as in Fig.2. Diameter of the pipe was equal 15 cm and its length - 760 cm. Thickness of the pipe metal was 1 mm. For the test the same generator was used. the results are shown in table 2

Table 2. A set of results obtained for shielded arrangement

Loading voltage U_1 [kV]	Arrangement and measured voltages at the beginning			
	two composed SPD		varistor as SPD	
	U_{P3} [kV]	U_{P1} [kV]	U_{P3} [kV]	U_{P1} [kV]
4,0	1,30	1,30	650	650
5,0	1,36	1,40	670	670
6,0	1,40	1,45	730	740
6,5	1,50	1,45	750	750

Conclusions

- Voltages appearing on protected devices are, as a rule, greater than voltages on SPD and the difference increases with a distance between them.
- The voltages appearing during the tests on protected devices depend distinctly on loading voltage values and the distance of SPD installation.
- The way of SPD installation influences considerably its efficiency.
- Simulations in PSpice showed the same results as laboratory tests.

REFERENCES

[1] Krasowski D.: "Considerations on basic parameters of low voltage surge protection devices and their application problems" XV IC on EMD 21-23. 09 2005 Białystok, P. 7.3, p. 1-4.

[2] IEC 61312-3:1999. Protection against LEMP. Part 3: Requirements of surge

[3] IEC 61643-11: Low-voltage surge protection devices. Surge protection devices connected to low-voltage power systems – Requirements and tests.

[4] IEC 62305-1:2006. Protection against lightning – Part 1: General principles.

[5] IEC 62305-2:2006. Protection against lightning – Part 2: Risk management

[6] IEC 62305-4:2006. Protection against lightning – Part 4: Electrical and electronic systems within structures.

[7] IEC 61643-12:2005. Low-voltage surge protection devices. Surge protection devices connected to low-voltage power distribution systems - Part 2: Selection and application principles

[8] Krasowski D., Zdobysław Flisowski Z.: „Problemy doboru ograniczników przepięć do ochrony urządzeń elektrycznych i elektronicznych w obiektach budowlanych (1)" Elektro-Instalator nr 10-11/2006 str. 42-48

***Authors**: dr inż. Bolesław Kuca, Politechnika Warszawska Zakład Wysokich Napięć i Kompatybilności Elektromagnetycznej ul. Pl. Politechniki 1 00-661 Warszawa , E-Mail: kucab@ee.pw.edu.pl; mgr inż. Dominik Krasowski, Politechnika Warszawska Zakład Wysokich Napięć i Kompatybilności Elektromagnetycznej ul. Pl. Politechniki 1 00-661 Warszawa, , E-mail: ominik@wp.pl*

The correspondence address is:
e-mail: ominik@wp.pl