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A New Approach to the Design of Low-Complexity Direct Digital Frequency Synthesizer

***Abstract**. A low–complexity direct digital frequency synthesizer based on linear interpolation method is presented in this paper. The proposed architecture employs a new technique to derive the slope coefficients at the first sample of each segment's interval thereby eliminating the ROM which stores those values. ROM elimination has resulted in significant logic element saving and simplified the whole DDFS structure. The proposed DDFS has been analyzed using MATLAB and tested over entire Nyquist frequency range. The spurious free dynamic range (SFDR) of synthesized sinusoid achieved is 84 dBc. The resultant low complexity architecture along with high spectral purity synthesized signal meets the specifications of recent portable battery-driven products.*

***Streszczenie.** W artykule przedstawiono bezpośredni syntezator cyfrowy częstotliwości, opracowany w oparciu o metodę interpolacji liniowej. Zastosowana technika pozwala na uzyskanie współczynnika pochyłości już z pierwszą próbką każdego z interwałów segmentów, przez co eliminowana jest konieczność użycia pamięci ROM. Przeprowadzono symulacje proponowanego rozwiązania w pełnym zakresie częstotliwości Niquist'a. Działanie metody zostało porównane z innymi znanymi architekturami. (**Nowe podejście do projektowania bezpośredniego syntezatora cyfrowego o małej złożoności**).*

Keywords: Direct digital frequency synthesizer, DDS, ROM-less DDFS, piecewise linear approximation.
Słowa kluczowe: bezpośredni syntezator cyfrowy, DDS, DDFS bez ROM-u, odcinkowa aproksymacja liniowa.

Introduction

Direct Digital Frequency Synthesis (DDFS) systems are regarded as being the most suitable for modem digital communication systems. In contrast to the Indirect digital phase looked loop (DPLL) synthesizer, the DDFS system is better in terms of precisely and easily handling its frequency, phase and amplitude in a digital form. Due to such features, it is becoming more possible to incorporate the DDFS with different digital modulations by using a digital signal processing method. The conventional DDFS structure is given in Fig.1.It has three basic blocks: phase accumulator, phase to amplitude converter, which usually employs ROM as a sine lookup table and digital to analogue converter.

ROM-based DDFS creates sine-wave output by indexing through a sine lookup table (LUT); the LUT contains the sine amplitude values corresponding to each possible phase value. At each clock period, the phase accumulator adds up an *M*-bit frequency instruction word (FIW) to generate these phase values. After a certain number of clock cycles equal to 2^M/FIW, DDFS generates one complete synthesized sine wave cycle. Hence, the period of the synthesized signal is simply equal to: clock period × (2^M/FIW), or the output frequency is given by

(1) $$f_{out} = \frac{FIW}{2^M} f_{clk}$$

The lowest frequency signal f_{min} can be generated by indexing through all (2^L) sine amplitude values when the FIW set to 1. Thus it can be expressed as;

(2) $$f_{min} = \frac{f_{clk}}{2^M}$$

For practical consideration, the DDFS can only generate frequencies up to 40% of the clock frequency; the constraint comes from the sampling theorem. It is obvious that whenever *L* increases, the size of ROM increases exponentially. The large ROM consumes high power and large area which is degrading the performance of DDFS, taking into account that the upper bound of the SFDR based on phase truncation is given by:

(3) $$SFDR = 6.02L - 3.92dB$$

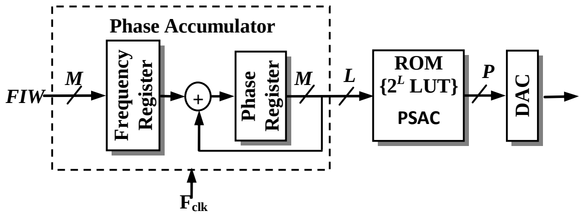

Fig.1. Basic DDFS structure

Which can be improved only with high phase resolution (i.e. large *L*), and that makes it difficult to obtain high spectral purity with small chip area and low power consumption. However, undesirable excessive power consumption must be alleviated in portable communication equipment. It is thus necessary to use some compression techniques to reduce the ROM size while still retaining high spectral purity.

Considering the fact that the ROM-based look up table has a perfect approximation of the sinusoid amplitude corresponding to all phase angles which are absent in other methods, all the recent works tried to imitate the proficiency of ROM-based LUT without any dependence on complex circuits that inherently use excessive power. So, the researchers tend to focus towards reducing the number of bits before applying it to the ROM and it is done either by truncating the output of the phase accumulator thereby eliminating a significant amount of ROM size, or reducing the ROM size by exploitation of trigonometric identities' principles [1]. For the first approach, even though the ROM size can be significantly reduced by truncating the output of the phase accumulator, the added spurious noise will degrade the spectral purity [2]. The alternative approaches completely discarded the need of a ROM by computing the samples of sine amplitude of the digital phase contents. The ROM elimination has been investigated in many researches, such as [3,4]. The ROM-less DDFS is based on a special phase conversion algorithm such as Taylors series evaluation [5], the second order parabolic approximation [6,7], the first order Chebyshev approximation [8], the coordinate rotation digital computer (CORDIC) algorithm [9,10], the piecewise linear approximation [11] and so on . However, it will be hard for any method that is based on high-order polynomials to meet the speed requirement of wireless communication applications. For instance, the hardware realization of Taylor's series evaluation is complicated and the running speed is slow. This paper investigates and proposes a novel DDFS architecture which is based on piecewise linear approximation. The proposed DDFS can simultaneously achieve an excellent spectral purity without additional circuitry.

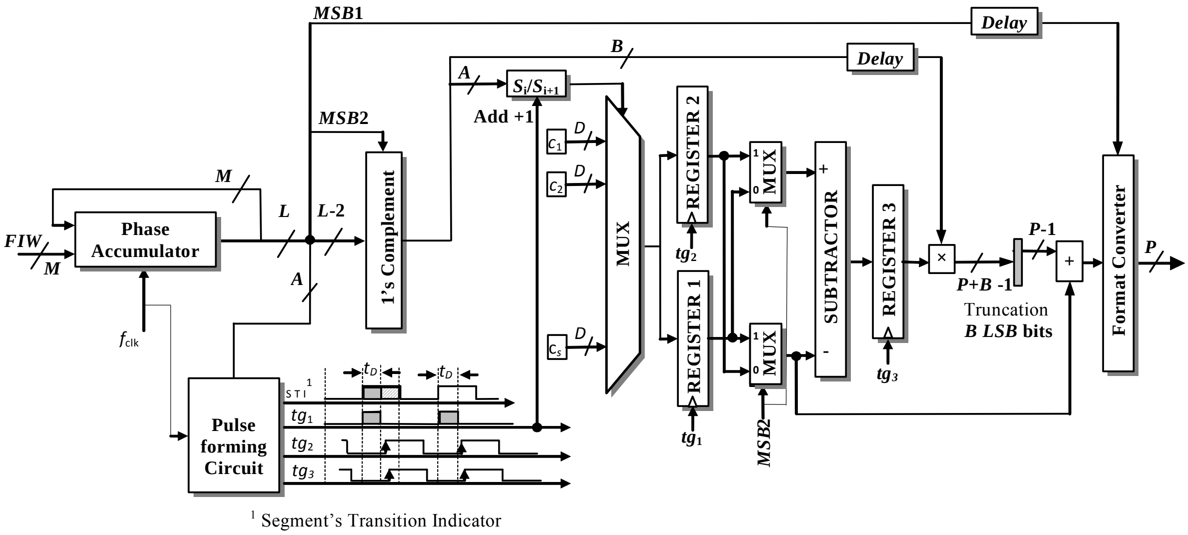

Fig.2. Block Diagram of the Proposed DDFS Architecture

Piecewise Linear Approximation Background

By employing the quarter wave symmetry, the sine amplitudes must be calculated for angles in the interval [0, $\pi/2$). The first quadrant to be approximated is

$$f(x)=\sin\frac{\pi}{2}\left(x+\frac{1}{2^{L+1}}\right) \quad (4)$$

Where: x is a fraction in the interval [0, 1), and is expressed in L bits, and $1/(2^{L+1})$ equal to 1/2 LSB of x, is the required phase shift to exploit quadrant symmetry [13]. In piecewise linear approximation, the first quadrant of the sine function is subdivided into s segments and each segment approximated by a linear polynomial of the form

$$P_i(x)=M_i(x-x_i)+C_i \;,\; x_i \le x \le x_{i+1} \;\; \& \, i[0:s-1] \quad (5)$$

Where M_i, and C_i are respectively the slope and initial amplitude coefficients of the ith segment.

All the previous works in the piecewise linear approximation [14-16] are based on the concept mentioned above, however, the difference comes from the evaluation of the M_i and C_i coefficients in such a way as to achieve good precision on the approximation of the sinusoid amplitude corresponding to all phase angles, and how can these coefficients be implemented without using complex circuits that inherently consume excessive power.

Direct implementation of the first order interpolation method requires two ROMs. The first is used to store the values of slope and the other for the storage of initial values. The existing technique, based on piecewise linear polynomials was first introduced by Freeman [14]. He approximated the first quadrant of the sine function by 16 piecewise linear segments. Initial amplitudes and segment slopes were stored in two ROMs, the architecture also incorporated with multipliers, adders and an additional small ROM to store the correction's values. In [15], the first quadrant of the sine function was approximated with linear segments of unequal lengths; the coefficients were carefully selected to improve the approximation. The other technique employed a single ROM clocked by twice frequency to drive the polynomial coefficients [16]. For this approach, operating the digital system with double clock frequency is a vital drawback. The actual output frequency range descended to 50% in comparison with existing counterpart architectures.

The difficulty arises from the fact that access to the memory cells is valid once at a specific time. This paper introduces a new technique that allows accessing the memory twice in one clock cycle using time sharing. By this approach, we need not have a new complex coefficient calculation, the coefficients simply relate to fewer conventional sine LUT points..

Proposed DDFS Architecture

As mentioned before the concept of this technique is the same as used in [14-16]. Fig.2 shows the block diagram of the proposed DDFS architecture. The *MSB*2 is used to select the quadrants of the sine wave, while the *MSB*1 is used to control the format converter [17].The remaining *L*-2 bits are fed into Complementor whose output is split into two parts, the *MSB* part, with *A* bits long, represents the *s* segments, and the *LSB* part with *B* bits long, represents an angle *x i*n the segment interval. A multiplexer (MUX) and its coefficients are the equivalent of a ROM which provide the segment initial amplitudes C_i. The proposed architecture also incorporates pulse forming circuit which controls the fetching and loading process of successive C_i coefficients. This circuit along with the three storage registers and one subtractor are essential to perform the task of the slope derivation.

Circuit Realization

As indicated in (5) each line segment is defined by two coefficients, M_i and C_i. The coefficient M_i which represents the slope of ith segment can be obtained from the segment initial amplitude coefficients C_i as follows.

$$\begin{aligned} M_i &= \frac{1}{\theta_s}(C_{i+1}-C_i),\;\; 0\le i\le s-1 \\ &= \frac{1}{\theta_s}[\sin(i+1)\theta_s-\sin(i\theta_s)],\;\; 0\le i\le s-1 \end{aligned} \quad (6)$$

where θ_s=π/2s, represent the length of segment interval which is quantized to *B*-bits length. Equation (6) can be realized by subtracting the sin($i\theta_s$) at successive phase angles and then dividing the result by θ_s. As θ_s unsigned constant coefficient equal to (2^B-1) we can see later the possibility of avoiding the division by slight modification, substituting (6 in (5) yields

(7) $$P_i(x) = \frac{[\sin(i+1)\theta_s - \sin(i\theta_s)].(x-x_i)}{\theta_s} + \sin(i\theta_s),\ 0 \le i \le s-1$$

It is clear that it must get two consecutive sine points at the same time to conduct the process of subtraction and extraction of the slope later. These two sine points can be got only when the corresponding phase angle point simultaneously to their addresses in the sine LUT and that is an inconsequent assumption. As mentioned earlier, the accessing of the memory is valid only once at a specific clock cycle. Thus, we introduce architecture of pulse forming circuit which performs the task of time sharing and proposes the procedure enumerated below to get around this problem.

The pulse forming structure is shown in Fig. 3a it has three simple blocks: digital comparator, pulse narrowing circuit (PNWC) and tapped delay. The schematic diagram is shown in Fig. 3b. We can deduce the operation of the pulse forming circuit by following the timing waveforms in Fig. 3c.

- At each clock cycle, the digital comparator examines the MUX Address inputs for detecting the changes in data select inputs i.e. transitions between the segments.
- The detected signal will then be applied to the pulse narrowing circuit (PNWC) to produce a t_D pulse width signal trigger1 (tg_1), which is usually a fraction of $1/f_{clk}$.
- Signal tg_1 gives an order to advance the data select inputs (DSI) of MUX by 1, hence the output of the MUX during this time slot is C_{i+2}.
- At the same time, tg_1 is used to load this value in register1 (R_1).
- After t_D, the data select inputs get back to the previous address value, so the output of MUX retreats to C_{i+1}.
- Trigger2 (tg_2) enables the register 2 (R_2) to load this value.
- Finally, the content of R_2 has to be subtracted from the content of R_1 and the resulting sum has to be stored in egister3 (R_3) at the tg_3 in order to get the targeted slope coefficient.

Simulation Results

Based on the concept introduced in the previous section, we have designed a DDFS with a targeted SFDR of 84dBc. The proposed DDFS was analyzed using MATLAB Simulink with 15-bit phase accumulator and 32 segments. According to [18], architecture of first order approximation with 32 segments has worst case spur of -84 dBc and this is below the SFDR upper bound for 15-bit phase resolution of uncompressed memory architecture. Consequently, the number of segments will determine the dominated spurs level. Fig.4 shows a MATLAB Simulink model of DDFS based on the architecture of Fig. 3. Where *A* is 5-bit length, *B* 8-bit length and *P* 14-bit amplitude resolution, yields to the total memory size of (2^5×14= 448 bit). The spurious level for the DDFS is shown in Figs. 5 for the output frequency of 23% of clock frequency when the FIW is set to 7536 . The results indicate an SFDR of about 84 dBc over the entire Nyquist range; this is in line with the theoretical upper bound introduced in [18] where:

(8) $$\mathrm{SFDR} = 24\mathrm{dBc} + 20\log \mathrm{S}^2$$

The compression ratio can be calculated with respect to (2^{L-2}×*P*) ROM size and *P*=*L*-1, where *L* is the phase resolution and *P* the amplitude resolution. It was shown that for our design with 15-bit phase resolution and 14 bit amplitude resolution which is yields a compression ratio of (2^5×14/2^{13}×14): 1=256:1 . Thus, we can conclude that the proposed architecture has advantages of simplicity and good spur level, with best compression ratio.

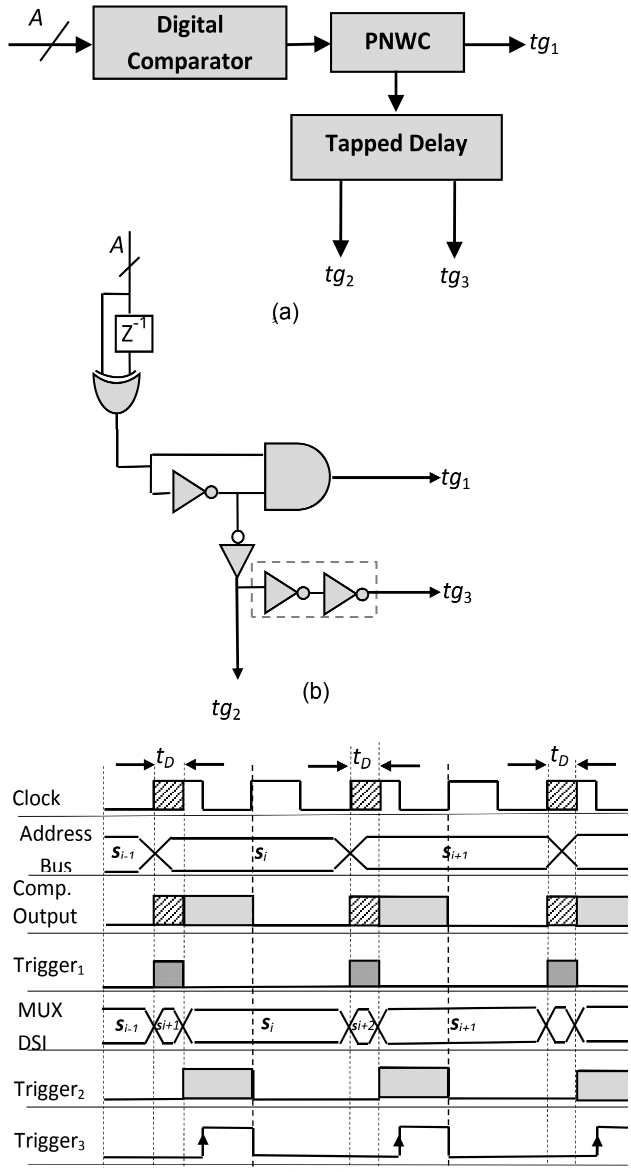

Fig. 3 Pulse forming circuit: (a) overall structure (b) Schematic diagram and (c) the timing diagram

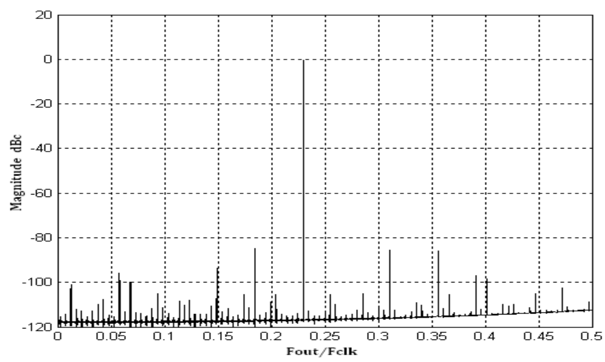

Fig. 5 Calculated output spectrum for f_{out} = 0.23 f_{clk}

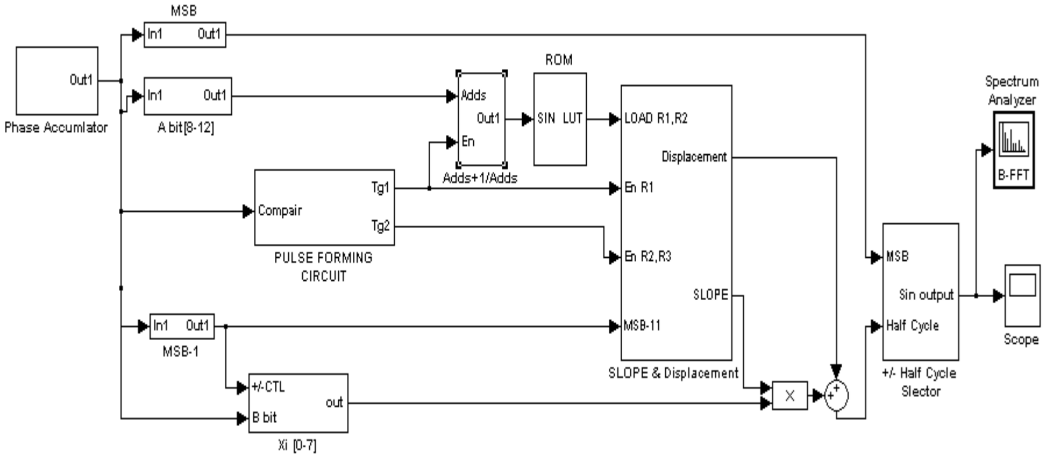

Fig. 4 The DDFS MATLAB Simulink Model.

Conclusions

In this paper, a novel ROM elimination technique was presented for application in low complex high spectral purity direct digital frequency synthesizers. Unlike many reported architectures that used complex circuits to compute the sine samples, Only 32 points from a standard sine LUT with fewer registers are required .System complexity is greatly reduced by using an efficient phase to amplitude conversion architecture. It was shown that a compression ratio of approximately 256:1 was attained. The proposed DDFS has been observed and tested over the entire Nyquist frequency range. The spurious free dynamic range of synthesized sinusoid achieved 84dBc which is adequate for many recent communications systems. The technique was compared with the existing ones in terms of storage, reduction computation, and spectral purity. The comparison shows significant improvement in all features.

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