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An Improvement of CMOS Voltage Reference

Abstract. *This paper presents a CMOS voltage reference design, which is widely used in electronic circuits, both analog and digital circuits. In the conventional, a CMOS voltage reference circuit design composed of several MOS transistors and complicated circuits, the output voltage cannot be adjusted to any levels. Therefore, in this paper proposed the CMOS voltage reference circuit design technique based on current combination circuit, which it was reduced number of MOS transistors and the proposed circuit is able to operate without complex startup circuit. The performance of the proposed circuit is confirmed through PSPICE simulation results, the circuit can be operated with supply voltage varies from 1.85 - 4 V, the output voltage reference is about 500±2.5 mV at wide temperature range of -58 °C to 120 °C, it has very low temperature coefficient of about 61.19 ppm/°C, and low power dissipation is 5.51 µW.*

Streszczenie. *W artykule opisano ulepszone źródło napięcia wzorcowego w technologii CMOS. W ulepszonej technologii wykorzystuje siemniej tranzystorów a możliwość ustawiania napięcia jest bardziej uniwersalna niż w typowych układach tego typu. (**Ulepszone źródło napięcia wzorcowego w technologii CMOS**)*

Keywords: Temperature compensation, CMOS, Voltage reference, Weak inversion.
Słowa kluczowe: in the case of foreign Authors in this line the Editor inserts Polish translation of keywords.

Introduction

The voltage reference circuit was developed and widely applied to electronic circuits which the stable power supply voltage requirement for proper circuit operations such as A/D and D/A converter, DRAM Flash memories, PLLs and others[1-3]. The low-power and low-voltage operations are widely used for portable devices, biomedical sensor and also included shopping intelligence tool in superstore [4-6]. The output voltage of generators are designed with low sensitivity to temperature, fabrication process and power supply variations. The CMOS voltage reference is one of generator circuit that can successfully achieve these requirements [7-9]. In the last few years, many researchers have reported the current and voltage reference circuit design technique to achieve the low temperature sensitivity and supply voltage variations [10-14]. However, conventional implementation of these circuits still composed of several MOS transistors and resistors for generating the bias current. Moreover, the above mentioned circuits are very complex and consumes a large chip area and power consumption [5-15].

Therefore, in this paper presents the CMOS voltage reference circuit design based on the new current summation technique that have opposite temperature coefficient for reference voltage generation which stablized over process, supply voltage and temperature variations and proposed circuit is able to operate without complex startup circuit which this technique was reduced number of MOS transistors and providing an accurate voltage reference for low supply voltage operations.

Principle of voltage reference circuit

The working principle of a voltage reference propose two parts of the circuit as shown in Fig.1. The first circuit is generated the voltage with a negative temperature coefficient of about -2 mV/°C, is called complementary to absolute temperature (V_{CTAT}) and the other circuit is generated the voltage with a positive temperature coefficient of about 0.086 mV/°C, is multiplied by gain K which has proportional to absolute temperature(V_{PTAT}).

The reference voltage generator is summed of CTAT and PTAT currents to generate a reference current (I_{ref}) which is employed for generating the reference voltage (V_{ref}), can be expressed as

$$V_{ref} = (I_{CTAT} + KI_{PTAT})R_{ref} \tag{1}$$

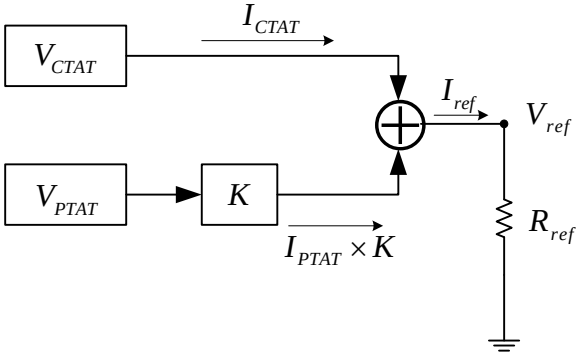

Fig.1. block diagram of a voltage reference circuit

The temperature compensation for reference voltage, the following condition must be achieved a zero-temperature coefficient [3, 8].

$$\frac{\partial V_{ref}}{\partial T} = 0 \tag{2}$$

The voltage reference with a temperature coefficient (TC) is formed by the min/max limits for the nominal output voltage over the operating temperature range is defined as follows.

$$TC = \frac{1}{V_{atroomtemp}}\left[\frac{V_{\max} - V_{\min}}{T_{\max} - T_{\min}}\right].10^6 \; ppm/°C \tag{3}$$

The voltage reference circuit exhibits a TC limit typically between 20 to 100 ppm/°C [16].

Purposed CMOS Voltage Reference circuit

The circuit configuration of CMOS voltage reference is shown in Fig. 2 can be divided into three parts. The first part is composed of transistors *M1*, *M3* and *R1* for generating the current with negative temperature coefficient (I_{CTAT}), second part is composed of transistors *M2* and *R2* for generating the current with a positive temperature

coefficient (I_{PTAT}) and the last part is current mirror circuit which is consisted of transistors *M4*, *M5* and *M6*. The *M4* is defined for summing the current of I_{CTAT} and I_{PTAT} which is independent of temperature and mirrored to the *M6* for generating the voltage reference (V_{ref}).

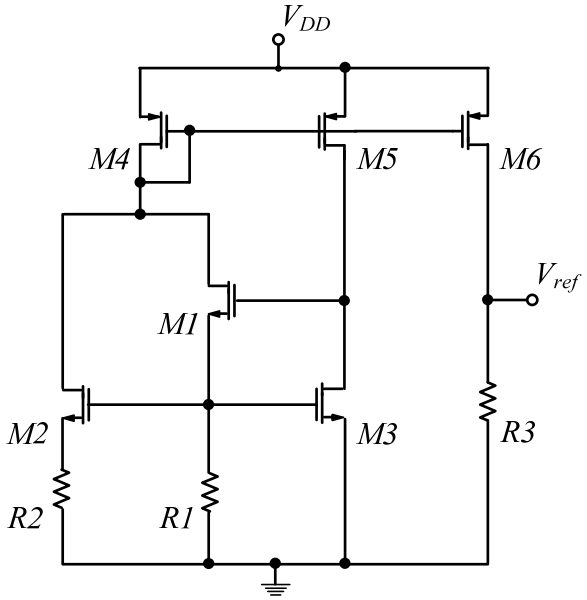

Fig.2. Proposed Voltage Reference Circuit

In the first part, the *M1* and *M3* are defined to operate in saturation and weak inversion region, respectively. Then, the drain current of *M1* and the gate-source voltage of *M3* ($V_{gs_{M3}}$) is given by

$$I_{D_{M1}} = \frac{1}{2} m_p C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \tag{4}$$

$$V_{gs_{M3}} = nV_T \ln\left[\frac{I_{ds3}.L_3}{I_t.W_3}\right] + V_{th} \tag{5}$$

Where V_T is the thermal voltage, can be written as

$$V_T = \frac{kT}{q} \tag{6}$$

Where k is the Boltzmann's constant *(1.38 x10^{-23} J/K)*, q is electric charge *(1.6 x10^{-19} C)* and T is absolute temperature. The drain current of *M3* is expressed in term of exponential can be expressed as

$$I_{ds3} = I_t \frac{W_3}{L_3} e^{\frac{q(V_{gs_{M3}} - V_{th})}{nkT}} \tag{7}$$

Where V_{th} is the threshold voltage, W_3 and L_3 is channel width and channel length of MOS transistor, respectively.

$$I_t = 2nm_n C_{ox} \left(\frac{kT}{q}\right)^2 \tag{8}$$

Where I_t is the saturation current of the MOS transistor, n is the slope factor, C_{ox} is the gate oxide capacitance per unit area and μ is the electron mobility,

Substituting equation (6), (7) and (8) into (5), then differentiation can be written as

$$\frac{\partial V_{gs_{M3}}}{\partial T} = \frac{V_{gs_{M3}}}{T} - 2n\frac{k}{q} \tag{9}$$

From eq. (9) found that, when increasing temperature the V_{gs} of MOS transistor *M3* will be decreased which is called V_{CTAT} and the I_{CTAT} is expressed by.

$$I_{CTAT} = \frac{V_{gs_{M3}}}{R1} \tag{10}$$

In the second part, from the circuit as shown in fig. 2 the *M2* is defined to operate in weak inversion region and V_{R1} is equaled to $V_{GS2} + V_{R2}$. So the voltage drop across *R2* can be written as

$$V_{R2} = nV_T \ln m \tag{11}$$

Where m is aspect ratio of MOS transistors *M2* and *M3*, and I_{R2} is proportional to V_T , can be written as

$$I_{PTAT} = I_{R2} = \frac{nkT}{R2q} \ln m \tag{12}$$

From equation (12), found that the current I_{R2} has a positive temperature coefficient; it's clearly seen that when increasing temperature, the current I_{R2} will be increased.

In the last part, the current mirror circuit is composed of transistors *M4*, *M5* and *M6*. The MOS transister *M4* is defined for summing the current of I_{CTAT} and I_{PTAT} which is independent of temperature, can be expressed as

$$I_{ref} = I_{CTAT} + I_{PTAT} \tag{13}$$

By substituting (10) and (12) into (13) can be obtained

$$I_{ref} = \frac{V_{gs_{M3}}}{R1} + \frac{nV_T}{R2} \ln m \tag{14}$$

The current I_{ref} is mirrored from *M4* to *M6*, then the reference voltage can be obtained as follow.

$$V_{ref} = I_{ref} R3 \tag{15}$$

The output reference voltage can be achieved the low temperature coefficient and set at any level by changing the resistance value of *R3*.

Table 1. The parameters of transistors and resistors

Transistors	*W/L*(μm/μm)
M1	10 / 5
M2-M3	50 / 5
M4-M5	5 / 5
M6	10 / 5
Aspect Ration *M2*/*M3*	15/1
Resistors	($K\Omega$)
R1	1400
R2	230
R3	544

Simulation results

The simulation results of the proposed voltage reference circuit are verified by PSPICE in a 0.5 μm standard CMOS technology. The device parameters of MOS transistors and the resistors are shown in Table 1, Fig.2. shows the output reference voltage of about 500 mV under temperature variations from -58°C to 120°C and voltage variation less than 2.5 mV, the temperature coefficient is 61.19 ppm/°C and the power dissipation is only 5.51 μW at the supply voltage V_{DD} = 2.0 V.

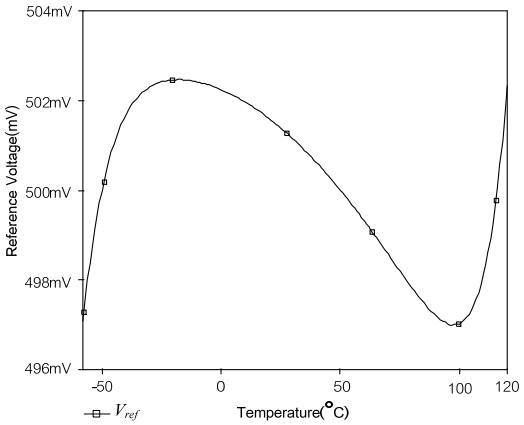

Fig.2. Temperature independence of the voltage reference

Fig.3. shows the currents I_{CTAT} and I_{PTAT} which has negative and positive temperature coefficient, respectively, after that both currents will be summed by *M4*, then mirrored to *M6* to produce I_{ref} and flow through a resistor (*R3*) to create the V_{ref} .

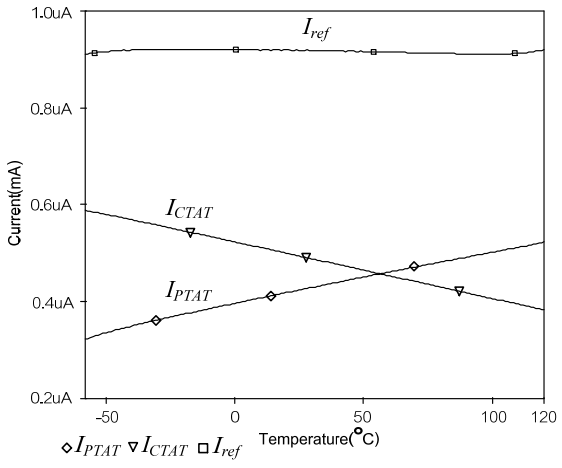

Fig.3. The currents I_{CTAT} , I_{PTAT} and I_{ref} as function of temperature

Fig.4. shows the reference voltage as a function of supply voltage, which can be successfully operated from 1.85 V to 4.0 V, the reference voltage is set of about 500 mV and voltage variation is about 2.5 mV/V. at room temperature.

As shown in Fig. 5, the reference voltage dependence of the supply voltage range is changed from 2.0 to 3.5 V and different temperatures (-30, 30 and 120°C), the line regulation of the reference voltage is about 3.0 mV/V at room temperature.

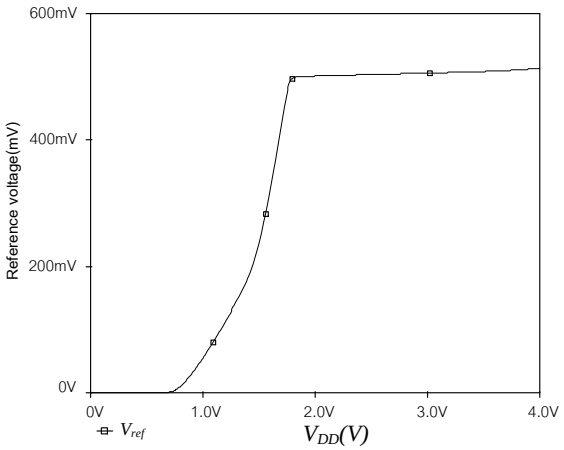

Fig.4. Reference voltage as a function of supply voltage

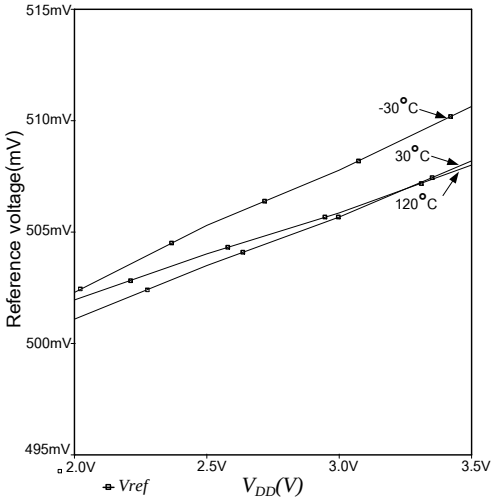

Fig.5. Reference voltage versus supply voltage variations and under different temperatures

Conclusion

An improvement of CMOS voltage reference circuit with new technique for current combination circuit which has negative and positive temperature coefficient without startup circuit, this methodology can be reduced the number of MOS transistors, chip area and low power consumption.

The results of simulation for the proposed circuit is shown that the reference voltage is very stable for a wide range of temperature and supply voltage variations.

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