Djurdje PERIŠIĆ[1], Aleksandar ŽORIĆ[2], Djordje BABIĆ[1], Djordje PERIŠIĆ[1]

Slobomir P University-Bosnia and Herzegovina (1), Faculty of Technical Science in Kosovska Mitrovica-Serbia (2)

Recursive PLL of the First Order

Abstract. *This paper describes a new type of Recursive Phase Locked Loop (PLL) of the first order. The PLL is a linear discrete system described by two recursive equations. The hardware implementation of PLL is described. Different analyses of PLL parameters are made. Computer simulation of PLL is introduced in order to give better insight into the PLL characteristics and to confirm the mathematical analyses, too. Made analysis shows that PLL is suitable for different applications. Precise digital phase shifting of pulse rate is one of the applications which is described. The picture of the input and output pulse rates, recorded on the simulated PLL by professional software package "Multisim", is presented.*

Streszczenie. *Opisano nowy typ rekurencyjnej pętli synchronizacji fazowej (PLL). Przedstawiono różne metody analizy układu oraz symulację komputerową. Opisano możliwość precyzyjnego cyfrowego przesunięcia fazowego impulsów. (**Rekursyjna pętla synchronizacji fazowej PLL pierwszego rzędu**).*

Keywords: Phase Locked Loop, Discrete linear system, Recursive algorithm.
Słowa kluczowe: układ PLL, rekursyjna pętla fazowa PLL.

Introduction

Different kinds of PLL are described in theory and practice and different kind of division of PLL can be made. Some earlier systematizations of PLL identified analog, hybrid, discrete and digital kinds of PLL. Although convenient in usage, this division was not precise enough because these groups were made according to different criterions. For instance, analog and hybrid PLL were defined according to the applied technology. Analog PLL are based on analog circuits, but hybrid ones use both analog and digital circuits. Discrete PLL represent discrete systems. They were separated in the independent group due to their principle of work. Namely, they make one correction of the output signal at each discrete time, i.e. once per period of the input signal. All the others PLL belonged to the digital ones, although the discrete PLL are also based on digital circuits.

The division of PLL could be more precise if the divisions are made upon more criterions. For instance the systematization of PLL according to the measured error between the input and output signal, which is used for the output correction, would be useful. The error may be generated by measuring the phase, the amplitude, the frequency and by measuring the time. The first ones are the classic PLL and they appear the most often in theory and practice. PLL based on the measurement of amplitude require a lot of hardware and they are not precise enough. PLL which are based on integration of difference between the input and output frequencies are useful for special applications, ref. [1-2]. PLL which are based on either the measurement of the time difference between the input and output signal or the measurement and comparison of theirs periods, are just somewhat presented in the literature. On the other hand, the measurement of the time is the most easy for the realization and the most precise today. Obviously, the corresponding algorithms for the processing of time error are not investigated. These algorithms are to be simple for realizations. They have to enable, at the same time, wide range of applications and to be potential for different output controls. Providing that the mentioned requirements have been met, this kind of PLL would appear as more powerful and more applicable than the previous ones.

The recursive models of PLL, offer algorithms that can perform PLL function and digital filtering at the same time. They appear as simple for realization and powerful for the applications.

This paper describes a new type of recursive PLL of the first order, based on the measurement of the time difference between the input and output signals.

The development of PLL of the first order is closely related to ref. [1-2]. Ref. (3-10) are also in the field of PLL and represent the wider base of literature. Ref. [11-15] are used in electronics implementation and as the mathematical and theoretical base in the development.

Mathematical description of PLL

One general case of the time relation between an input signal Sin and the output signal Sop of PLL, is shown in Fig. 1. Note that the classical phase difference between the input and the output signal is changed by discrete time differences. The periods TI_0, TI_1,….TI_k, TI_{k+1}, and TO_0, TO_1,….TO_k, TO_{k+1}, as well as the time differences d_0, d_1, d_2…..d_k, d_{k+1}, occur at discrete times respectively t_0, t_1, t_2,…..t_k, t_{k+1}. The discrete times t_0, t_1, t_2,…..t_k, t_{k+1} are defined by the falling edges of the pulses of Sop in Fig. 1.

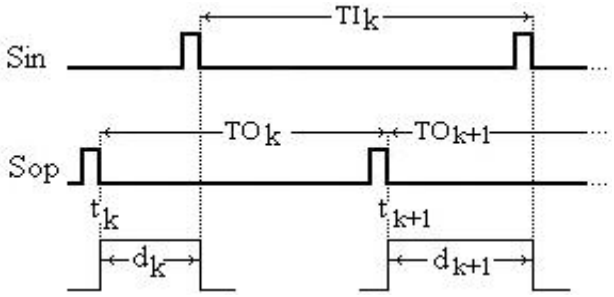

Fig. 1 The variables describing the input and the output of PLL

The natural recursive relation (1) between the variables, yields from Fig. 1:

(1) $$d_{k+1} = d_k + TI_k - TO_k$$

The main recursive equation describing PLL is given by the expression (2):

(2) $$TO_{k+1} = T + d_{k+1} * m$$

where T is the time constant and "m" is the parameter of PLL. The physical meaning of T and "m" will be explained in the part, which describes the realization of PLL. According to eq. (1) and (2), PLL has two output variables, which describe the behavior of PLL in the function of TI. The output variables are d(k+1) = f[TI(k)] and TO(k+1) = f[TI(k)].

To analyze the conditions under which the described system possesses the properties of PLL, let us find the Z transform of eq. respectively (1) and (2):

(3) $$z*d(z)-z*d_0=d(z)+TI(z)-TO(z)$$

(4) $$z*TO(z)-z*TO_0=TI*z/(z-1)+\\ +\left[z*d(z)-z*d_0\right]*m$$

Calculating d(z) from eq. (3) and changing it into eq. (4), it can be found out:

(5) $$TO(z)=[m*TI(z)+R(z)]/(z-1+m)$$

where

(6) $$R(z)=d_0*m*z+(z-1)*(TO_0+d_0*m)+T$$

In the same way, changing TO(z) from eq. (5) to eq. (3), it can be calculated:

(7) $$d(z)=TI(z)/(z-1+m)-\\ -R(z)/[(z-1)*(z-1+m)]+d_0*z/(z-1)$$

Two transfer functions describing PLL, can be defined from respectively eq. (5) and eq. (7):

(8) $$H_{TO}(z)=TO(z)/TI(z)=m/(z-1+m)$$

(9) $$H_d(z)=d(z)/TI(z)=1/(z-1+m)$$

Step Analysis of PLL

Providing that the step function is applied to the input TI(k) = TI = const., it is necessary to change the Z transform TI(z) = TI*z/(z-1) into eq. (5) and eq. (7). Changing TI(z) into eq. (5) and using the final value theorem, it is possible to find the final value of the output period TO_∞ = lim TO(k) if $k\to\infty$, using TO(z):

(10) $$TO_\infty=\lim[(z-1)*TO(z)]_{z\to1}$$

Applying eq. (10), it yields:

(11) $$TO_\infty=\lim[TO(k)]_{k\to\infty}=TI$$

Note that, instead of the output frequency, the output period TO(k) is used in this analyses. Since the phase difference between Sin and Sop is also changed by the time difference d(k) in this analyses, it is necessary to discover the behavior of d(k). If TI(z) is changed into eq. (7), using the final value theorem in the same way like for TO_∞, it yields:

(12) $$d_\infty=\lim d(k)_{k\to\infty}=\lim[(z-1)*d(z)]_{z\to1}$$

Applying eq. (12), it yields:

(13) $$d_\infty=(TI-T)/m$$

The expressions (11) and (13) are valued only if PLL is the stable system i.e. if the pole $|z_1| < 1$, where z_1 is the pole of the transfer function $H_{TO}(z)$ or $H_d(z)$. Since $z_1 = 1 - m$, it yields that PLL is stable system for

(14) $$0<m<2$$

According to eq. (11) and (13), it follows that the described model possesses the properties of PLL. The time d_∞, representing the time difference for the stable PLL, does not depend on the initial conditions and it can be controlled by the system parameter "m" and time constant T. Time constant T is entered into PLL and can be changed accordingly. If, for instance, m = 1, d_∞ = TI – T. This means that it is possible to change the time difference "d" linearly, directly by changing T. If T = TI, d_∞ = 0, the phase difference is zero, what is exactly the same as in conventional PLL.

.

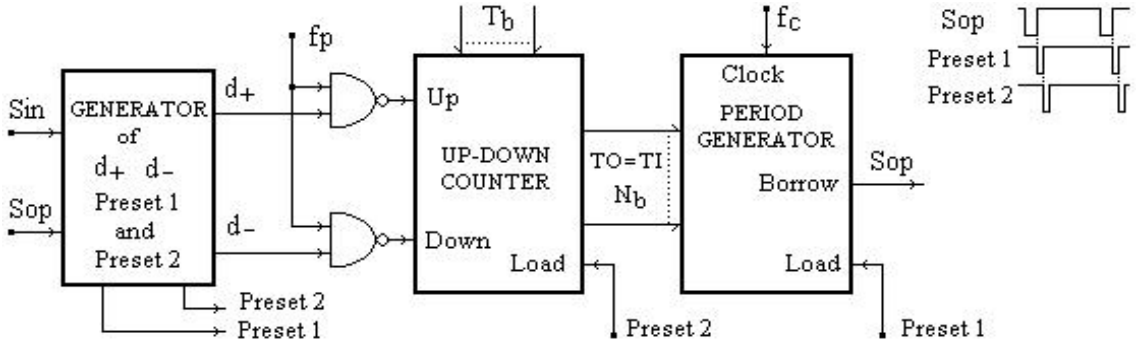

Fig. 2 The functional organization of hardware modules of PLL

Realization of PLL

The hardware organization of PLL is shown in Fig. 2. PLL consists of Up-down counter, period generator, generator of control signals and two logic circuits NAND. The functioning of the period generator is described in ref. [2]. Let us remember that the period generator is based on Up-down counters and that TO of signal Sop is TO = $N_d*t_cN_d$ is the decimal value of binary code N_b and t_c is the period of clock, i.e. $t_c = 1/f_c$. Two clock signals Sc and Sp are used in the realization of PLL shown in Fig. 2. Note that the clock signals Sc and Sp are changed in Fig. 2 by their frequencies respectively f_c and f_p intentionally, because f_c and f_p are PLL parameters, which will appear in the final expressions for the outputs of PLL. To explain this statement, let us transform eq. (2) in another form, which is more suitable for the realization of PLL and understanding the physical role of frequencies f_c and f_p in Fig. 2. If "m", as ordinary number, is changed with $m = f_p/f_c$ in eq. (2), eq. (2) will, after transformation, get the following form:

(15) $$TO_{k+1}*f_c=T*f_c+d_{k+1}*f_p$$

The eq. (15) discovers now how to perform calculation according to eq. (2). All members of eq. (15) are just ordinary number, since $f_c = 1/t_c$ and $f_p = 1/t_p$. It is now clear that, according to eq. (15), TO is to be generated by the period generator using clock of frequency f_c, binary word T_b must be converted into time T using f_c as well, and d_{k+1} is to

be measured by the clock of frequency f_p. All these conclusions are applied in the realization of PLL, shown in Fig. 2.

The generator of control signals d_+, d_-, Preset 1 and Preset 2, according to its function in PLL, changes the role of a comparator in a standard analog PLL. The relation between Preset 1, Preset 2 and Sop is shown in Fig. 2. Their realization is simply. They are realized by two monostable multivibrators. They could also be realized by two RC differentiators. However, since the time difference "d" can be positive d_+ and negative d_- as well, it was necessary to generate them on separate lines and to provide either addition or subtraction, just like in Fig. 2. The time difference d_+ is always added to T_b, but the time difference d_- is subtracted from T_b in Up-down counter.

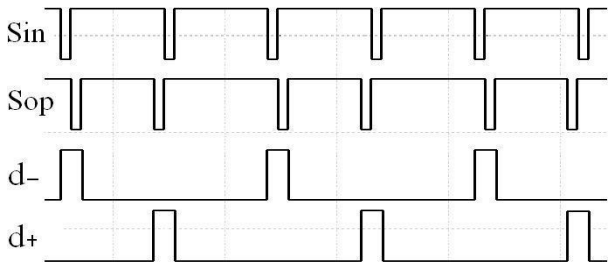

Fig. 3 Generation of Sop (eq. 2), d- and d_+ are visible.

The functioning of generator and PLL is presented in Fig. 3. The picture is made on the simulated PLL, realized by the profesional software package for electronic circuits „Multisim„. The voltage waveforms in Fig. 3 are taken whenPLL is in the stable state. For this purpose, it was chosen $f_c = f_p$ (m = 1). Binary word T_b is chosen so that its decimal value $T_d * t_c = T \approx TI$. According to eq. (13), $d_\infty = TI - T \approx 0$. TI/t_c is only about 6. Small relation between TI and t_c is chosen to enable the visible width of d_+ and d_-. The difference between the adjacent periods TO is visible, too. The sign of "d" is changing every period. It can be noticed from Fig 3 that TO tends to reach TI, but that is not possible, because the relation TI/tc is very small. It can also be seen that whenever two pulses of Sop occur during a period TI, that means that the TI > TO, "d" is positive and next TO is increased. If two pulses of Sin comes during a period TO, that means that TO > TI, "d" is negative and next TO is decreased. If during one period TO occur only one pulse of Sin, the time difference will not change sign. The same would happen if only one pulse of Sop occur during one period of Sin. The previous explanations represent, at the same time, the complete description of functioning of generator. If TI/t_c increases, the wides of d_+ and d- would decrease and tend to zero. For the stable PLL the content of UP-down counter represents the measured TI and, at the same time, the output period TO, since TO = TI.

Pulses Preset 1 and Preset 2, shown in Fig. 2, provide the functioning according to eq. (2). As soon as the calculation of TO is finished, pulse Preset 1 presets the counter content to the period generator. Immediately after that, pulse Preset 2 presets T_b into counter. The next step is the generation of new period TO and at the same time calculation with the next time difference "d" multiplied by "m", according to eq. 2.

Simulation of PLL outputs for different parameter "m"

The simulation of PLL functioning is performed using equations (1) and (2). The time difference d(k) and the output period TO(k) are simulated for the same parameters "m" and the same initial conditions. The simulation results, for the different value of "m", are shown in Fig. 4. The input period is 10 time units (t.u.), T is 1 t.u. and the initial values of TO_0 and d_0 are respectively 8.5 t.u. and 4 t.u. Note that time unit can be any one, assuming that they are the same for all variables. The simulated d_∞ in Fig 4a agrees with d_∞ calculated by eq. (13), proving the correctness of the math analyses. It can be seen that $TO_\infty = \lim TO(k)_{k\to\infty} = TI$ in Fig. 4b, for any "m". Note that TO_∞ and d_∞ do not depend on the initial conditions and that d_∞ can be controlled by the system parameter "m" and time constant T.

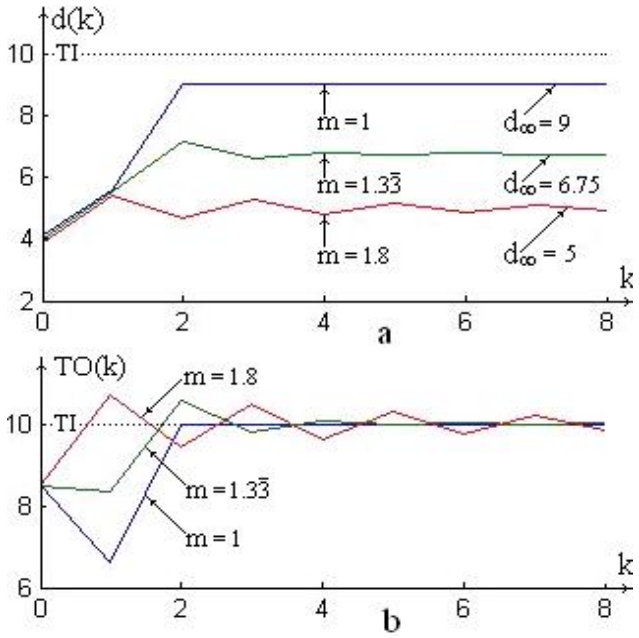

Fig. 4 The curves of d(k) and TO(k) for different parameter „m"

The phase shifting

Using the results of this analysis, it is simple to determine the expresion for the phase shifting PS of pulses of Sop. The final phase shifting PS_∞ is simply $PS_\infty = 2\pi * d_\infty / TO_\infty$. Changing d_∞ and TO_∞ from eq. (11) and (13), it yealds:

$$PS_\infty = 2\pi * [(TI - T)/TI] * (f_c / f_p) rad \quad (16)$$

Changing $m = f_p / f_c$ into eq. (16), it follows:

$$PS_\infty = 2\pi * [(TI - T)/TI] * (f_c / f_p) rad \quad (17)$$

If $f_c = f_p$, eq. (17) will change to:

$$PS_\infty = 2\pi * (1 - T/TI) rad \quad (18)$$

According to eq. (16), the phase shifting can be performed either by parameter "m" or by parameter T. However it is more convenient to adopt m = 1, and use the eq. (18) for this purpose. If the parameter T changes in range from zero to TI in eq. (18), PS will cover the value from 2π rad to zero. PS can also reach negative values for T > TI.

Using eq. (1), eq. (2) and the expression PS(k) = d(k)/TO(k), the locking procedure of TO(k), the time difference d(k) and the phase shifting PS(k) are calculated and presented in Fig. 5. TO(k), d(k) and PS(k) are simulated for m = 1, TI = 10 t.u. = constant and for the different values of parameter T, which are presented in Fig. 5. The initial conditions for all variables in Fig. 5a, Fig. 5b and Fig. 5c are the same: $TO_0 = 9.5$ t.u., $d_0 = 4$ t.u. and $PS_0 = 2\pi * d_0 / TO_0 = 2.65$ rad. Note that PLL is very fast if

parameter m = 1, Fig. 5a, Fig. 5b and Fig. 5c. All transient states are finished within two steps. The same can be noticed in Fig. 4a and Fig. 4b for those curves for which the parameter m = 1.

The values for time shifting d_∞ in Fig. 5b are calculated according to eq. (13) and the values for phase shifting PS_∞ in Fig. 5c are calculated using eq. (18). All calculated values agree with the simulated ones in Fig. 5b and Fig. 5c, what is the proof that the mathematical analyses were correct.

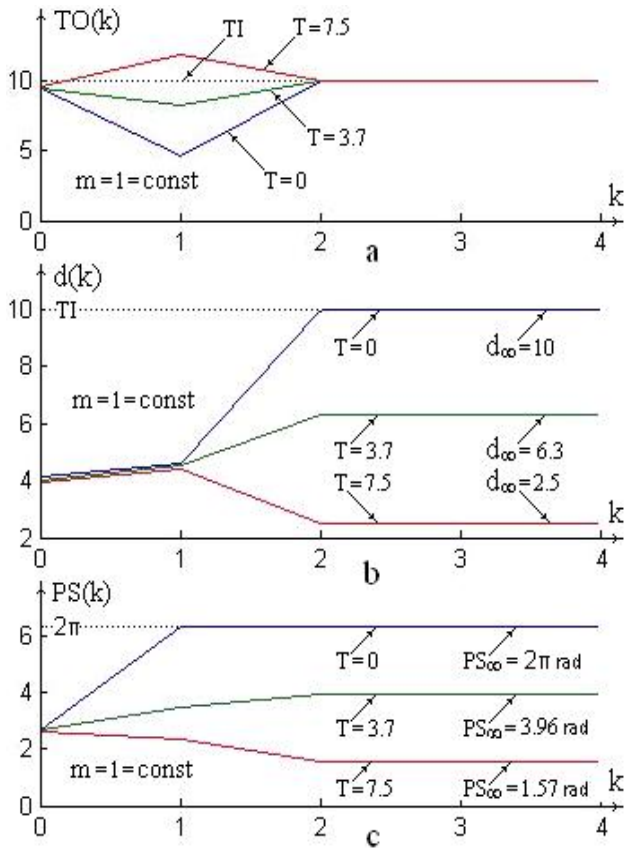

Fig. 5 Presentation of TO(k), d(k) and PS(k) for different „T"

Conclusion

The description and illustrations of the realized PLL of the first order represent a new approach to design and construction of PLL in both theoretical and practical sense. It discovers the way of development of PLL based on measurement of time, which is more precise and convenient than the measurement of the phase, the frequency, and the amplitude.

The Z transform analyses of the described algorithm provide a detailed insight into the physical process of all PLL variables and in each discrete step.

One of possible application of PLL is the phase shifting of pulse rate, which is described in the paper. The precision of the phase shifting can be very high, because it depends on relation TO/t_c. The higher relation TO/t_c provides the higher resolution of shifting.

Since the described PLL represents a new type of PLL, further analysis of its properties would be useful in order to expand the area of its application.

Acknowledgement

This article was supported by the Ministry of Science and Technology of the Republic of Serbia under the projects III47016 and TR 32023.

REFERENCES

[1] Dj. M. Perišić, A. Zorić, S. Obradović, Dj. Dj. Perišić, FLL as Digital Synthesizer based on Binary Rate Multiplier Control, Electrical Review, ISSN 0033-2097, R.89 NR 1a/2013, Page 145-148.

[2] Dj. Perišić, A. Žorić, S. Obradović, P. Spalević, Application of Frequency Locked Loop in Consumption Peak Load Control, Electrical Review, ISSN 0033-2097, R.88 NR 1b/2012, Page 264-267.

[3] R. N. Dean, A. K. Rane, A Digital Frequency-Locked Loop System for Capacitance Measurement, IEEE Trans. On Instrumentation and Measurement, Vol. 62, Issue 4, 2013 Page 777-784.

[4] J. T. Curran, G. Lachapelle, C. Murphy, Improving the Design of Frequency Locked Loops for GMS Receivers, IEEE Trans. on Aerospace and Electronic Systems, Vol. 48 Nr. 1, 2001, Page 850-868.

[5] X. Q. Guo, W. Y. Wu, H. R. Gu, Phase Locked Loop and Simulation Methods for Gridinterfaced Converters: A Review, Electrical Review, ISSN 0033-2097, 4/2011, Page 182-187.

[6] A. M. Raičević, B. M. Popović, PLL as the Frequency Synthesizer with Continuous Phase Divider, Electronics and Electrical Engineering - Kaunas: Technologija, 2009, No. 5(93), pp. 47–50, No. 5(93), Page 47–50.

[7] C. C. Chung, An all-digital phase-locked loop for high speed clock generation, IEEE Journal of Solid-State Circuits, 2003, Vol. 38, Issue 2, Page 347-359.

[8] D. Jovcic, Phase locked loop system for FACTS, IEEE Transaction on Power System, August 2003, Vol. 18, Page 2185-2192.

[9] D. Abramovitch, Phase-locked loops: a control centric tutorial, Amecan Control Conference-2002, Procedings of 2002, 2002, Vol 1, Page 1-15.

[10] Giovani Bianchi, "Phase-Locked Loop Synthesizer Simulation", Nc-Hill, Inc. New York, USA, 2005.

[11] Roland E. Best, Phase Locked Loops, Mc Graw Hill, ISBN 0-07-141201-8, 2003, P. 421.

[12] Vich R (1987-first edition). Z Transform Theory and Application (Mathematics and Applications), Ed. Springer.

[13] Gardner F. M., "Phaselock tecniques", Hoboken, Wiley-Interscience, 2005.

[14] A. Agarwal, J. Lang, Foundation of Analog and Digital Electronic Circuit, Denise E. M. Penrose, San Francisko, USA, 2005, P. 984.

[15] D. B. Talbot, Frequency Acquisition Techniques for Phase Locked Loops, Wiley-IEEE Press, 2012, P. 224.

***Authors**: prof. dr Đurđe Perišić, Faculty of Information Technologies, str. Pavlovića put bb. 76300 Slobomir, Bosnia and Herzegovina, E-mail: djurdje@beotel.rs ; prof. dr Aleksandar Č. Žorić, Faculty of Technical Science, str. Kneza Miloša 7, Kosovska Mitrovica, Serbia, E-mail: aczoric@yahoo.com; prof. dr Djordje Babić, Faculty of Information Technologies, str. Pavlovića put bb. 76300 Slobomir, Bosnia and Herzegovina, E-mail: djordje.babic@spu.ba; Djordje Perišić, Faculty of Information Technologies, str. Pavlovića put bb. 76300 Slobomir, Bosnia and Herzegovina, E-mail: djoleusa@yahoo.com .*