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FPGA Based Implementation of Amplitude Modulated Triangular Carrier PWM

Abstract: *The amplitude modulated triangular carrier pulse width modulation method (AMTCPWM) is a natural sampled PWM method which can extend the linearity of the sinusoidal PWM (SPWM) to full range of the pulse dropping region and increase the dynamic range of the SPWM control. Any submission in the PWM theory with a specific performance target is mandatorily requires either a reference or a carrier modification. This paper presents a reprogrammable architecture to implement the AMTCPWM with perfect reproduction capability. The architecture is implemented using Spartan 6 family device LX45 using Modelsim 6.3 and Xilinx 13.2i.*

Streszczenie. *Metoda modulacji amplitudowej fali nośnej trójkątnej AMTCPWM umożliwia rozszerzenie możliwości klasycznej metody sinusoidalnej PWM SPWM. W pracy zaprezentowano wykorzystanie układów FPGA. (**System PWM z modulacja fali trójkątnej wykorzystujący układy FPGA**)*

Keywords: Voltage source inverter, voltage gain linearization, amplitude modulated triangular carrier PWM, FPGA
Słowa kluczowe: przekształtnik napięciowy, układ PWM, układy FPGA

Introduction

Switching power converters are designed to convert electrical power from one form to another with high efficiency [1]. The function of a voltage source inverter (VSI) is to convert a fixed dc voltage into a variable voltage and variable frequency ac voltage [2]. An interesting feature of power electronic circuits is that, depending on the application, the basic circuit topology can be modified with additional elements or used with different control methods that provide additional functionality or work better with the same functionality [3]-[7]. PWM techniques change the frequency spectrum of the VSI's output voltage such that major non-fundamental components are at relatively high frequency.

Traditional natural sampling techniques rely on analog circuits, where a fixed triangular carrier waveform is compared to a variable magnitude and frequency sinusoidal reference waveform. The intersection point determines the switching waveform. Digital platforms offer improvements over their analog counterparts. They are immune to noise and are less susceptible to voltage and temperature changes. Development of the high performance microprocessor has encouraged the digital implementation of PWM methods [8]. Generating PWM signals requires a high sampling rate in order to achieve a wide bandwidth performance. Most computation resources of the processor are used for generating PWM signals. Field programmable gate array (FPGA) is a programmable logic device (PLD) developed by Xilinx® Inc. comprising thousands of logic gates. Some of them are combined to form a configurable logic block (CLB) [9]. A CLB simplifies higher-level circuit design. Interconnections between logic gates using software are defined through SRAM or ROM, which will provide flexibility in modifying the designed circuit without altering the hardware. Concurrent operation, less hardware, easy and fast circuit modification, comparatively low cost for complex circuitry and rapid prototyping make it the preferred choice for prototyping an application specific integrated circuit (ASIC) [10]. The main difference from DSP-based solutions is that FPGAs allow concurrent operation (simultaneous execution of all control procedures), enabling high performance and computational making the implementation of intensive control methods feasible. The advent of FPGA technology has made many computational intensive PWM strategies in reality.

Several attempts have been noticed with the motivation of perfect imitation of natural sampled SPWM in a digital platform [11]. A 16-bit microprocessor (MC68000) system has been used to generate pulse-width modulation (PWM) voltage waveforms for a three phase VSI. The features such as quarter wave symmetry, 120^0 phase differences etc. are exploited for conserve the processor time [12]. A planar transformer technology based high frequency PWM has been implemented for high power converters using FPGA and complex programmable logic Device (CPLD) ICs [13]. The low cost architecture developed is capable of developing PWM frequencies up to 3.985 MHz with a duty cycle resolution of 1.56%. A flexible, inexpensive laboratory setup that can be configured for exploring a number of power converter topologies, controlled in both open loop and closed loop has been presented. In addition to driving passive loads, the setup can be used to demonstrate DC motor torque, speed, and position control, as well as variable speed three-phase AC motor control [14]. FPGA based digital control for a power factor correction (PFC) flyback ac/dc converter has been presented [15].

The digital implementation of amplitude modulated triangular carrier pulse width modulation method (AMTCPWM) is described in this paper. The reprogrammable architecture developed is cable of imitating the AMTCPWM with perfect reproduction. The architecture is implemented using Spartan 6 family device LX45 using Modelsim 6.3 and Xilinx 13.2i. The algorithm uses the sine reference data just for a quarter wave and also does not require separate data for amplitude modulation of the carrier wave. The designed architecture could reproduce the AMTCPWM with 373mW power consumption, 100MHz frequency and 5193 slices.

AMTC PWM Method

A switching sequence for the basic single-phase full-bridge inverter, shown in Fig. 1, which consists of two switching poles, S1/S2 and S3/S4, there are 2^4=16 different possible combinations of switching. Only four of these combinations are useful for obtaining the PWM pattern across the inverter output. PWM schemes presented in this study are assumed to be synchronous PWM.

The generation of PWM patterns through modulation is just amplitude to width transformation. That is, the appropriate carrier-based PWM method programs a "per carrier cycle average output voltage" equal to the reference voltage. In the traditional unipolar sinusoidal PWM (SPWM), a triangular carrier and a sinusoidal reference are compared for generating the gating pulses.

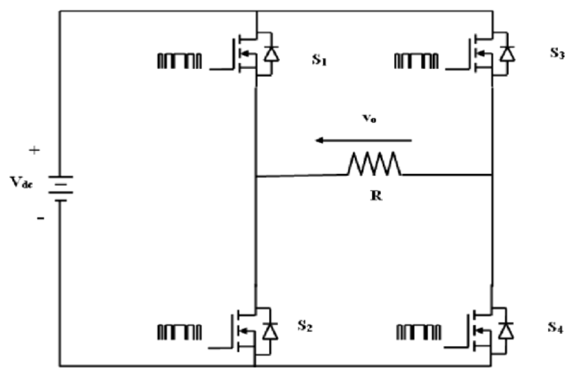

Fig.1. Single-phase voltage source inverter

In the SPWM switching strategies, fundamental improvement (particularly when dc link voltage is of finite value) demands an increase in width of pulses in the regions around the center of the reference i.e. a reduction in number of commutation by pulse dropping [16]-[17]. The reference output voltage relationship is linear until the reference voltage magnitude exceeds the modulator linearity limit and the condition is called overmodulation. When the dc link voltage of a PWM utility has a finite value, the voltage linearity of a modulator is confined to a limited voltage range, as the higher voltage values are to be obtained by increasing the inverter gain. The system loses the linearity over the fundamental as indicated in Fig.2 and introduces many more harmonics in the side bands as compared to the linear range. When the modulation index is greater than unity and the gain reduces sharply in a nonlinear manner. The modulation index approaches very large values ($\rightarrow\infty$) and the gain approaches zero. In this mode the SPWM output voltage saturates at its theoretical maximum i.e. the output of square operation, $[(4/\pi).V_{dc}]$. This value is 1.273 times the maximum possible output of linearity limit.

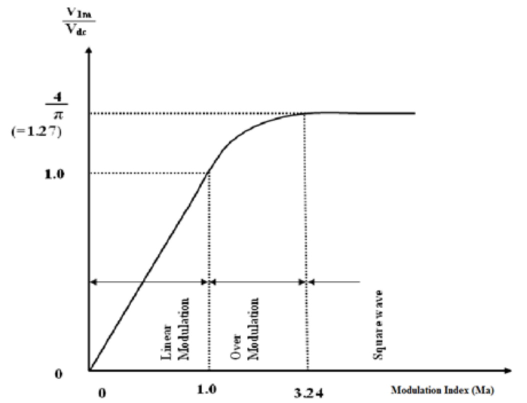

Fig.2.Modulation index versus Output voltage fundamental component

There is no simple PWM algorithm which retains voltage gain linearity until the full utilization of dc input for single-phase inverter system. The transition from PWM to square wave mode operation was an unresolved problem limiting the performance of ac drive systems. Modified regular sampled SPWM scheme named amplitude modulated triangular carrier PWM (AMTCPWM) has been developed to give single mode operation of SPWM inverter; by linearly hopping to square wave region. It also offers linear gain characteristics in comparison to the conventional SPWM without involving complex computations and significant changes in device losses. In the AMTCPWM method, the conventional sine wave remains as a reference signal while the carrier is amplitude modulated triangular signal as shown in Fig.3. The carrier is basically a high frequency triangular, which is (amplitude) modulated by a sinusoidal modulating signal of reference frequency.

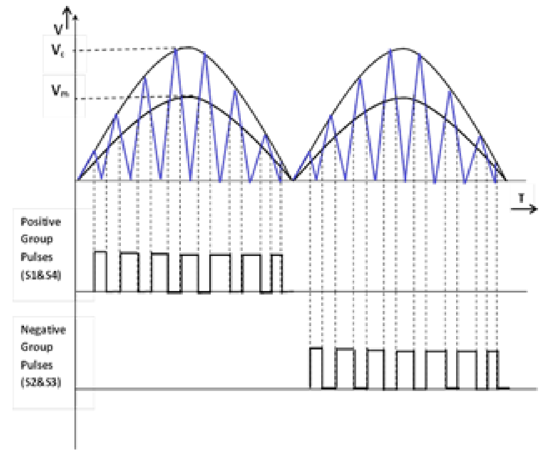

Fig.3. AMTCPWM

Fig.4 depicts the proposed architecture for implementing the AMTCPWM method. The architecture consists of sine data manipulation (SDM) unit, amplitude modulated carrier (AMC) generation unit, reference wave scaling (RWC) unit and comparator and pulse separation (CPS) unit. The SDM generates the address in sequence for fetching the sine data. The sine data for the first quarter is kept in the Look-up-table (LUT) and the data for the consequent three quarter sections can be derived through an intelligent way. The manipulated sine data is used for both reference wave and the amplitude modulation envelop. The intelligence of SDM unit helps in obtaining the sine data continuously for the complete cycle. The quarter selection is supported by the multiplexer. Based on the timed samples of the sine data the amplitude modulation of the up/down counted triangular carrier is guided by the AMC unit. RWC unit multiplies the modulation index value

with the sine data to get the required sine reference. The CPS unit compares carrier and reference waves, and produces the gating pulses for positive and negative group of devices separately. This parallel mode of execution is well detailed in Fig.5.

Table 1 describes the comprehensive digitization and approximation procedures involved in sine LUT. The clock of the architecture is derived from the internal clock of SPARTAN-6 through proper clock division method. The Xilinx Spartan-6 LX45 FPGA is used for implementation, which is 324-pin BGA package. It has 128Mbyte DDR2 with 16-bit wide data, 16Mbyte x4 SPI Flash for configuration and data storage, 100MHz CMOS oscillator and 48 I/Os routed to expansion connectors.

Table 1. Sampled sine data for LUT

Degree	Actual Data [Sin(degree*180/pi)]	Scaled-up value for 2^{10} (Rounded Value)	Binary Value
0	0	0	00000000000
1.8	0.031423398	32	00000100000
9	0.156496911	160	00010100000
34.2	0.56228207	575	01000111111
41.4	0.661529994	677	01010100101
45	0.707330278	724	01011010100
84.6	0.995617718	1019	01111111011
90	0.9999998	1023	01111111111

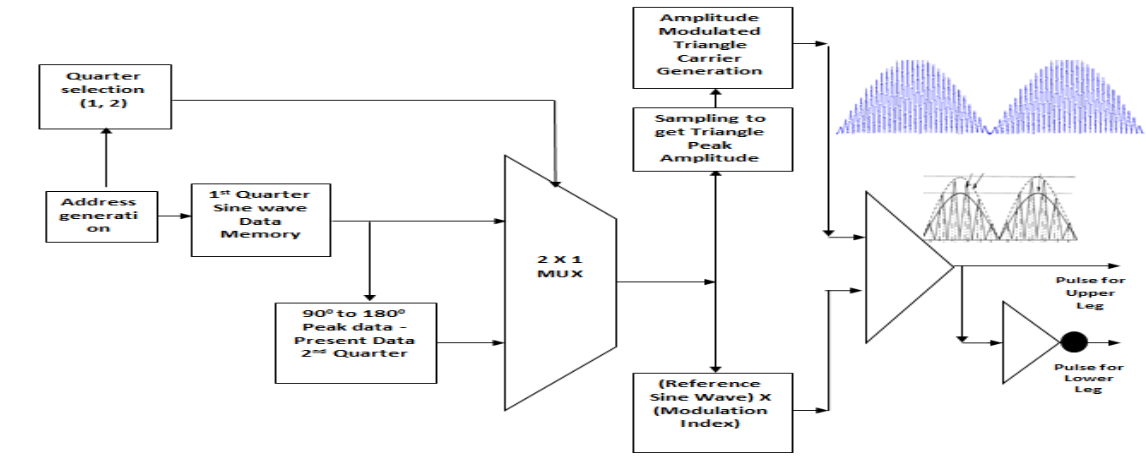

Fig.4. The proposed architecture

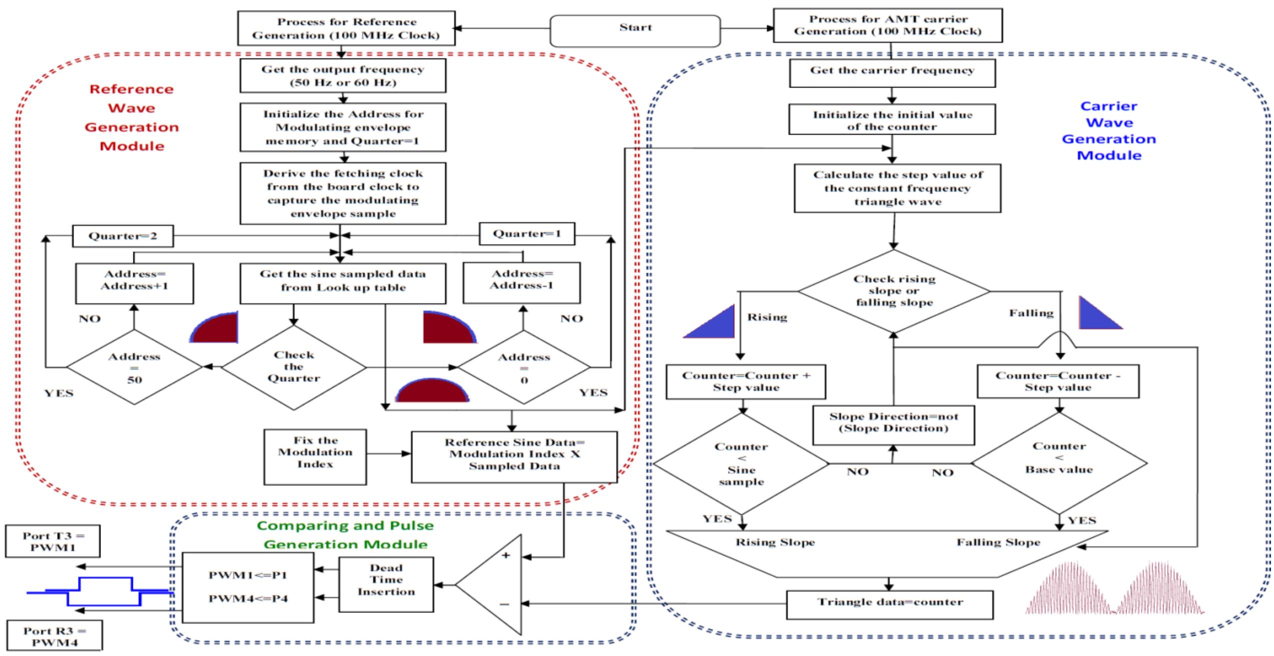

Fig.5. Parallel computational flow of the architecture

Results and Discussion

Fig.6 and Fig.7 shows the typical output voltage and corresponding spectrum of AMTCPWM at M_a=0.8, M_f=15 respectively for the V_{dc} of 300V. From the graph it is clear that the AMTCPWM scheme operates with maximum-linear gain and reaches the square wave boundary while the SPWM scheme exhibits drop in the gain after 300V. Table 2 gives the values of modulation index, THD and lower order (sub-carrier) harmonics at the output voltage (peak) level of 240V in both SPWM and AMTCPWM methods with 300V input and M_f=15. From the table, it is understood that all the lower order harmonics are increased considerably in case of AMTCPWM method.

The timing and functionality verficication based on ModelSim Simulator output is presented in Fig.8. Device utilization summary is tabulated in Fig.9. Fig.10 shows the RTL schematic view of the AMTC-PWM design obtained by Xilinx Synthesis.

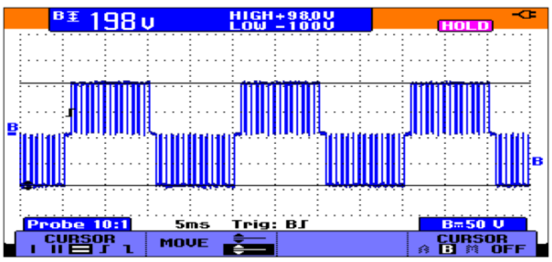

Fig.6. Output voltage waveform- AMTCPWM (Mt=0.8,Mf=15)

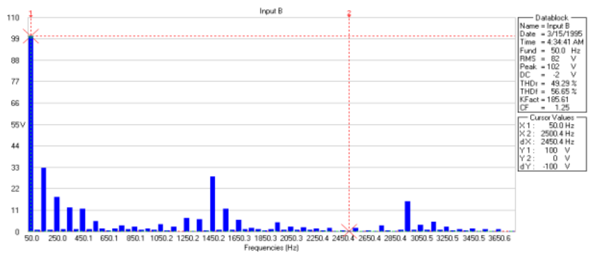

Fig.7. Harmonic Spectrum- MTCPWM (Mt=0.8, Mf=15)

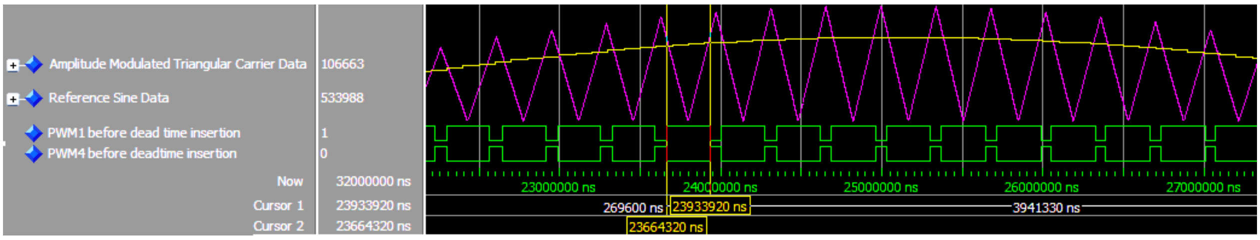

Fig.8. ModelSim Simulator output

Table 2. Comparison of SPWM and AMTCPWM

Method	M_a	THD (%)	h_3 (%)	h_5 (%)	h_7 (%)	h_9 (%)
SPWM	0.800	68.02	0.70	0.17	0.27	0.29
AMTCPWM	0.628	86.68	32.46	18.63	12.28	8.78

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	231	54576	0%
Number of Slice LUTs	460	27288	1%
Number of fully used LUT-FF pairs	185	506	36%
Number of bonded IOBs	6	218	2%
Number of BUFG/BUFGCTRLs	3	16	18%
Number of DSP48A1s	3	58	5%

Fig.9. Device utilization summary

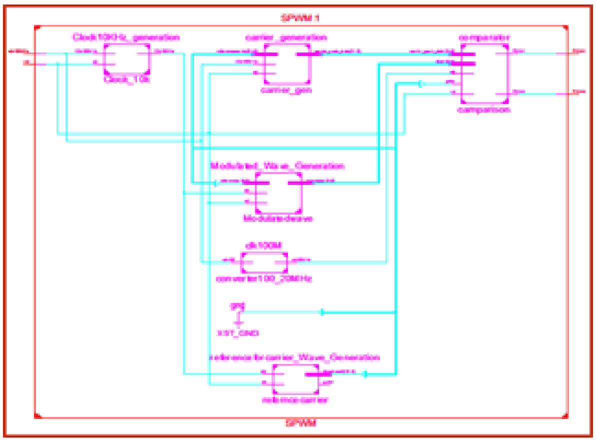

Fig.10 RTL Schematic view of the AMTC-PWM Design.

Conclusion

FPGA is a good candidate having the advantage of the flexibility of a programming solution and the efficiency of a specific architecture with a high integration density, and high speed. The heart of any inverter topology is the switching strategy used to generate the switching edges of the PWM voltage waveforms. The voltage linearity, harmonic distortion, and maximum obtainable output voltage are the prime expectation from any PWM strategy. The AMTCPWM technique provides full utilization (up to square wave region) without any pulse dropping and mode changing. The proposed architecture combines four simple units and implements the AMTCPWM with good accuracy in a reprogrammable digital platform.

REFERENCES

[1] Kassakian K.G., Schlecht M.F., Verghese G.C., Principles of Power Electronics. Reading, MA: Addison-Wesley, 1991.

[2] Bowes S.R., New sinusoidal pulse width-modulated inverter, *Proceedings of IEE*, 122(1975) No.11, 1279-1285.

[3] Mohan N., Undeland T.M., Robbins W.P., Power Electronics; Converters, Applications and Design, John Wiley, 1995, 211-218.

[4] Vikram Kaura and Vladimir Blasko, A new method to extend linearity of a sinusoidal PWM in the overmodulation region," *IEEE Transaction on Industry Applications*, 32(1996), No.5, 1115-1121.

[5] Michael A. Boost, and Phoivos D.Ziogas, State -of -Art– Carrier PWM Techniques: A Critical Evaluation," *IEEE Transactions Industry Applications*, 24(1998), No.2, 271-280.

[6] Houldsworth J.A., Grant P.A., The use of harmonic distortion to increase the output voltage of a three-phase PWM inverter," *IEEE Transactions on Industry Applications*, 20(1984), No.5, 1224-1228.

[7] Rodriguez J., Jih-Sheng Lai, Fang Zheng Peng., Multilevel inverters: a survey of topologies, controls, and applications, *IEEE Transactions on Industrial Electronics*, 49(2002) , No.4, 724–38.

[8] Mekhilef S., Rahim N.A., Omar A.M., Microprocessor implementation of three-phase PWM switching strategies", *Proceedings of the IEEE International Conference on Power Electronics and Drive System (PEDS'99)*, 1(1999) , 161-166.

[9] The programmable logic data book", Xilinx® Data Book, 1998.

[10] Monmasson E., Chapuis Y.A., Contributions of FPGAs to the control of electrical systems-A review," *IEEE Ind. Electron. Soc. Newsletter*, 49(2002), 8–15.

[11] Green and Boys J.T., Implementation of pulse width modulated inverter modulation strategies, *IEEE Trans. Ind. Appl.*,18(1982), No. 2, 138-145.

[12] Khaled E.Addoweesh, William Shepherd and Hulley L.N., Induction Motor Speed Control using a Microprocessor-based PWM inverter, *IEEE Transactions on Industrial Electronics*, 36(1989), No.4, 516-522.

[13] Eftichios Koutroulis, Apostolos Dollas, Kostas Kalaitzakis, High-frequency pulse width modulation implementation using FPGA and CPLD ICs, *Journal of Systems Architecture*, 2005.

[14] Ted K.A., Brekken and Ned Mohan, A Flexible and Inexpensive FPGA-Based Power Electronics and Drives Laboratory, *Proceedings of 37th IEEE Power Electronics Specialists Conference (PESC'06)*, 2006, 1-4.

[15] Angel de Castro, Pablo Zumel, Oscar García, Teresa Riesgo, and Javier Uceda, Concurrent and Simple Digital Controller of an AC/DC Converter With Power Factor Correction Based on an FPGA, *IEEE Transactions on Power Electronics*, 18(2003), No.1, 334-343.

[16] Holtz J., Lotzkat W., Khambadkone A., On Continuous Control of PWM Inverters in the Overmodulation Range Including the Six-Step Mode, *Proceedings of 18th Annual IEEE International Ind. Electronics Soc. Conference (IECON'92)*1992,307-312. 1992.

[17] Houldsworth J.A., Grant P.A., The use of harmonic distortion to increase the output voltage of a three-phase PWM inverter, *IEEE Transactions on Industry Applications*, 20(1984), No.5, 1224-1228.

[18] Ramkumar S., Jeevananthan S., Kamaraj V., Novel Amplitude Modulated Triangular Carrier Gain Linearization Technique for SPWM Inverter", *Serbian Journal of Electrical Engineering (SJEE)*, 6(2009), No.2, 239-252.

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