

# Modulation Algorithm for a Simplified Multilevel AC-DC-AC Converter

**Abstract.** This paper describes control and modulation algorithm of an interesting new 3-level AC-DC-AC converter topology which is based on well known Neutral Point Clamped (NPC) converter. Main advantage of this approach allows single 3-phase, 3-level converter to be utilized as a full interface between Permanent Magnet Synchronous Generator (PMSG) and the single-phase grid. Study of modulation methods for proposed converter are supported by the simulation. The AC-DC converter is controlled with regard of Field Oriented Control (FOC) principle. The current control of the DC-AC converter is based on the P+Multi-Resonant controller and Second Order Generalized Integrator Phase Locked Loop (SOGI-PLL). The multi resonant structure allows a proper operation of voltage source converter under non-ideal grid voltage. Article describes semiconductor voltage drop and dead time compensation of their influences on converter's current waveforms. Theoretical background is given.

**Streszczenie.** Artykuł opisuje algorytm sterowania i modulacji dla przekształtnika z diodami poziomującymi ze zmniejszoną liczbą łączników. Omówione zostały problemy kompensacji wpływu spadków napięć dla tego typu przekształtników. Przedstawiono wyniki badań symulacyjnych trójfazowego przekształtnika AC-DC-AC z diodami poziomującymi. Opisano wpływ czasu martwego oraz spadków napięć na złączach elementów półprzewodnikowych a także metody ich kompensacji. Przeznaczeniem układu przekształtnika złożonego z 12 tranzystorów IGBT jest przetwarzanie energii produkowanej przez generator z magnesami trwałymi (PMSG). Do sterowania generatora przez przekształtnik AC-DC wykorzystano algorytm polowo-zorientowany. Sterowanie przekształtnikiem od strony sieci elektroenergetycznej bazuje na regulatorze proporcjonalno-multirezonansowym. (Algorytm modulacji dla wielopoziomowego przekształtnika AC-DC-AC o zredukowanej liczbie łączników.)

**Keywords:** NPC, dead time compensation, voltage drop compensation, component-minimized

**Słowa kluczowe:** przekształtnik z diodami poziomującymi, kompensacja wpływu spadków napięć, zmniejszona liczba łączników

## List of Symbols

$t_{...level}$	– time duration of switching signals,
$Q$	– control signals for IGBT transistors,
$S$	– duty cycles of control signals,
$u, i$	– voltage and current,
$\sim Q$	– negation for control signals of IGBT transistors,
$m$	– normalized reference voltage
$t_s$	– sampling time,
$dt$	– dead time,
$D_{\pm,0}$	– duty cycles for negative, positive and zero states,
$G$	– conductance,
$G(s)$	– transfer function in s domain,
$K_p, K_i$	– proportional and resonant gain of resonant controller,
$V_{0..8}$	– vectors for AC-DC converter,
$\Delta$	– difference operator,
$\omega_r$	– rotor angular speed,
$\omega$	– grid voltage frequency pulsation.
$...gridconv$	– signals for DC-AC (grid side) converter,
$...a,b,c$	– voltage/current in a, b, c phases,
$...a',b'$	– voltage/current in a', b' reference frame,
$...1,2,3$	– switches in 1,2 and 3 converter legs,
$...DC$	– dc-bus voltage,
$...ideal$	– voltage/current with ideal converter model,
$...comp$	– voltage/current after compensation,
$...ref$	– reference signals,
$...old$	– values from previous sampling instant,
$... \alpha\beta, dq$	– stationary and rotating coordinates,
$...dtsat$	– value for dead time limit,
$...on,off$	– on and off state values,
$...CEon$	– collector-emitter junction voltage drop in IGBT,
$...FW$	– diode forward voltage,
$... \pm$	– duty cycles for positive and negative output voltage states,
$...0$	– duty cycles for zero output voltage states,
$...pred$	– values obtained by prediction for next sampling instant,
$...cr$	– correction for reference voltages,
$...*$	– complex number denotation,
$...tr$	– symbols regarding transistors,
$...di$	– symbols regarding diodes,
$...C1,C2$	– symbols regarding dc-link capacitors.

## Introduction

Cost optimization of a power converter by reducing the number of power electronic switches was firstly proposed for applications in drive market sector [1], [2], [3]. These attempts were based on the idea of replacing one of the semiconductor branches with a split capacitor bank and connecting a phase wire to its middle, what is shown in Fig. 1 It gives lower number of switching devices comparing to a classical 2-level AC-DC-AC converter which corresponds to reduced number of control channels, IGBT driver circuits etc. (therefore a single standard 6-transistor integrated power module can be used for AC-DC-AC converter). Despite above advantages of converter from Fig. 1 for obtaining sinusoidal current there is a necessity to maintain twice higher DC voltage, what gives higher voltage stress of converter semiconductor devices. This problem can be solved by application of a 3L-NPC introduced in [4]. When this technology was emerging in industry not a single integrated power module product for 3-level devices was available. At the present day manufactures are selling easy to use, integrated half-bridge power modules with clamping diodes. New compact devices make it easier to improve the topology with a split capacitor in DC-link. Thus, the improved topology of an AC-DC-AC converter is shown in Fig. 2.

The 3-level NPC in comparison with a 2-level topology has well known advantages [5]:

- reducing generator torque pulsations,
- reduction of the grid filter size,
- lower overall converter losses.

Moreover, a single phase 3-level NPC inverter with a split capacitor branch was described in Chapter 2.3 of [6] for pho-

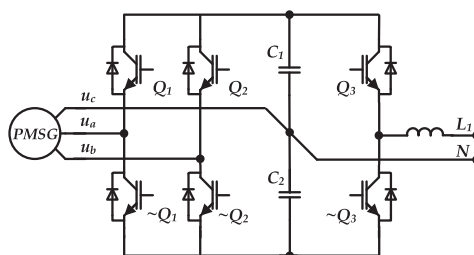


Fig. 1. Two level reduced component converter.

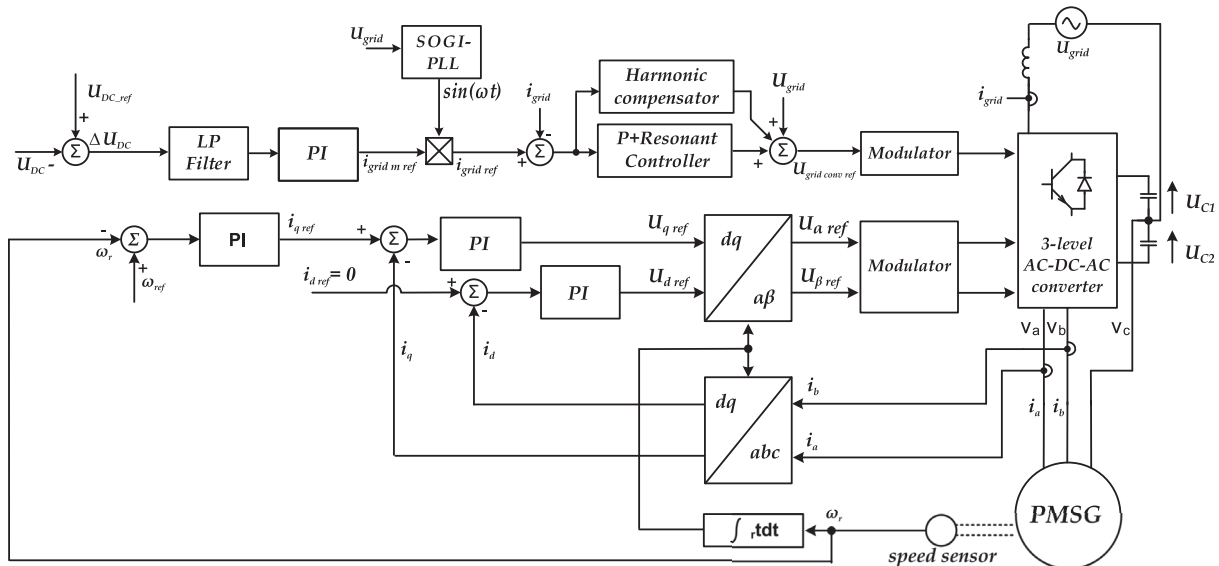


Fig. 3. Control structure - block scheme.

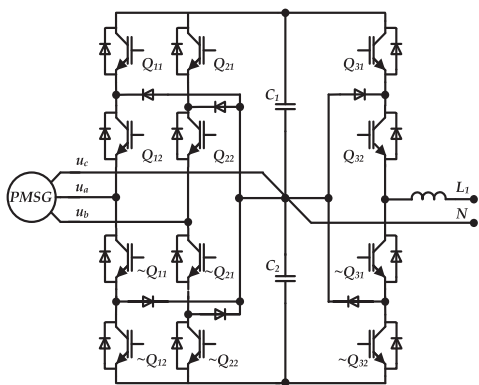


Fig. 2. Simulation results

to voltaic application. It can be concluded that a concept of multilevel converters with reduced switching devices count appears in literature but not as a full AC-DC-AC converter. First section of this article describes the overall control structure, next section and following are describing modulation algorithms for AC-DC and DC-AC parts. The last two sections are reserved for describing solutions for compensation of voltage drop and dead time effects in three phase AC-DC converter.

### Overall control structure

AC-DC converter control scheme is based on FOC method [7]. In this scheme reference speed denoted as  $\omega_{ref}$  is compared with measured angular speed  $r$  (Fig. 3). Obtained error is an input for a PI speed controller that calculates the reference for the current  $i_{q\ ref}$  (responsible for electromagnetic torque). Reference current  $i_{d\ ref}$  is set to be zero. PI current controllers set voltage values of  $U_{d\ ref}$  and  $U_{q\ ref}$  needed for modulation. Control scheme for single-phase DC-AC converter is presented also in Fig. 3, where practical implementation requires operation in convenient abc coordinate system. Because of current being the control variable an AC signal P+Resonant controller firstly proposed in [8] is used. The  $\Delta U_{DC}$  voltage is an error calculated by subtraction of measured sum of voltages on lower and upper capacitors ( $U_{DC}$ ) from given DC voltage  $U_{DC\ ref}$ . Error filtered by a low pass filter with a  $f_{cutoff} = 30\text{Hz}$  is entering a PI controller. Output value is then multiplied by a sine function of the grid voltage angle, which is calculated by

a SOGI-PLL. Resulting outcome becomes reference value for the P+R current controller. Resonant part of mentioned controller is tuned at the grid frequency  $\omega$  for which the highest gain is obtained. Transfer function of a P+R controller is given as:

$$(1) \quad G_{P+R}(s) = K_p + \frac{K_i s^2}{s^2 + \omega^2}$$

Furthermore, it is possible to improve the control structure in order to compensate for higher harmonics in output current when working with a distorted grid voltage. It is done by introducing additional resonant parts to the P+R controller, separately for each individual frequency. Hence, (1) becomes:

$$(2) \quad G_{P+MR}(s) = K_p + \sum_{h=1,3,7,9} \frac{K_i s^2}{s^2 + \omega^2}$$

In this paper, harmonics of the 3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup> and 9<sup>th</sup> order were chosen to be compensated (Fig. 4). Additional resonant harmonic compensation parts are not affecting the fundamental frequency component because every surplus resonant block is damping only at its own frequency. This structure is known as Proportional Multi-Resonant (PMR) controller [6]. One of most relevant problem is modulation algorithm that needs to consider characteristic features of this topology.

### Modulation algorithm for DC-AC converter

From the grid side this converter is nothing more than a simple half bridge NPC converter with three possible to obtain switching combinations (Fig. 5). Proposed modulation method for grid side converter is based on a 1-DM modulation [9].

In this case duty cycle will be determined by (Fig. 6):

- calculation of normalized reference voltage (*I*),
- choice between two nearest states (*II*),
- calculating durations for chosen states (*III*).

### Modulation algorithm for AC-DC converter

Converter from the machine (generator) side has 9 possible switching states (Fig. 7) including one zero vector ( $V_0$ ). An example calculation for sector I is presented in Fig. 8. In order to obtain output voltage at each of eight sectors created by them on  $\alpha\beta$  plane two vectors closest to the reference vector are used and ( $V_0$ ) in the middle of switching period pro-

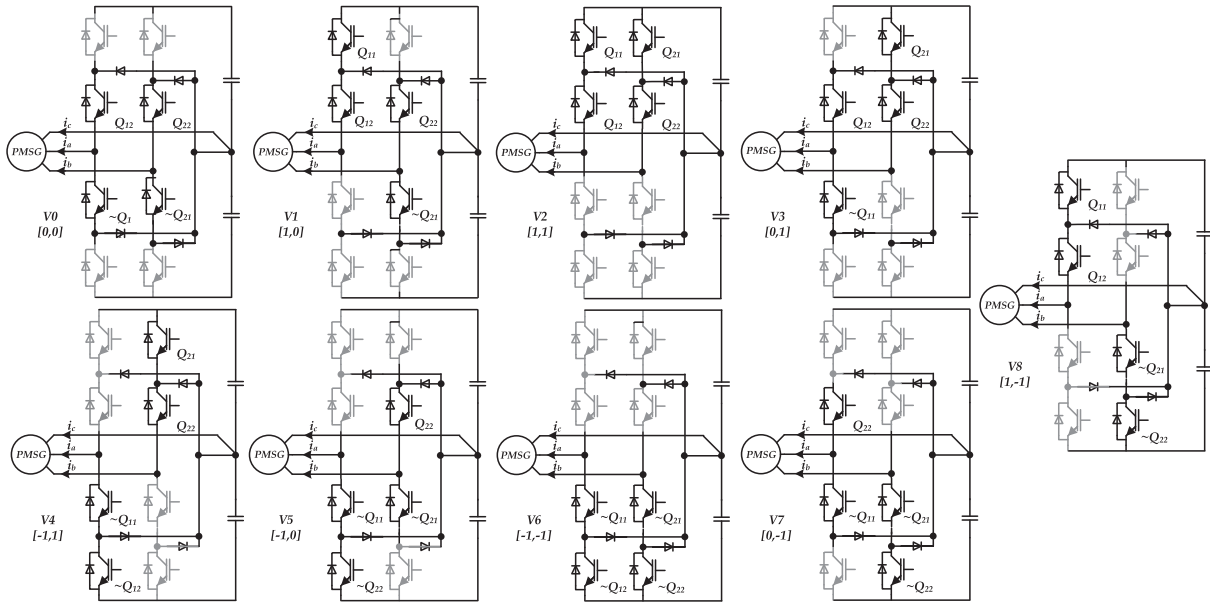


Fig. 7. Switching states of AC/DC generator side converter.

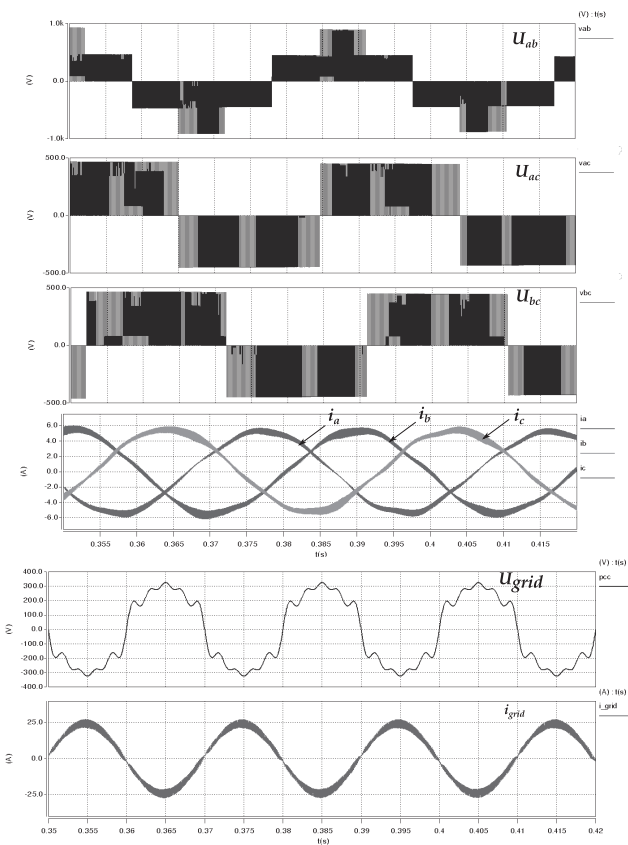


Fig. 4. Currents and voltages for AC-DC-AC converter with ideal semiconductor switches. From top: phase to phase voltages, phase currents, grid voltage, grid current after compensating for distorted grid voltage.

ducing a symmetrical output pulses. This type of modulation method utilizing nine vectors was proposed in [10]. An alternative way for generating switching signals for this type of AC-DC converter was described by Jacobina et. al [2]. In this case modulator requires transforming  $\alpha\beta$  to a stationary coordinate system with two reference voltages  $U'_a$  and  $U'_b$  with  $60^\circ$  angle difference between them (Fig. 9). After this transformation is performed two sinusoidal signals can be used in either carrier based, hysteresis or 1-DM modulation for pulse

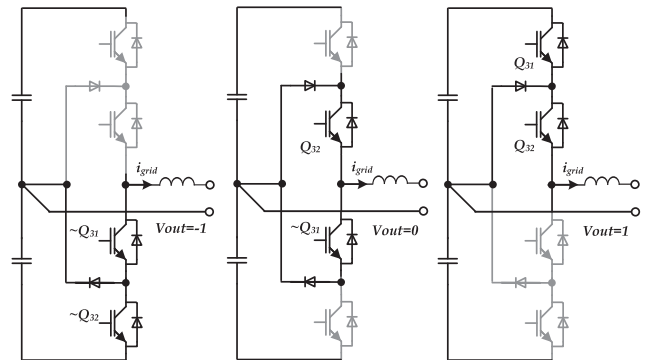


Fig. 5. Combination of switching states for DC-AC grid side converter

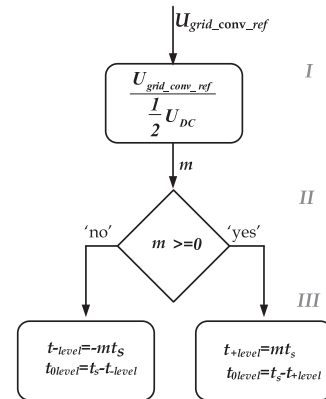


Fig. 6. Calculation based on the 1-DM modulation technique  
width modulation. Problems that should be considered when implementing a modulation algorithm in a converter with such asymmetrical topology with only two active phases:

- voltage drop on semiconductor switches,
- effect introduced by dead time.

Those problems are different than usually proposed for conventional multilevel topologies [11], because distortions caused by these effects are more noticeable for AC-DC part of the converter than it is for DC-AC part connected to grid.

#### Compensation – semiconductor voltage drop effect

Simulation model for this AC-DC-AC converter was build in Saber program using Insulated Gate Bipolar Transistor

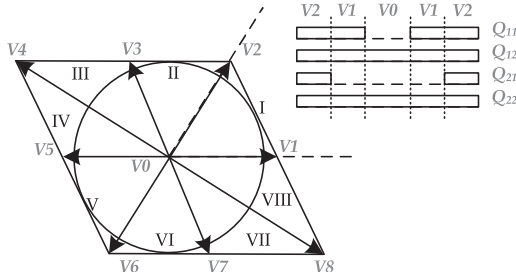


Fig. 8. Vectors obtained from switching states in stationary coordinates and switching periods from sector I

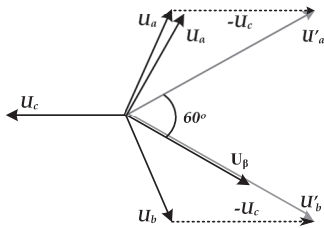


Fig. 9. Phase voltages, voltage reference and output phase voltages.

(IGBT) switch model with presented in Fig. 10. Currents with ideal model of controlled switches and model with voltage drop on semiconductor switches are shown in Fig 11. In

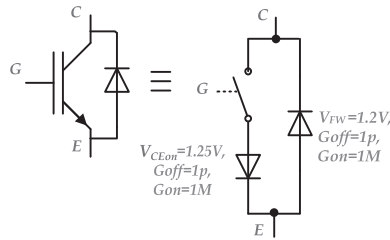


Fig. 10. IGBT model consisting of switch and two diodes: transistor diode ( $T_d$ ) simulating nonlinear transistor voltage drop and freewheeling diode ( $D_{fw}$ ). NPC diodes are also modeled this way with exception of  $V_{FD_{on}} = 0.9V$  (in practice average value for both freewheeling and NPC diodes can be used)

the second case converter currents for are heavily distorted. Effects of voltage drop on semiconductor junctions are compensated by adding a correction to calculated duty cycles. In order to estimate values of voltage drops phase currents should be predicted for next switching instant.

$$(3) \quad i_a^{pred} = i_a \frac{i_a - i_a^{old}}{t_s} \quad i_b^{pred} = i_b \frac{i_b - i_b^{old}}{t_s}$$

Predicted currents are compared with values calculated from transistor and NPC diode data sheets in order to determine state of elements in a and b phases and corresponding voltage drops:

$$(4) \quad \begin{aligned} i_{on}^{tr} &= V_{CEon} G_{off}^{tr}; & i_{on}^{di} &= V_{FW}^{di} G_{off}^{di} \\ i_{on}^{tr} &= V_{CEon} G_{off}^{tr}; & i_{on}^{di} &= V_{FW}^{di} G_{off}^{di} \\ i_{a,b}^{pred} \leq i_{on}^{tr} &\rightarrow v_{a,b}^{tr} = V_{CEon} \\ i_{a,b}^{pred} \leq i_{on}^{di} &\rightarrow v_{a,b}^{di} = V_{FW} \\ i_{a,b}^{pred} > i_{on}^{tr} &\rightarrow v_{a,b}^{tr} = V_{CEon} + \frac{1}{G_{on}^{tr}} i_{a,b}^{pred} \\ i_{a,b}^{pred} > i_{on}^{di} &\rightarrow v_{a,b}^{di} = V_{FW} + \frac{1}{G_{on}^{di}} i_{a,b}^{pred} \end{aligned}$$

Using  $U_{\alpha ref}$  and  $U_{\beta ref}$  transformed to 2-phase coordinate system as in 9 a mean value of voltage drop per sampling period is estimated. Assuming that at zero states voltage error is  $v_{a,b}^{di} + v_{a,b}^{tr}$  (single transistor and a single NPC diode

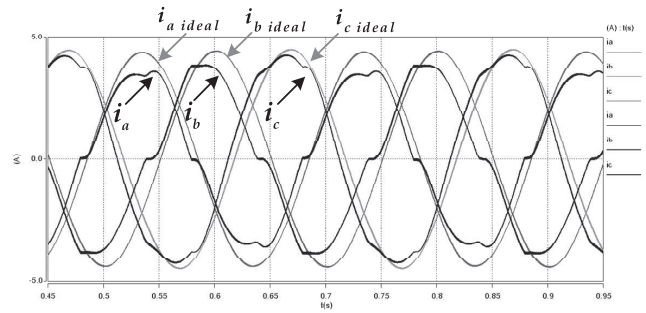


Fig. 11. Phase currents for ideal converter model and converter utilizing switches with voltage drop.

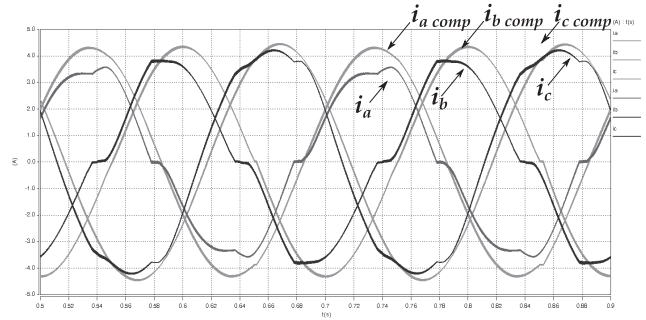


Fig. 12. Phase currents with voltage drop compensation.

in a branch are conducting) and in remaining states  $\pm 2v_{a,b}^{tr}$  we can write:

$$(5) \quad \begin{aligned} D_{a'\pm} &= \frac{|U_{\alpha\beta ref}^*|}{U_{dc}} - \frac{|U_{a' ref}|}{U_{dc}}; & D_{a'0} &= 1 - D_{a'\pm} \\ D_{b'\pm} &= \frac{|U_{\alpha\beta ref}^*|}{U_{dc}} - \frac{|U_{b' ref}|}{U_{dc}}; & D_{b'0} &= 1 - D_{b'\pm} \\ U_{a'}^{cr} &= (D_{a'\pm}(2U_a^{tr}) + D_{a'0}(U_a^{di} + U_a^{tr}))sgn(i_a) \\ U_{b'}^{cr} &= (D_{b'\pm}(2U_b^{tr}) + D_{b'0}(U_b^{di} + U_b^{tr}))sgn(i_b) \end{aligned}$$

Then voltages are transformed to  $\alpha\beta$  coordinate system and added to reference voltages for modulator.

$$(6) \quad U_{\alpha}^{cr} = \frac{\sqrt{3}}{2}(U_{a'}^{cr} - \frac{1}{2}U_{b'}^{cr})U^{\hat{dr}} = \frac{\sqrt{2}}{2}U_{b'}^{cr}$$

Since this converter is using transistors in only two of three phases this effect is clearly visible as asymmetry in phase current amplitudes. Simulation results with applied compensation method are shown in (Fig. 12):

### Compensation - dead time effect

Because of IGBT devices are turning off much more slower than turning on, there is a need for introduction a delay in control signals of gate drivers in order to prevent short-circuiting the dc bus. This delay is only for rising edge of control signals and usually is set to 1-2.5 $\mu$ s. This effect is more visible for low modulation index and low frequency operation [11]. Fig. 13 is a comparison of currents with ideal converter model and a model with dead time set to 1 $\mu$ s, output frequency is 5Hz. Correction for limiting the effect of dead time is calculated based on current sign and saturation level  $i_{dtsat}$  experimentally chosen to take in consideration noise near current zero crossing. Like in Fig. 13 for  $|i| < i_{dtsat}$  correction value is modeled by two linear functions marked as 1 and 2. Break point separating these two is in  $(x_1, y_1)$  coordinates of this point are equal  $x_1 = 0.5i_{dtsat}$

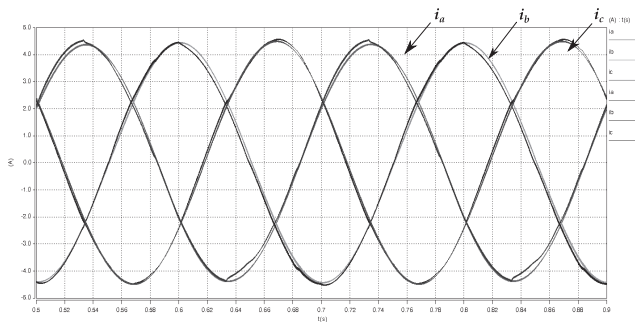


Fig. 13. Currents with dead time effect introduced and with an ideal model of a converter.

and  $y_1 = 0.33i_{dtsat}$  where  $i_{dtsat} = 0.5A$ . These values were chosen experimentally. In case when  $|i_{a,b}| > i_{dtsat}$  correction is equal to  $sgn(i_{a,b})$ . Because this specific con-

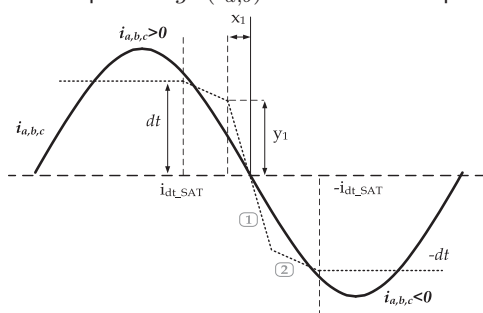


Fig. 14. Phase current and correction function for dead time compensation.

verter type generates voltages that in vector representation are not equal in length (Fig. 8). After obtaining this correction it is necessarily to chose duty cycle of which switching combination should be increased/decreased and in case of a modulator generating vectors non-equal in length introduce a scaling constant. It is easier to implement this compensation in vector modulation when lengths of those vectors are precisely calculated than in 1-DM or carrier based modulation algorithms. Results of compensation for converter with dead time introduced to control signals and without voltage drop on semiconductor switches and with  $f=5Hz$  ( $dt = 1.5\mu s$ ) are shown on Fig. 15. As can be seen shape of phase currents  $i_a$  and  $i_b$  improved mainly near zero crossing.

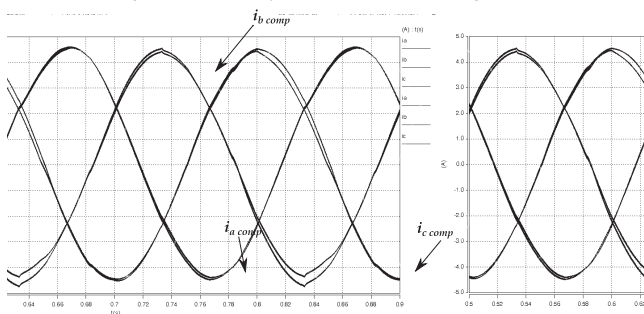


Fig. 15. Currents with dead time effect introduced and with an ideal model of a converter.

## Conclusion

This paper presented an overall control structure and modulation algorithm that included dead time and semiconductor voltage drop compensation for a simplified AC-DC-AC NPC converter. Model utilized non-ideal semiconductor devices and additional dead time introduced in IGBT con-

trol signals. When comparing to a classic three-phase conventional NPC converter effects of dead time is even more visible because only two phases are affected by this phenomenon. Also hence current in the third uncontrolled phase is a sum of two active ones voltage drop on devices leads to higher current flowing through winding of third phase. Results of simulation study shown that applying compensation techniques for voltage drop on semiconductor devices and distortion introduced by dead time leads to better waveforms of output currents.

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## REFERENCES

- [1] Van Der Broeck, H. W.; Van Wyk, J. D.: A Comparative Investigation of a Three-Phase Induction Machine Drive with a Component Minimized Voltage-Fed Inverter under Different Control Options, Industry Applications, IEEE Transactions on, 20, pp. 309-320, 1984.
- [2] Jacobina, C.B. and da Silva, E.R.C. and Lima, A.M.N. and Ribeiro, R.L.A.: Vector and scalar control of a four switch three phase inverter, Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE, 1995.
- [3] Blaabjerg, F.; Neacsu, D. and Pedersen, J.: Adaptive SVM to compensate DC-link voltage ripple for four-switch three-phase voltage-source inverters, Power Electronics, IEEE Transactions on, 14, pp. 743-752, 1999.
- [4] Mlodzikowski, P.; Kot, R.; Stynski, S.; Malinowski, M.: Simulation Study of a Simplified Multilevel AC/DC/AC Converter for a Small Wind Turbine, PEIA (I Power Electronics for Industrial Applications and Renewable Energy Conversion), 1, pp. 203-208, 2011.
- [5] Teichmann, R.; Malinowski, M.; Bernet, S.: Evaluation of three-level rectifiers for low-voltage utility applications, Industrial Electronics, IEEE Transactions on, 52, pp. 471-481, 2005.
- [6] Teodorescu, R.; Liserre, M.; Rodríguez, P.: Grid Converters for Photovoltaic and Wind Power Systems, Wiley-IEEE Press, 2011.
- [7] Zaragoza, J.; Staines, C.; Arias, A.; Pou, J.; Robles, E.; Ceballos, S.: Comparison of speed control strategies for maximum power tracking in a wind energy conversion system, MELECON 2010 - 2010 15th IEEE Mediterranean Electrotechnical Conference, 1, pp. 961-966, 2010.
- [8] Sato, Y.; Ishizuka, T.; Nezu, K.; Kataoka, T.: A new control strategy for voltage-type PWM rectifiers to realize zero steady-state control error in input current, Industry Applications, IEEE Transactions on, 34, pp. 480-486, 1998.
- [9] Leon, J.I. and Portillo, R. and Vazquez, S. and Padilla, J.J. and Franquelo, L.G. and Carrasco, J.M.: Simple Unified Approach to Develop a Time-Domain Modulation Strategy for Single-Phase Multilevel Converters, Industrial Electronics, IEEE Transactions on, 55, pp. 3239-3248, 2008.
- [10] Bor-Ren Lin and Ta-Chang Wei: Space vector modulation strategy for an eight-switch three-phase NPC converter, Aerospace and Electronic Systems, IEEE Transactions on, 40, pp. 553-566, 2004.
- [11] Minshull, S.R. and Bingham, C.M. and Stone, D.A. and Foster, M.P.: Compensation of Nonlinearities in Diode-Clamped Multilevel Converters, Industrial Electronics, IEEE Transactions on, 57, pp. 2651-2658, 2010

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