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Design and Analysis of the Droop-Controlled Parallel Four-leg Inverters to Share Unbalanced and Nonlinear Loads

Abstract: *In this paper, the performance of wireless operation of four-leg parallel inverters, at the presence of unbalanced nonlinear loads, is investigated. In order to control the parallel inverters, an inner current and external voltage control loops should be designed. In this paper, a proportional controller for the current internal loop as well as a proportional-resonant one for the voltage external loop are investigated and designed to ensure the proper performance of the system at the presence of unbalanced and nonlinear loads. In this paper, droop control and virtual output impedance loops have formed the power sharing control system for the parallel inverters. The proposed system is able to feed balanced, unbalanced, and nonlinear loads and provides an appropriate sinusoidal voltage waveform for loads by accurately sharing power between the parallel inverters. Simulation results verify the accurate and proper performance of the proposed system.*

Streszczenie. *Zaprezentowano właściwości bezprzewodowej pracy przekształtnika w obecności niezrównoważonego, nieliniowego obciążenia. Sterowaniu podlegają wewnętrzna pętla prądowa jak i zewnętrzna pętla napięciowa. System sterowania kontroluje spadki napięcia oraz zewnętrzną impedancję.* ***Projekt i analiza poczwórnego przekształtnika ze sterowanymi spadkami stosowanego do pracy w warunkach niezrównoważonych i nieliniowych obciążeń.***

Keywords*:* four-leg inverter, parallel inverters operation, Droop method, Virtual output resistive impedance
Słowa kluczowe: poczwórny przekształtnik, kontrola spadku, niezrównoważone obciążenie.

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Introduction

According to rapid increase of electronic-based devices applications, the unbalanced and nonlinear loads form the main part of the uninterrupted power sources loads. These nonlinear and unbalanced loads, lead to voltage disturbance directly affecting the proper performance of loads and inverters. Four-leg inverters, possessing an additional leg compared to the conventional three-leg ones, are able to pass the zero-sequence current of unbalanced and nonlinear loads [1]. The advantage of four-wire inverters over three-wire ones falls in its current zero sequence provision feature. Three-phase unbalanced loads and the single-phase ones are the origins of zero sequence current, where the zero sequence current flows towards the Δ side is prevented if a Y-Δ transformer is utilized in the output side of the three-phase three-wire inverter. Comparing a three-phase inverter possessing Y-Δ transformer to a three-phase four-wire inverter depicts that the four-wire inverter has distinctive advantages over the three-phase inverter with transformer, from size, weight, moving ability, initial manufacturing costs, compatibility, and system total efficiency viewpoints. However, there exist some disadvantages such as input/output complexity, fault management, and the number of elements in the system compared to the three-phase inverter with transformer [2].

There are two general topologies for four-leg inverters: three-leg inverters with split dc-link capacitors, and four-leg inverters in which the neutral point of load is connected to the mid-point of the fourth leg. The split-link topology is simpler and uses fewer semiconductors (six compared with eight) but introduces the problem of ensuring close voltage sharing between the split capacitors and the need to attenuate voltage ripple off them. A large neutral current (produced by either unbalanced or nonlinear loads) causes a large perturbation to the split voltages. Such a perturbation needs to be compensated for in the phase-voltage control scheme and risks malfunction of the inverter. Voltage balancing controllers, such as dynamic hysteresis current control, have been proposed to overcome the problem, but the zero-sequence current can still cause large dc voltage imbalance. The voltage deviation can be attenuated by using larger dc-link capacitors but with an obvious penalty in cost and size. The split-link topology requires that the phase voltage peak is less than or equal to the split dc-link voltage (normally half the total dc-link voltage), whereas the four-leg inverter can allow a line-voltage peak equal to half the total dc-link voltage. This gives an approximately 15% advantage in dc voltage utilization in favor of the four-leg inverter [3]. However, there are some parasitic capacitances between the dc busbars, packages, heat sinks, and ground, which may yield to some common-mode current flows through long paths involving ground. These are known to be a source of electromagnetic compatibility (EMC) problems. This issue can be reduced using a large enough choke coil in the neutral conductor [4]. Comparing these two topologies indicates that the four-leg inverters show better performance in low voltage utilizations especially if the neutral current is significant. However, the three-leg inverters with split dc-link capacitors perform better in high voltage utilizations, particularly under multilevel application circumstances [2]

In power systems design, the parallel connection of voltage source inverters has been remarkably considered. Reliability improvement, increase in accessibility, power ratings and fault endurance rate, and simpler maintenance are some advantages of the parallel operation of inverters. The issues to be considered in parallel inverters operation include equal current sharing between inverters (if the inverters ratings are equal) and flexibility in the number of parallel units. Several control techniques have been proposed to achieve the mentioned targets, classified into two general types. The first control type is based on the droop method, which is a kind of wireless interconnection. Since this method requires just the local measurement information, it has higher reliability and flexibility, compared to the second type. The second control type consists of techniques based on the instantaneous load sharing, which can be classified into four general types: central control, master-slave control, circular chain control, and average current sharing [5].

In parallel operation of three-phase inverters, different methods are proposed up to now to compensate the resultant unbalancing and nonlinear current, majority of which utilize three-phase three-wires, while three-phase four-wire inverters with split dc-link capacitors is applied only in one case. Applying synchronous reference frame (SRF) theory and PI controller on positive sequence of inverter voltage is proposed in [6]. In [7], a method based on the aggregation of PI controllers and SRF on positive and negative sequences of inverter output voltage is suggested. Negative sequence compensation through shunt converter [8-9] and through series converter [10] is also investigated.

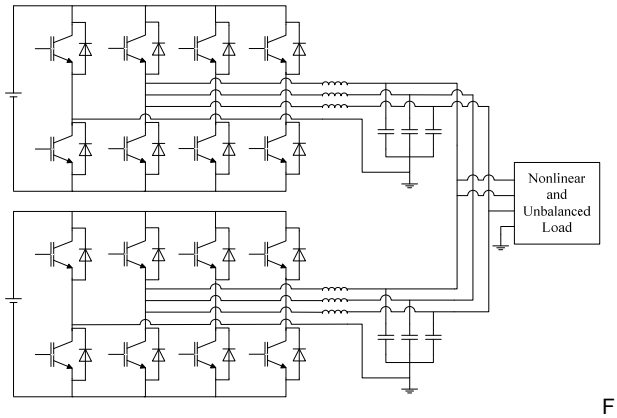
In [11], a common three-phase frequency droop technique versus active power (P-f) and voltage droop versus reactive power (Q-V) is presented where the share of each inverter in providing total harmonic V-A of local electric power network is specified using a droop curve of the harmonic V-A versus harmonic conduction (Q-H), in addition to controlling the share of each inverter in active and reactive powers main sequence. In [12], a droop method is proposed based on reactive power versus current negative sequence and voltage positive sequence, which is able to be aggregated by the conventional active power droop in terms of frequency, and by reactive power droop in terms of voltage methods. Parallel operation of two three-phase UPSs connected to Y-Δ transformer through master-slave control technique is investigated in [13]. In [14], a droop method for paralleling three-phase four-wire inverters with split dc-link capacitor at the presence of nonlinear and unbalanced loads is presented.

In researches conducted on three-phase parallel inverters operation field, as reviewed above, the parallel operation of three-phase four-leg inverters has not been accomplished yet and the present research aims to investigate parallel operation of three-phase four-leg inverters at the presence of nonlinear and unbalanced loads.

Considering the aforementioned methods about parallel inverters operation and investigating the advantages and disadvantages of each one, in this paper a long distance between inverters is assumed, and thus, the droop control method has been selected to control the parallel operation of four-leg inverters. Also, the proportional and the proportional-resonant controllers are proposed and designed for the current internal and voltage external loops, respectively, to assure proper parallel performance of the three-phase four-leg inverters.

System Configuration

Fig. 1 shows the configuration of the proposed system. Two three-phase four-wire inverters are under consideration for parallel operation. The parallel inverters are connected to the nonlinear and unbalanced loads through a tie wire. In this system, it is aimed to provide the proper voltage on loads and to equally share the unbalanced and harmonic current of loads between inverters. Each four-leg inverter's switching is accomplished through the carrier-based modulation technique for more simplicity in control and implementation.



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iFig.1. Two parallel four-leg inverters

Four-Leg Inverter Control Strategy

Initially, the performance of a four-leg inverter, as well as the issues to be considered in control and design of its parameters, is investigated to achieve appropriate performance and operation of the parallel four-leg inverters.

A. General Structure

Fig. 2 shows the single voltage loop control structure. This control scheme eliminates the need of current sensors but fails to achieve high steady-state and transient responses with adequate stability margin. All three control objectives can be ensured with multiloop control (shown in Fig. 3). Only a proportional controller is enough for inner current loop though it produces a significant phase shift at operating frequency. A large gain associated with outer voltage controller is essential in order to compensate the phase shift and to ensure negligible steady-state error.

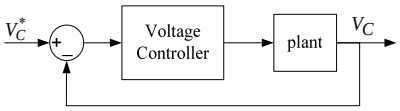

Fig.2. Single voltage loop

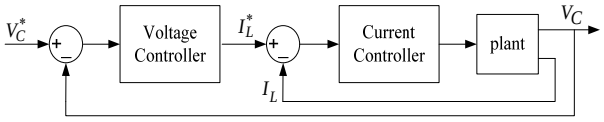

Fig. 3. Multiloop with inner current loop

In present case, a large steady-state gain is achieved by classical proportional-resonant controller in stationary reference frame [15]. Again, in multiloop or cascaded loop controller, the bandwidth of the voltage controller cannot be increased beyond certain value. Hence, inner current loop plays a significant role on damping of resonance oscillation due to output *LC* filter.

B. Inner Current Loop and Damping of Resonance Oscillation

First, let us consider the configuration of inner current loop. The inner loop variable used here is inductor current for better resonance damping and power circuit protection. Fig. 4 shows the configuration of the current loop with a proportional controller. V_i is the inverter output voltage and I_L (s)/V_i(*s*) is the plants transfer function when the disturbance input *Io* is ignored. The plant transfer function is given by

$$\frac{I_L(s)}{V_i(s)} = \frac{sC}{1+s^2LC} \tag{1}$$

It is marginally stable and susceptible to resonance oscillation. From (1), the closed-loop transfer function can be derived as

$$\frac{I_L(s)}{I_L^*(s)} = \frac{sK_cGC}{1+sK_cGC+s^2LC} \tag{2}$$

Equation (2) clearly indicates that if current controller gain (K_c) is increased, better damping of resonance oscillation can be achieved. Fig. 5 shows the corresponding root locus for various values of K_c. For $K_c \geq 0.104$, the oscillatory behavior of the system is completely eliminated. The closed-loop transfer function in (2) is approximated as

$$\frac{I_L(s)}{I_L^*(s)} \approx \frac{sC}{1+sK_cGC} \tag{3}$$

for design verifications of outer loop. This assumption is valid because there is considerable amount of steady-state phase and magnitude error in current loop. This is clear from the Bode plot of the closed-loop transfer function for inner current loop (shown in Fig. 6).

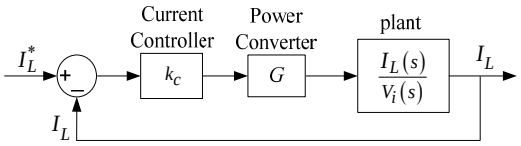

Fig. 4. Inner current loop and plant.

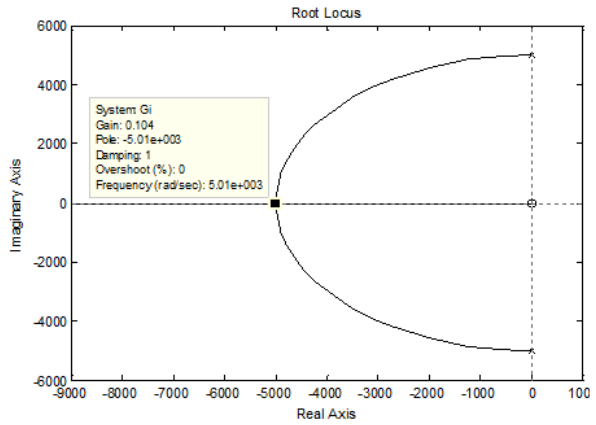

Fig. 5. Root locus plot of current loop.

C. *Outer Voltage Loop and Stability Analysis*

From the inner current loop gain function (see Fig. 6), it may appear that a simple proportional–integral (PI) controller with high bandwidth may be used to achieve voltage control. In such a case, the dc gain of the loop will be infinity. It is found that such a controller gives rise to starting problems since this high dc gain sometimes leads the control to get into overmodulation. Therefore, the strategy to obtain stable operating point as well as good steady-state performance requires unconventional compensator design.

The structure of the outer voltage loop with proportional-resonant controller is shown in Fig. 7. Because of limitations in practical implementations true resonant controller cannot be used. Fig. 7 shows the approximate resonant controller with cutoff frequency ω_{cut} . Output of voltage controller is the reference input for inner current controller (inductor current reference I_L^*). Fig. 7 also shows the approximate current loop transfer function [as given in (3)] and load current I_o as disturbance input. Ignoring the disturbance input, the characteristics equation of outer voltage loop is given in (4), as shown at the top of next page. The stability criteria can be checked from Routh array given by (5). As for all possible values of K_p > 0 and K_i > 0 the first row of Routh array has no sign change, the system stability is ensured for all values of K_p and K_i . Hence, it is possible to achieve a fast steady-state response for fundamental frequency ω_o.

$$s^3 K_c GC + s^2\left\{1 + K_p + 2\omega_{cut} K_c GC\right\} + s\left\{\left(2 + 2K_c + K_i\right)\omega_{cut} + \omega_0^2 K_c GC\right\} + \omega_0^2\left(1 + K_p\right) = 0 \quad (4)$$

The controller structure shown in Fig. 7 is a single-phase equivalent of three-phase controller. This control structure is sufficient to handle both balanced and unbalanced loading conditions.

D. *Inverter* Control in Nonlinear and Unbalanced Loads

The output voltage of a power supply connected to nonlinear or unbalanced loads includes prominently third, fifth and seventh-harmonics other than fundamental. The control structure is indicated in figure 7 is not suitable to compensate disturbing effect of load current on the output voltage. As shown in figure 8, three separate resonant controllers for third, fifth and seventh harmonic components are considered in outer voltage loop as (6). The magnitudes of K_{i3} , K_{i5} and K_{i7} specify the steady-state error for third, fifth and seventh-harmonic components respectively. The stability analysis using Routh array criteria for this controller

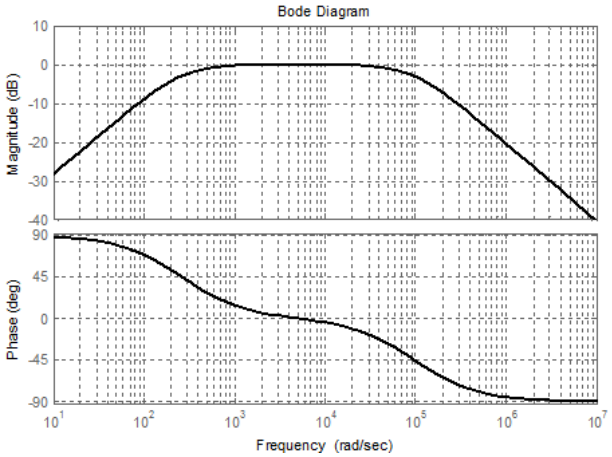

Fig. 6. Bode plot of $\frac{I_L(s)}{I_L^*(s)}$

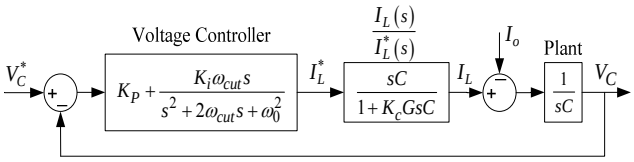

Fig. 7. Proportional-resonant controller for fundamental component.

structure implicates very complicated mathematical calculations. In order to simplify calculations, controller parameters are determined using Bode plots. When K_{i3} , K_{i5} and K_{i7} are set to zero then controller structure is appropriate only for linear loads. By increasing these values (for example, 0, 2, 4 Ω^{-1}, etc., in figure 9), the steady-state error for third, fifth and seventh-harmonic components reduces; however, the phase margin gradually falls. Finally, for K_{i3} = K_{i5} = K_{i7} = 6 Ω^{-1} (commensurate with magnitude > 40 dB at third, fifth and seventh harmonic frequencies) the steady-state error will be less than 1% for these three harmonic components. Therefore, from this design criterion, K_{i3} , K_{i5} and K_{i7} are chosen. However, these values can be further increased to obtain better performance. However, for K_{i3} = K_{i5} = K_{i7} = 4 Ω^{-1} , the bode plot indicates that the phase margin is obviously low and this matter causes undesirable oscillation in output voltage waveform. For K_{i3} = K_{i5} = K_{i7} = 6 Ω−1 (commensurate with suitable steady-state error for harmonic components) the system is not stable (phase margin = −1°). In order to eliminate such problem and to decrease the steady-state error for harmonics below desired limit, a lead-lag compensator [15] is used and applied in the bode plot of figure 9.

The dynamic response of the system can be improved further by adding a inductor current loop (optional). The current controllers are proportional type and its proportional gain is calculated as equation (7).

(5)
$$\begin{array}{lll} s^3 & : & K_c GC & \left(2+2K_c+K_i\right)\omega_{cut}+K_c GC\omega_0^2 \\ s^2 & : & 1+K_p+2\omega_{cut}K_c GC & \omega_0^2\left(1+K_p\right) \\ s^1 & : & \left(2+2K_c+K_i\right)\omega_{cut}+\dfrac{2\omega_{cut}\left(K_c GC\omega_0\right)^2}{1+K_p+2\omega_{cut}K_c GC} & 0 \\ s^0 & : & \omega_0^2\left(1+K_p\right) & 0 \end{array}$$

(6)
$$G_v(s)=K_p+\frac{K_i\omega_{cut}s}{s^2+2\omega_{cut}s+(\omega_0)^2}+\frac{K_{i3}\omega_{cut3}s}{s^2+2\omega_{cut3}s+(\omega_0)^2}+\frac{K_{i5}\omega_{cut5}s}{s^2+2\omega_{cut5}s+(\omega_0)^2}+\frac{K_{i7}\omega_{cut7}s}{s^2+2\omega_{cut7}s+(\omega_0)^2}$$

(7)
$$k_c=\frac{L}{G\Delta T}$$

where L is the output inductor of the inverter, G is the gain of the converter, and ΔT is the sampling time.

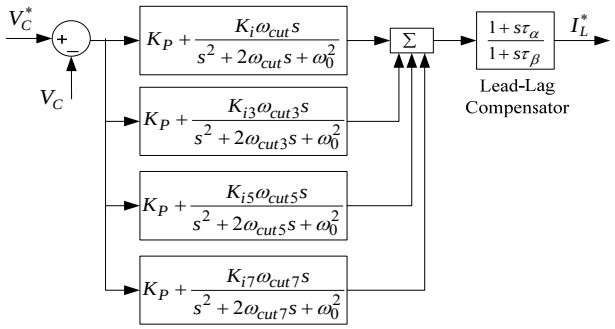

Fig. 8. Proportional-multiresonant controller for fundamental and harmonic (third, fifth and seventh) components

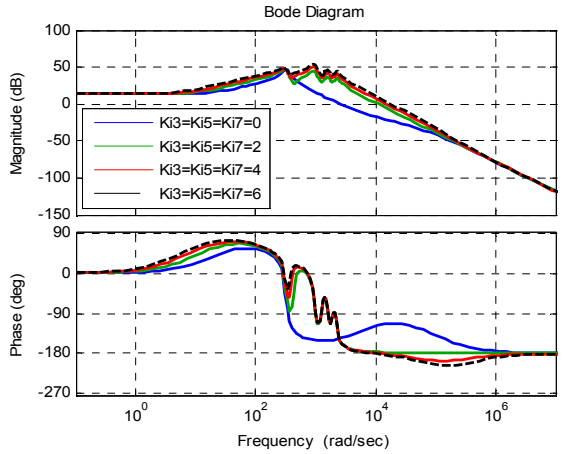

Fig. 9. Bode plot of voltage loop for different values of K_{i3} , K_{i5} and K_{i7} (in Ohm inverse).

The current controller outputs are added with the feedfarward output capacitor voltages to relieve the burden on the current controllers. Next, three inverter reference voltages are given to the power circuit through the modulator and driver.

Concentrating on the controller part, (equation (8) can be written from (6) the following:

(8)
$$V_i=\left[\left(V_c^*-V_c\right)G_v(s)LL(s)-I_L\right]k_cG$$

where $LL(s)$ is the transfer function of the lead-lag compensator and kc is the proportional gain of the current controller. By combining (7) and (8) and putting $I_L = I_o + sCV_c$, (9) can be written as:

(9)
$$V_c=G(s)V_c^*-Z_o(s)I_o$$

where $G(s)$ and $Z_o(s)$ are the control transfer function and the output-impedance transfer function, respectively, and are given as follows:

(10)
$$G(s)=\frac{G_v(s)LL(s)k_cG}{1+\left(r_L+k_cG\right)Cs+LCs^2+G_v(s)LL(s)k_cG}$$

(11)
$$Z_o(s)=\frac{r_L+k_cG+sL}{1+\left(r_L+k_cG\right)Cs+LCs^2+G_v(s)LL(s)k_cG}$$

In (10), $G(s)$ is the closed-loop transfer function of the voltage loop. The open-loop transfer function of the voltage loop is given by

(12)
$$G_{op}(s)=\frac{G_v(s)LL(s)k_cG}{1+\left(r_L+k_cG\right)Cs+LCs^2}$$

The overall block diagram of voltage control loop based on the proportional-resonant control is shown in Fig. 10.

Parallel Operation of Four-Leg Inverters

In this paper, the control aim is to uniformly share the currents of output unbalanced and nonlinear loads of inverters such that an appropriate voltage is applied across the output loads. In this next section, to illustrate the operation and performance of parallel four-leg inverters, at first, the active and reactive powers of each phase are calculated, and then, the droop characteristic of three-phase active and reactive powers is studied; the voltage reference generation using virtual resistive output impedance is investigated.

A. Each Phase Active and Reactive Power Calculation

The active and reactive power shared by the converter are evaluated from the measured signals. The output capacitor voltage V_c and the output current shared by the converter I_o are used to determine the instantaneous active and reactive power as follows:

(13)
$$\begin{aligned} P_i &= V_c I_o \\ Q_i &= -V_c I_o\left(-90^\circ\right) \end{aligned}$$

where P_i and Q_i are the instantaneous active and reactive powers, respectively. The -90° phase shift in I_o is required to calculate the reactive power. Then, P_i and Q_i are processed by low-pass filters (LPFs) in order to eliminate the oscillatory component. The cutoff frequencies of the LPFs are selected as one decade below the line frequency.

B. Droop Characteristics of Three-phase Active and Reactive Powers

Total three-phase active and reactive power can be obtained by simply adding per phase P and Q values.

These three-phase active powers (P_{3ph} and Q_{3ph}) due to low-pass filtering do not contain any oscillatory component and thus, can be treated as positive sequence active and reactive powers. The frequency and magnitude of the voltage references of each phase are determined by P_{3ph} and Q_{3ph} as follows (14).

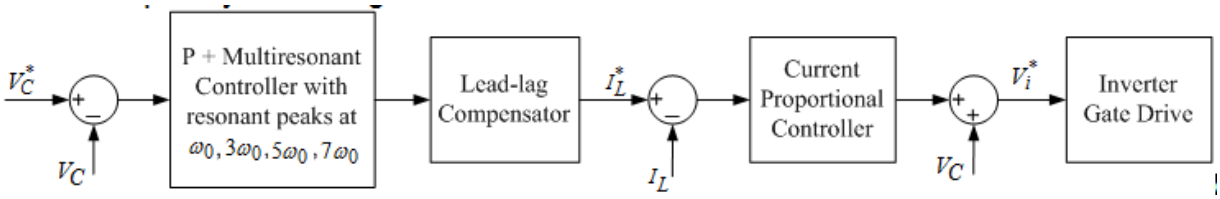

Fig. 10. Block diagram of the voltage control loop based on the proportional-resonant control.

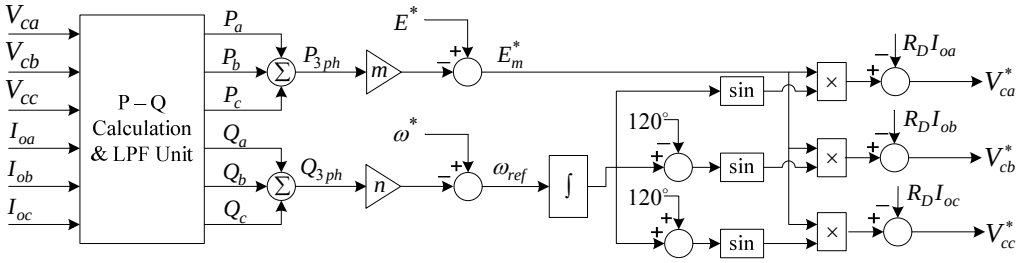

Fig. 11. Block diagram of the voltage control loop based on the proportional-resonant control

$$E_m^* = E^* - nP_{3ph} = E^* - n\left(P_a + P_b + P_c\right)$$
$$\omega_{ref} = \omega^* + mQ_{3ph} = \omega^* + m\left(Q_a + Q_b + Q_c\right) \quad (14)$$

The droop characteristics guarantee to bring the phase angles and voltage magnitudes of the units to a equilibrium point and thus eliminate circulating current completely at steady state [14].

C. Voltage Reference Generation With Virtual Resistive Output-Impedance Loop

With the help of the generated amplitudes (E_m^*) and frequency (ω_{ref}), the voltage references can be obtained as

$$\begin{bmatrix} V_{ca}^* \\ V_{cb}^* \\ V_{cc}^* \end{bmatrix} = \begin{bmatrix} E_m^* \sin\left(\omega_{ref} t\right) - R_D I_{oa} \\ E_m^* \sin\left(\omega_{ref} t - 120^\circ\right) - R_D I_{ob} \\ E_m^* \sin\left(\omega_{ref} t + 120^\circ\right) - R_D I_{oc} \end{bmatrix} \quad (15)$$

In (15), R_D represents the virtual resistive output impedance.

The Block diagram of the voltage control loop based on proportional-resonant control is shown in Fig. 10. Fig 11 illustrates the block diagram of parallel four-leg inverters control system based on droop and virtual resistive output impedance loops, used to generate the reference voltage.

Simulation Results

The structures of two parallel four-leg inverters in presence of nonlinear and harmonic loads are simulated to investigate the accuracy of the performance and operation of the proposed system. The power system parameters and the inverter control parameters are listed in Table I.

In order to evaluate the dynamic performance of the proposed system, a nonlinear load is connected to the inverters in the [0 0.1Sec] time interval and an unbalanced load is then added to the previous load in t = 0.1Sec.

Fig. 12 shows the three-phase voltage generated by the parallel inverters. As it can be observed, the generated voltage has a three-phase sinusoidal form, despite the existence of nonlinear and unbalanced loads.

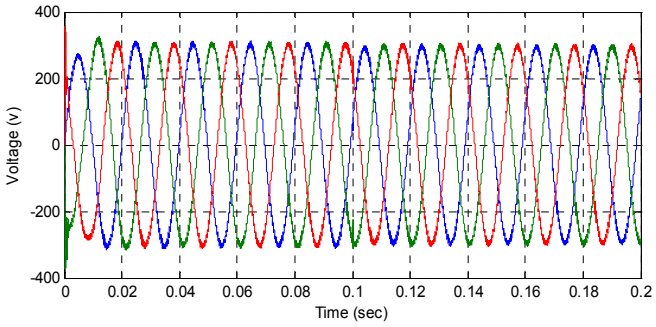

Fig. 12. The output voltage of parallel four-leg inverters.

Table 1. Power circuit and control parameters values

Parameters	Values
V_c	380 v
f_s	5kHz
L	3 mH
R	0.1 Ω
C	10 μF
k_c	1.28 Ω
k_p	0.0125 Ω^{-1}
k_i	1.8 Ω^{-1}
k_{i3}	6 Ω^{-1}
k_{i5}	6 Ω^{-1}
k_{i7}	6 Ω^{-1}
ω_{cut1}	31.41 rad / sec
ω_{cut3}	92.23 rad / sec
ω_{cut5}	157.08 rad / sec
ω_{cut7}	219.9 rad / sec
τ_α	108 μsec
τ_β	15 μsec

n	1.8×10^{-3} rad/sec/VAR
m	1.8×10^{-3} V/W
R_D	$0.5\,\Omega$

The current drawn by the loads is shown in Fig. 13. It can be seen that an unbalanced load is added to the nonlinear one in t=0.1 sec. This figure well depicts the appropriate dynamic performance of the system, as well as proper operation in load sharing.

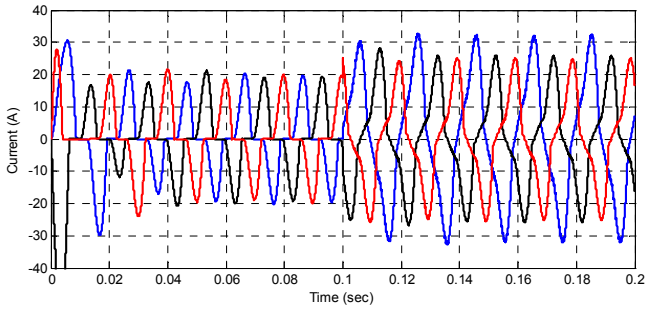

Fig. 13. The three-phase current of nonlinear and unbalanced loads at the output of parallel four-leg inverters.

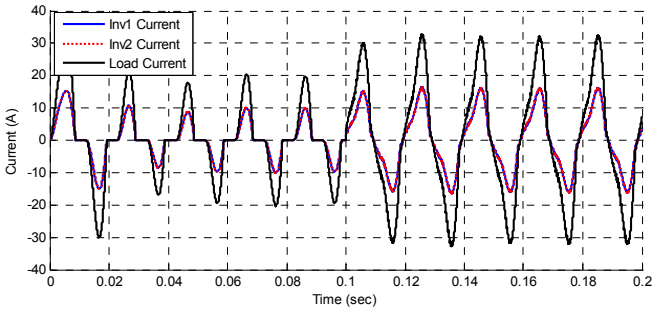

Fig. 14. One phase current waveform of each inverter with equal ratings and total drawn phase current.

To illustrate the equality of both inverters current, the current of both inverters and total current drawn in one phase are shown in Fig. 14. This figure shows the correct operation of control system and there is no circular current between the inverters.

Conclusion

In this paper, design of parallel four-leg three-phase inverter controllers at the presence of unbalanced and nonlinear loads is proposed. In order to achieve the proper performance of the proposed system at the presence of unbalanced and nonlinear loads, the proportional controller for current internal loop and proportional-resonant controller for voltage external loop are proposed. The controllers' parameters are designed systematically. The long distance between inverters is assumed and thus, the virtual resistive output impedance based droop control method is used to parallel the four-leg inverters. The proposed system is able to share balanced, unbalanced, and nonlinear loads and provides proper sinusoidal voltage waveform for loads as well as accurate current sharing between parallel inverters proportional to their ratings. The simulation results show the appropriate performance and operation of the proposed system.

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