

Analysis and Design of Hybrid Learning Control scheme for High Performance UPS Inverters

Abstract. This paper presents a high performance control scheme for a single phase uninterruptible power supply (UPS) inverter. In the proposed structure, a learning-type controller eliminates periodic disturbances and therefore guaranties high steady-state performance while an instantaneous feedback controller ensures fast dynamic response of the system. Analysis and design of each controller are presented and a brief stability analysis of the complete system is given. Finally to validate the proposed control scheme, simulation results of the system are presented.

Streszczenie. W artykule opisano metodę sterowania jednofazowym przekształtnikiem stosowanym w systemie UPS. Zastosowano układ uczący się co gwarantowało płynną pracę systemu. Bazujący na chwilowych wartościach sterownik w sprzężeniu zwrotnym zapewniał dobrą dynamikę. **Analiza i projekt hybrydowego uczącego się sterownika w zastosowaniu do systemu UPS**

Keywords: Uninterruptible Power Supply (UPS), Repetitive Controller, Deadbeat Controller, Total Harmonic Distortion (THD).

Słowa kluczowe: system UPS, przekształtnik, sterownik.

doi:10.12915/pe.2014.04.09

Introduction

Uninterruptible power supply (UPS) systems are used to provide reliable and well-regulated AC voltages for critical and sensitive loads. The performance of UPS inverter is measured both in terms of steady-state performance, such as voltage regulation and Total Harmonic Distortion (THD), and transient performance, such as response to a sudden change in linear and non-linear load.

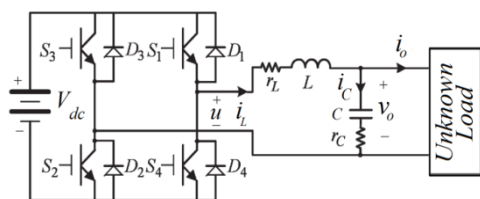


Fig.1. Single-phase full-bridge inverter

Fig. 1 shows a UPS inverter configuration that is commonly used in single-phase UPSs. Instantaneous feedback methods such as multi-loop [1], sliding-mode[2] and Deadbeat control (DBC)[3, 4] demonstrated High quality output voltage and fast dynamic responses. However, these methods alone cannot eliminate the periodic distortion caused by nonlinear loads and parameter uncertainties. As a result, the steady-state performance is low, especially in the case of nonlinear loads. On the other hand, the learning-type controllers such as repetitive controller (RC)[5, 6] and Iterative learning controller [7], basically aim at canceling periodic disturbances. Actually they utilize the repetitive nature of the disturbances while other methods do not. In this method, the output voltage is the only variable needs to be sensed, and the control action needs not to be very fast to achieve high quality output voltage, but sub-cycle response is impossible. So fast dynamic response is not achievable [6].

In this paper, we propose a new hybrid learning controller consisting of a deadbeat controller and a repetitive controller linked in cascade configuration (Fig. 2). The deadbeat controller improves the transient response, while the repetitive controller serves to eliminate the

periodic errors resulting from periodic disturbances. The design procedure is presented in detail and the stability of overall system is discussed. Finally, computer simulation results are presented to validate the proposed method.

Dynamic model of the Single-Phase Inverter

Under the assumption that the switching frequency is high enough, the PWM inverter is considered as a voltage source and the dynamic response of a UPS inverter is mainly determined by the LC filter. According to Fig.1 transfer function model can be written as follows [7]:

$$(1) \quad V_o(s) = G_P(s)U(s) - G_o(s)I_o(s)$$

where:

$$(2) \quad G_P(s) = \frac{r_c CS + 1}{LCS^2 + C(r_L + r_c)S + 1}$$

$$(3) \quad G_o(s) = \frac{r_c CLS^2 + (L + r_c r_L C)S + r_L}{LCS^2 + C(r_L + r_c)S + 1}$$

In steady state, the second term of (1) is repetitive since the load current is repetitive. By considering the effect of load current $Q(s)I_o(s)$ as external disturbance $D(s)$, the model of UPS inverters is :

$$(4) \quad V_o(s) = G_P(s)U(s) + D(s)$$

Proposed Controller

Fig. 2 shows the proposed hybrid learning controller for single-phase UPS inverter. In this figure, $Y(z)$ is the system output, $R(z)$ is the sine reference, $E(z)$ is error, $U_{RC}(z)$ is the RC output and $U(z)$ is the reference of DB controller. All repetitive disturbances that cause deviation in the output voltage, such as load current and dead-time effect in the inverter switches, are summarized as $D(z)$. As shown in Fig.2, RC is added in the outside of the closed loop and simply adjusts the command given to the existing DB control system. DB controller emphasizes on dynamic response, while RC specializes in improving steady-state tracking accuracy.

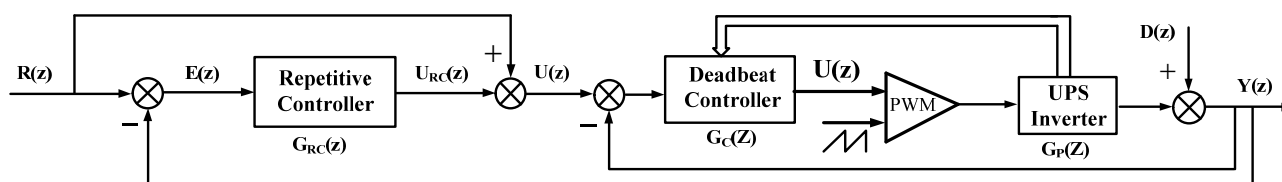


Fig.2. Block diagram of proposed hybrid learning controller

Principle of Repetitive Control

Repetitive control originating from the internal model principle is a well known solution for periodic distortions' rejection problem in a dynamic system [5]. A general closed loop system with an RC is illustrated in Fig. 4. In this figure, K_{RC} is the RC gain, $z^N \phi(z)$ is a compensator, $U_{RC}(z)$ is the output of RC, $Q(z)$ is a constant or a zero phase low-pass filter, $G_p(z)$ is plant and $N=f_f/f_s$ where f_f is the fundamental frequency of reference signal and f_s is the sampling frequency.

The stability analysis of the repetitive control action is ensured if the error signal e_r in the closed-loop operation is bounded [5, 6]. For the plant given in Fig.2, the transfer function of $E(z)$ can be computed as :

$$(5) E(z) = \frac{1 - z^{-N} Q(z)}{1 - z^{-N} H(z)} [(1 - G_p(z))R(z) - D(z)].$$

Where:

$$(6) H(z) \triangleq Q(z) - K_{RC} z^N \phi(z) G_p(z)$$

sufficient conditions for system stability can be derived by small gain theorem as follows [6]:

$$(7) |H(e^{j\omega T_s})| < 1$$

Error convergence rate and Steady-state tracking error are two key criteria to evaluate an RC's performance. Supposing $Q(z)=1$, due to periodic nature of reference and disturbance signals ($D(z)=z^{-N}D(z)$ & $R(z)=z^{-N}R(z)$), the error convergence can be derived from (6):

$$(8) E(z) = H(z)z^{-N}E(z)$$

Equ.8 implies after each fundamental period, magnitude of $E(z)$ is reduced to $|H(e^{j\omega T_s})|$ times of the original value. To achieve fast error convergence $|H(e^{j\omega T_s})|$ must be close to zero. $|H(e^{j\omega T_s})|$ is called error convergence index [5, 6]. Noting that at steady state, the tracking error is periodic, based on Equ.16 the steady-state error is obtained as:

$$(9) |E(e^{j\omega T_s})| = \left| \frac{1 - Q(e^{j\omega T_s})}{1 - H(e^{j\omega T_s})} \right| |(1 - G_p(z))R(z) + D(z)|$$

Based on quation (9), in steady state, the reference tracking error $|1-G_p(z)R(z)|$ and the error caused by the disturbance $|D(z)|$ are all reduced to $|1-Q(e^{j\omega T_s})|/|1-H(e^{j\omega T_s})|$ times of

their original values. $|1-Q(e^{j\omega T_s})|/|1-H(e^{j\omega T_s})|$ indicates harmonic rejection capability, and therefore is defined as harmonic rejection index [5, 6]. Note that it is also a function of frequency. For high performance Steady-state tracking error, harmonic rejection index must be designed to be close to zero.

instantaneous Feedback Controller Design

Fig.4 shows the proposed cascade deadbeat control scheme for UPS inverter [4]. It consists of two loops, the outer loop controls the output voltage, while the inner loop controls the inductor current. It is fundamental to underline that the sampling frequency of inner current loop is twice the outer voltage loop's sampling frequency. This avoids instabilities arising from the interaction between the internal current loop and the external voltage loop. Since the load's dynamics are unknown, the load current will act as a disturbance to the outer voltage loop, Thus decoupling of load current i_o is used for the outer loop. Similarly, the output voltage (v_o) acts as an exogenous disturbance in the current loop and output voltage's decoupling is used for the inner loop. Based on Fig.3, the open loop gain of current loop can be easily described as:

$$(10) G_i(z) = Z \left(\left[\frac{1 - e^{-T_s S}}{S} \right] \left[\frac{1/L}{S + \alpha} \right] \right) = \frac{1 - e^{-\alpha T_s}}{r_L z - e^{-\alpha T_s}}$$

Where $1 - e^{-T_s S}/S$ is transfer function of zero-order holder and $\alpha = r_L/L$. The characteristic Equation of the closed current loop is:

$$(11) G_i(z) = z - [e^{-\alpha T_s} - k_c \left(\frac{e^{-\alpha T_s} - 1}{r_L} \right)] = 0$$

we placed the root of the closed-loop system at the origin of z-plane to achieve deadbeat effect. The gain (K_C) is thus designed as [4]:

$$(12) K_C = \frac{r_L e^{-\alpha T_s}}{1 - e^{-\alpha T_s}}$$

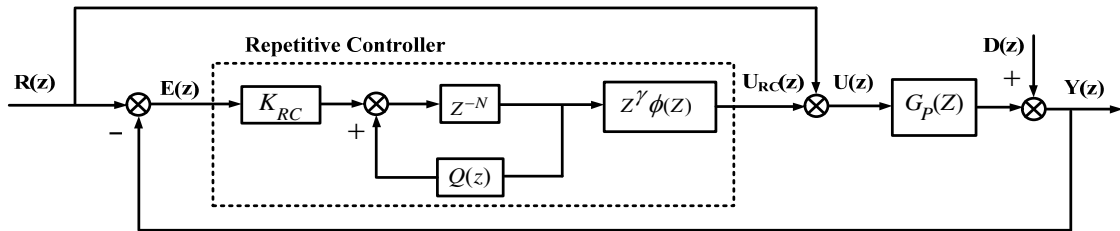


Fig.3. Block diagram of the repetitive controlled SPWM inverter system

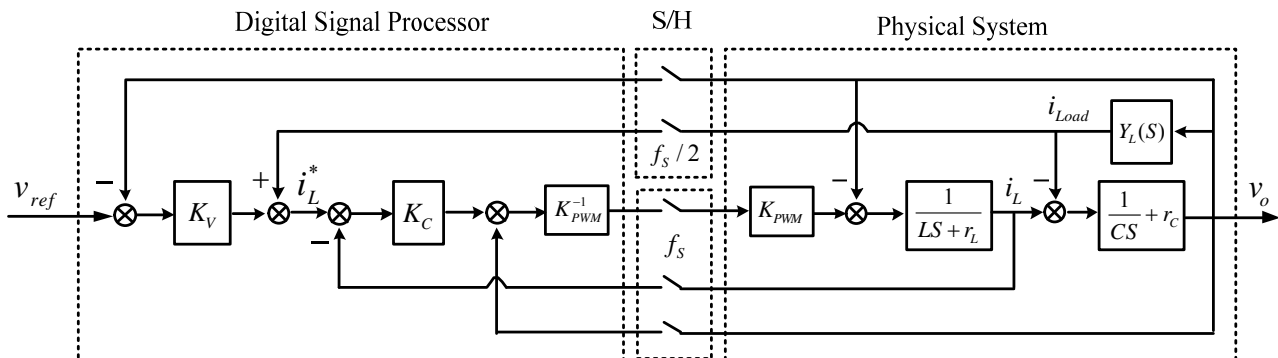


Fig.4. Block diagram of proposed hybrid learning controller

Due to its fast dynamics, the designed inner loop can follow the current command faithfully, So in the design of the outer voltage loop, the inner loop voltage is assumed as a constant gain (K_C) for design of outer voltage loop. Under this assumption, the open voltage can be easily described as[4]:

$$(13) \quad G_v(z) = Z \left(K_C \cdot K_V \left[\frac{1 - e^{-2T_s S}}{S} \right] \left[r_c + \frac{1}{SC} \right] \right)$$

Where $1 - e^{-2T_s S}/S$ is the transfer function of zero-order holder with $0.5f_s$ sampling frequency. Similarly, the gain (K_V) is designed through deadbeat theory as follows [4]:

$$(14) \quad K_V = \frac{C}{2T_s - Cr_c}$$

Finally, the transfer function of closed loop system, can be computed Based on Equ.1 and Fig.3 as:

$$(15) \quad V_o(s) = \frac{k_v k_c (Cr_c + 1)}{LCs^2 + C(k_c(k_v r_c + 1) + r_L)s + k_v k_c} V_{ref}(s) + \frac{-r_c LCs^2 + (Ck_c r_c - Cr_c r_L - L)s + (k_c - r_L)}{LCs^2 + C(k_c(k_v r_c + 1) + r_L)s + k_v k_c} I_o(s)$$

Case Study Design for hybrid controller

The parameters of the system are listed in Table 1. Based on Equ.1 and using bilinear transform, the digital model of the inverter in no-load condition is :

$$(16) \quad G_p(z) = \frac{0.2526z + 0.1848}{z^2 - 1.41 + 0.8465}$$

As shown in Fig. 5, the transfer function has a resonant peak of about 12.4 dB at a frequency of 5200 rad/s. Based on Eq.13 and Eq. 15, the gain of voltage and current loops are computed as $K_V=1.477$ and $K_C=2.9503$ respectively. Based on Eq.16 The closed loop transfer function of DB controlled system is:

$$(17) \quad G_{FB}(z) = \frac{0.5026z + 0.1745}{z^2 - 0.4261z + 0.1031}$$

Frequency response of deadbeat controlled system is shown in Fig.5. The bandwidth of the system is about 7800 (rad/sec).

Table 1. Parameter of plant

Parameter	Symbol	value
Rated RMS voltage	V_{ref}	110 (RMS)
Reference sin frequency	f_f	50 Hz
Rated power	P_{out}	3 KW
Filter inductor	L	200 μ H
ESR of Filter inductor	r_L	0.2 Ω
Filter capacitor	C	180 μ F
ESR of Filter capacitor	r_C	0.05 Ω
Switching frequency	f_{sw}	15 kHz
Sampling frequency	f_s	15 kHz
DC link voltage	V_{dc}	250 V

The compensator (i. e. $z\phi(z)$) is designed to compensate the plant to Satisfy stability condition and achieve fast error convergence. Thus we need to make error convergence index $|H(e^{j\omega T_s})|$ as small as possible, ideally this can be achieved by setting:

$$(19) \quad e^{j\gamma\omega T_s} \phi(e^{j\omega T_s}) G_{FB}(e^{j\omega T_s}) = 1 \quad \omega \in [0, \pi f_s]$$

In this case, a simple IIR low pass filter can be used as the LPF part of compensator. Hence $\Phi(z)$ is selected as:

$$(20) \quad \phi(z) = \frac{0.09131z^2 + 0.1826z + 0.09131}{z^2 - 0.9824 + 0.3477}$$

Frequency response of $\phi(e^{j\omega T_s}) \cdot G_{FB}(e^{j\omega T_s})$ is shown in Fig. 5. Next, the time-advance unit (z^γ) is determined according to the phase characteristics of $\phi(e^{j\omega T_s}) \cdot G_{FB}(e^{j\omega T_s})$. It is selected to compensate the phase lag of $\phi(e^{j\omega T_s})$.

$G_{FB}(e^{j\omega T_s})$. Based on fig. 5 , z^3 is selected for time-advance unit.

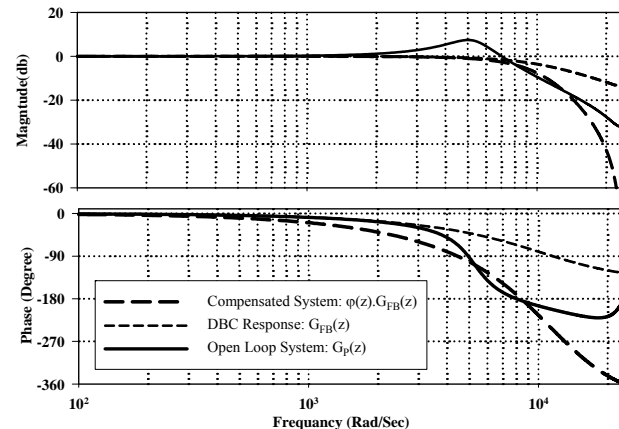


Fig.5. Frequency response of system

RC's gain (K_{RC}) significantly affects error convergence rate and harmonic rejection capability. Based on Equ. 6, if K_{RC} is selected to be a constant that is close to unity, very fast error decay can be expected for frequencies of up to almost the filter cutoff frequency. A too small (or too high) value of K_{RC} , yields a poor error convergence rate and smaller stability margin. The exact value of K_{RC} for achieving fast error convergence can be selected based on experimental/simulation testing. We set $K_{RC}=1$.

$Q(z)$ directly indicates the steady state tracking error and stability margin of the repetitive controller. Based on Equ.10, $Q(z)$ must be designed very close to unity within a wide frequency range to have zero steady-state error. But for increasing stability margin (Equ. 6) $Q(z)$ can be set to a close-to-unity constant, typically 0.95. This effectively increases the stability margin, but at the cost of non-zero steady-state error. A zero-phase FIR filter is another choice for $Q(z)$. In this case, zero steady-state error and good stability margin can be achieved. Locus of vector $|H(e^{j\omega T_s})|$ is shown in Fig. 6 for $K_{RC}=0.95$ and $Q(z)=0.25z^{-1}+0.5+0.25z^1$. This figure confirms that zero-phase FIR filter is a better choice for stability margin.

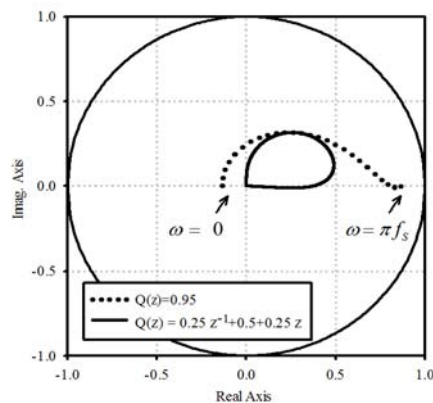


Fig.6. Locus of vector of $|H(e^{j\omega T_s})|$

Simulation Results

To verify the validity of the proposed repetitive control strategy, MATLAB/Simulink simulations are carried out under the test conditions of the International Electrotechnical Commission Standard 62040-3. Fig.7 shows the steady-state response of the proposed hybrid controller for rectifier load. It should be noticed that the output voltage contains only a little amount of high-frequency harmonics.

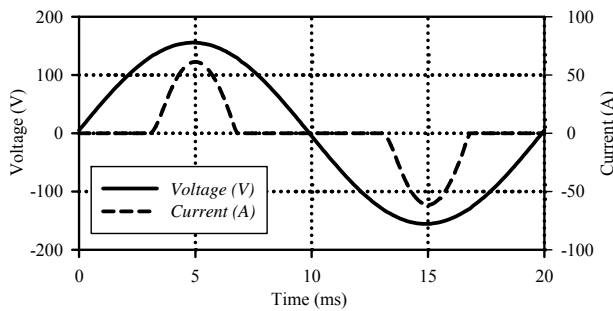
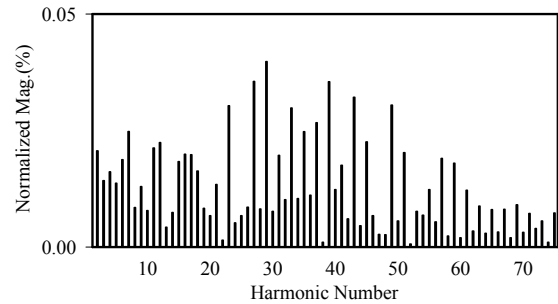


Fig.7. Steady state test Single-phase uncontrolled rectifier at 2.1 kVA, THD=0.19%



Based on Table 2, the output voltage THD was 7.8% and 2.45% for open-loop and deadbeat controller respectively, while with the proposed hybrid controller the THD is decreased to 0.19%.

Table 2. THD% of output voltage for nominal non-linear load

Controller	Open loop control	Deadbeat Controller [5]	Proposed Method
THD%	7.8	2.45	0.19

Fig. 8 shows the simulation results for step linear loading from 20% to 100% rated output active power (at $t=65\text{ms}$) and load removal from 100% to 20% ($t=165\text{ms}$). The undershoot related to the step load is below 8% and it settles down at 0.4ms. The overshoot due to the step load removal is also below 9% of rated voltage and it settles down after 0.3ms. It can also be seen that the error convergence speed of hybrid RC is also fast. Only about one fundamental cycles are needed for error convergence.

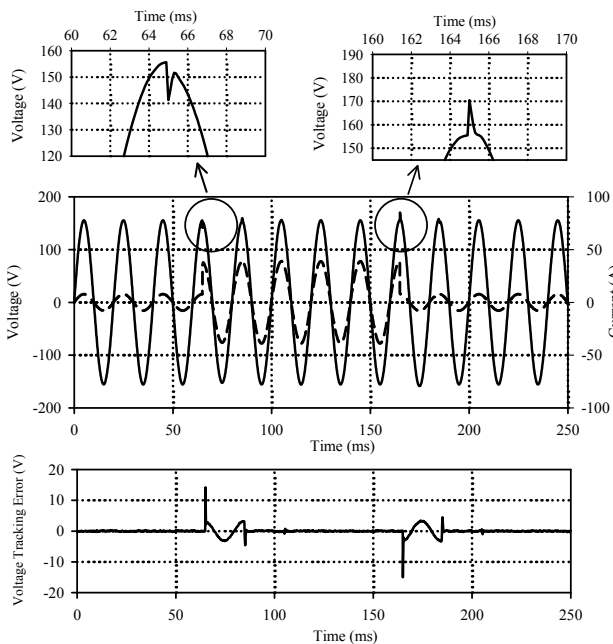


Fig.8. Linear load step from 20% to 80% and 80% to 20%

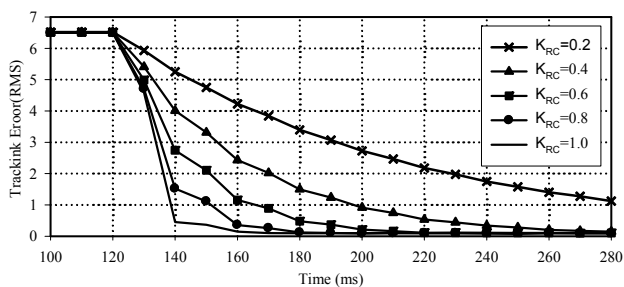


Fig.9. Tracking error convergence with different value of k_{RC}

Conclusion

In this paper, a repetitive controller (with zero-error tracking capability) linked with a deadbeat controller (with fast transient response) in cascade configuration is proposed and successfully applied to a UPS inverter. A zero-phase non-causal FIR filter $Q(z)$ is placed on the positive feedback path inside the RC to improve the robustness of the whole system. Simulation results shows that the proposed controller can achieve very low THDs (0.19% in the Worst case) and fast error convergence (less than three fundamental cycles) and good dynamic response. The proposed controller can also be applied to other power electronic applications such as PWM rectifier, grid connected inverter and active filters.

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Authors: Mohammad Javad Qanaatian, MSc Student of electrical engineering, Iran University of Science and Technology, Tehran, Iran, E-mail: ghanaatian@yahoo.com.

Associate professor Abdoreaz Rahmati, School of electrical engineering, Iran University of Science and Technology, Tehran, Iran, E-mail: rahmati@iust.ac.ir