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Design and analyses of a low power linear voltage regulator in 0.18um CMOS process

Abstract. *Linear voltage regulator is inevitable in most electronic systems and demands low power and low area. A low dropout (LDO) linear voltage regulator is proposed in this paper by utilizing Current Feedback Amplifier (CFA) technology. The design achieves low power and low area by reducing the internal compensation capacitor and resistors. The simulated result shows that the design consumes only 567.1370pW which is 35% less than the reference circuit. The design also achieves low area and higher gain.*

Streszczenie. *W artykule omówiono liniowy regulator napięcia wykorzystujący koncepcję LDO (low dropout). Układ wykorzystuje wzmacniacz z prądowym sprzężeniem zwrotnym CFA I technologię CMOS. Zrealizowano układ pobierający o 35% mniej energii niż układy znane z literatury.* ***Projekt i analiza regulatora napięcia o małym poborze mocy wykonanego w technologii CMOS 0.18 μm***

Keywords: CMOS, low dropout, voltage regulator.
Słowa kluczowe: regulator napięcia, low dropout, technologia CMOS
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Introduction

System on Chip (SoC), modern communication systems including Wireless Local Area Network (WLAN), Radio Frequency Identification (RFID) etc are becoming increasingly popular day by day [1-4]. These systems demands low cost, high integrability and small size [5,6]. Power management is an essential device in these systems. Over-load protection, over-heat shield, stabilization, low power and low area are the essential features of the power management devices to assure the correct operation of these systems [7].

The rapid advancement of Complementary Metal Oxide Semiconductor (CMOS) technology allows power management devices to achieve these criteria [8-10]. LDO linear voltage regulator is widely used in power management devices [11]. LDOs are one of the most critical modules as it is able to provide a nearly constant DC voltage for all the electronic systems. To regulate the performance (line and load regulation) transient overshoot and undershoot are required. On the other hand, to characterise, the power (output current, quiescent current, input and output voltage, and power and current efficiency) is necessary. Therefore, the LDOs need to be carefully designed to enhance the system stability in various operating condition.

LDOs contain the error amplifiers to detect the error between the output voltage and the reference. Error amplifier controls the pass transistor when the current passes through the output capacitor. Fast rejection of steep transient load variations, input voltage and loads are the metrics needed to be fulfilled when designing the LDO [12,13]. There are several methods to design the LDO such as pole-zero cancellation method, dual loop feedback and current-mode feedback buffer amplifier, voltage current source and flipped voltage follower to improve the stability and transient response [14-16]. Saberkari et al. proposed a current feedback amplifier for the fast transient response and regulation [17]. Dynamic biasing of derivative feedback was used in an ultra low power capless LDO by Jorge et al. [18]. Wang et al. improved the operating frequency by using the nested feedback loops in LDO linear voltage regulator [19]. However, none of the design could avoid numerous resistors and capacitors. A low power LDO linear voltage regulator is proposed in this paper by reducing the number of the resistors and capacitors by utilizing the CFA technology.

Methodology

The proposed LDO linear voltage regulator is the modification of the [17] as shown in Fig. 1. The reference circuit was built up using CFA topology. Open-loop voltage follower with output local current feedback based on a level-shifted slipped voltage follower (LSFVF) includes in CFA.

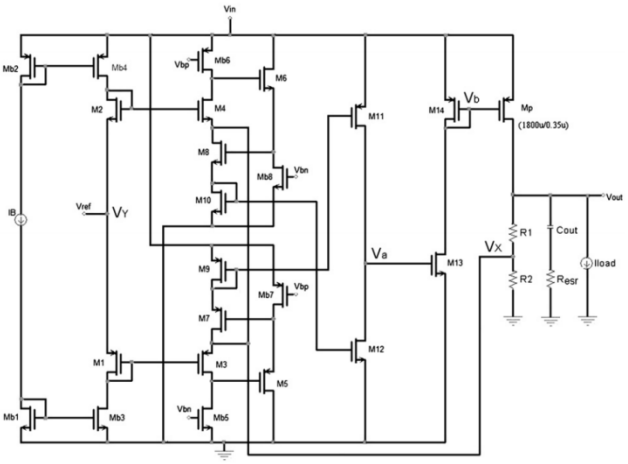

Fig.1. Reference circuit diagram [17]

The CFA consists of a pass transistor Mp, a class AB voltage follower M1-M12, an inverting output buffer (M13, M14). There are two feedback networks in that circuit which is R1 and R2. V_{ref} is fed into the circuit to ensure no DC current drain. When load current increases, Vout is decreased. At the same time, the terminal voltage at M3, M4 and gate voltage M7, M8, M5 and M6 is also affected. The current passes through transistors (M7, M9, and M11) but the current is decreased at transistor M8, M10, M12. The voltage is increased at M13 but decreases at Mp.

The proposed design reduces the complexity of the above mentioned circuit by reducing resistors and internal compensation capacitor. The schematic diagram of the proposed LDO linear voltage regulator is shown in Fig. 2. The parameters used for the proposed design are Resr=2kΩ, Vbp, Vbn and Vref =3V.

Result and Discussion

The proposed voltage regulator was designed and simulated in 0.18-μm CMOS process with the Design Architect (DA-IC) and IC station tools of Mentor graphics. The 27^0C operating condition has been set for the reference LDO and the proposed LDO. The width and length of the transistors are shown in Table 1.

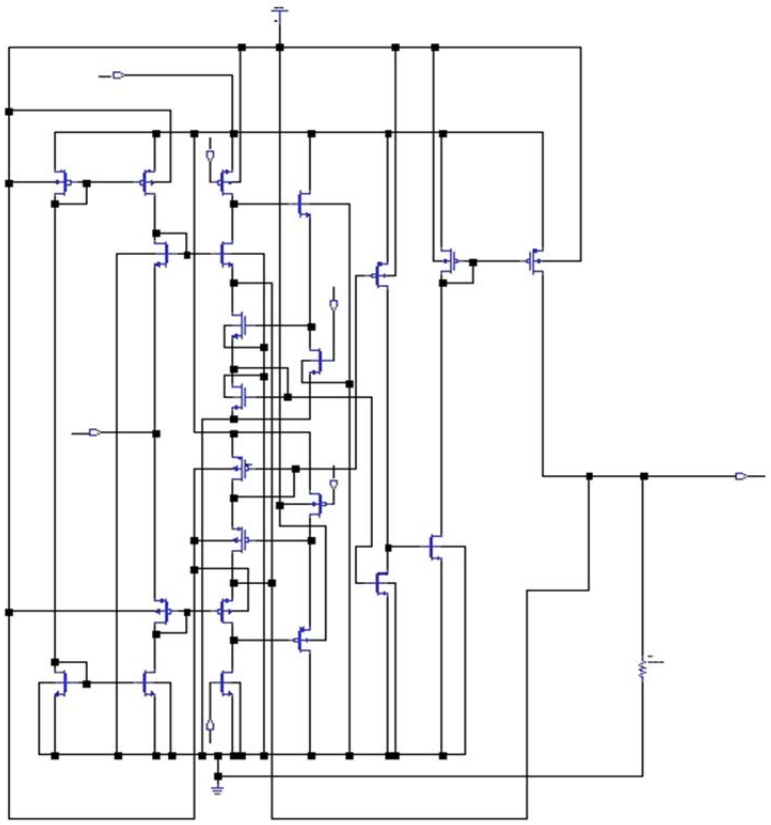

Fig.2. Schematic diagram of the proposed LDO linear voltage regulator

Table 1: Width and Length of the transistors

Transistor	Size (Width/Length)um
Mb2, Mb4, M2, Mb6, M4	7.5/0.25
Mb1,M1, Mb3, M3, Mb5	15/0.25
M8, M6, M11	1.4/0.25
M10, M9, Mb7	0.5/0.18
M7	3.4/0.25
Mb8	1.65/0.25
M5	2.85/0.25
M12	1.4/0.18
M14	0.75/0.18
M13	0.1/0.25
Mp	50/0.18

By using, the critical design parameters listed in Table 1, the output data V(out) for the modified LDO is shown in Fig.3 with supply voltage of 4 V. From Fig. 3 it is clear that, the output voltage is V(out) = 3.6 V after providing the 4V as the input voltage.

Figure 4 shows the V(out) when the input supply voltage is 5 V. However, the proposed LDO is able to produce 3.7V as the output voltage at this stage. The Vout before and after modification of the circuit is only 0.1V which does not differ much. Therefore, it is found that the design is sufficient enough to generate a good LDO regulated linear voltage output.

The gain between the reference LDO and the proposed LDO is compared to justify the better performance of the proposed design. Table 2 shows the comparison result of the gain between the reference circuit and the proposed circuit.

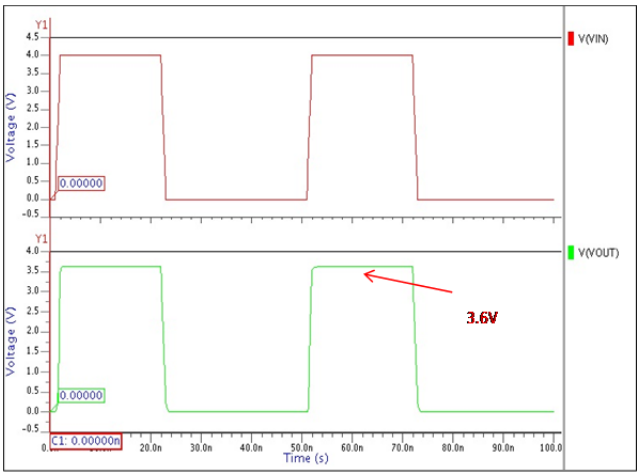

Fig. 3.Simulated output voltage with a 4V input voltage

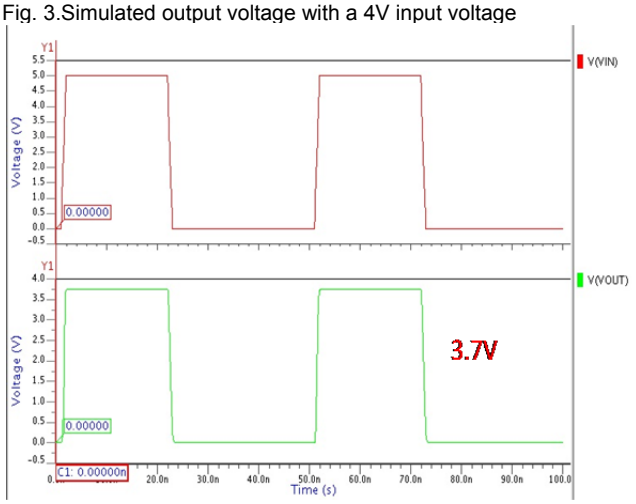

Fig.4. Simulated output voltage with a 5V input voltage

Table 2. Comparison between the reference and proposed circuit

	[17]		Proposed circuit	
	Vin=4V, Vout=2.8V	Vin=5V, Vout=2.8V	Vin=4V, Vout=3.6V	Vin=5V, Vout=3.7V
Gain	0.7	0.56	0.9	0.74
Gain dB	-1.55	-2.52	-0.46	-1.31

Based on the above result, the gain of the proposed circuit is better than the reference circuit. This is because the linear voltage regulator is a step-down converter. The proposed design also outperforms in power dissipation due to the reduction of resistors and capacitor. Table 3 shows the power dissipation of the proposed design with the reference circuit.

Table 3. Comparison of the power dissipation

	[17]	Proposed
Power dissipation (P Watts)	867.1987	562.1370

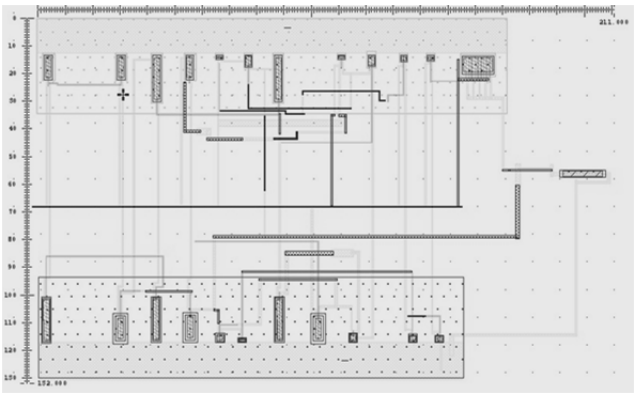

Fig. 5. Layout diagram of the proposed LDO voltage regulator

The usage of the resistors and capacitors increase the power dissipation. Based on Equation (1), chip junction temperature increases with the higher power dissipation.

$$T_j = T_A + (R_{\theta JA} x P_D) \quad (1)$$

where, PD is the power dissipation in package (W), TA is ambient temperature for the package (°C) and R θJA is junction to ambient thermal resistance (°C/W).
The layout of the proposed LDO linear voltage regulator was drawn with IC Station of Mentor Graphics as shown in Fig. 5. The transistors were drawn according to the calculated width and length of Table 1. The area of the proposed design was found only 311µm x 132µm.

Conclusion

An improved LDO linear voltage regulator is presented in this paper. The modified circuit has been designed by using the CEDEC 0.18µm CMOS process. The design is capable of working under a voltage range from 4V to 5V. The power dissipation of the proposed design is only 562.1370pW which is 35% lower than the reference circuit. Additionally, the circuit is able to produce higher gain than the reference circuit. The design also achieves low area as the resistors and capacitor are avoided.

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