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A New Bandgap Voltage Reference Circuit using CMOS Differential Voltage Current Conveyor

Abstract. *This paper proposes a new approach of bandgap voltage reference (BGR) circuit design by using CMOS differential voltage current conveyor (DVCC). The proposed circuit employs single DVCC, which is able to reduce the number of devices used to bandgap core and start-up circuits. The simulation results indicate reference voltage of about 500mV, temperature coefficient (TC) of 20ppm/℃, which can be successfully operated with a minimum supply voltage of 1.2V in a temperature range of 0-100℃ and a total power dissipation of 56.6 μW at room temperature.*

Streszczenie. *Opisano pasmowy wzorzec napięcia NBGR zaprojektowany w technologii CMOS z wykorzystaniem układu DVCC (differentia voltage current conveyor).Zaprojektowany wzorzec umożliwia uzyskanie napięcia ok. 500 mV ze współczynnikiem temperaturowym 20 ppm/^{o}C przy minimalnym napięciu zasilającym 1.2 V przy poborze mocy 56 uV.* ***Pasmowy wzorzec napięcia wykorzystujący układ DVBCC***

Keywords: Band gap voltage reference, BGR, DVCC, CMOS, POR.
Słowa kluczowe: wzorzec napięcia, układ DVBVCC, technologia CMOS

doi:10.12915/pe.2014.08.19

Introduction

Bandgap voltage reference (BGR) is one of the most popular circuits are used for many applications of both analog and digital circuits such as A/D, D/A, DRAM and flash memories. The low-power and low-voltage operations are increasingly in demand for smaller portable devices. Bandgap voltage reference can be successfully applied to stabilize over supply voltage, process and temperature variations. The output voltage of the conventional BGR circuit is usually of about 1.2V [1], measured in electron volts, which is almost equal to the silicon energy gap and cannot be used in the latest deep-submicron technologies. In the conventional designs and implementations of the BGR circuit consists of four parts: bandgap core, startup, voltage summation and output state. The bandgap core circuits are almost the same design as reported in [2], the startup circuits are designed by different methods and techniques which consists of several transistors and complicated circuits [3-7], and voltage summation circuits are designed by using the different active building blocks. At the beginning, operational amplifiers (op-amps) were the basis of many active building blocks [8-11] and originally used for error amplifiers in bandgap reference circuits [12-15]. There are several practical limitations which many researchers reported in literature [16-19]. The operational transconductance amplifier (OTA) is one of the active building blocks are used in BGR circuits [20-21], however the OTA still has disadvantages of narrow dynamic range, low current drive capability and worse linearity compared with CCII [22-23]. And the second-generation current conveyor (CCII) can be used to replace the conventional op-amp in the BGR circuit [24], due to the CCII has low impedance at X terminal and high impedance at Y terminal but the error amplifier of BGR circuit also require two high input impedance terminals. Therefore, this paper presents a new bandgap voltage reference circuit using CMOS differential voltage Current Conveyor (DVCC). Due to, the DVCC provides two high input impedance terminals [25-26], lower power consumption, greater linearity, larger dynamic range and better accuracy with circuit solutions for low supply voltage operation and achieve the correct biased point at power-on.

Basic concept of BGR.

Fig. 1. shows basic structure of BGR circuit which consists of bandgap core, startup, voltage summation and output stages. The base-emitter voltage (V_{BE}) of bipolar junction transistor (BJT) is reduced with increasing temperatures of about -2mV/ºC, which is called complementary to absolute temperature (CTAT).

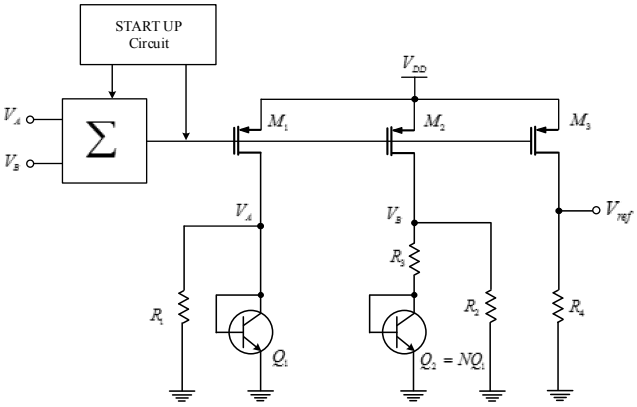

Fig.1. Block diagram of a bandgap voltage reference

The $V_T = kT/q$ is thermal voltage, k is Boltzmann's constant (1.38*10^{-23} J/ºK), q is magnitude of electron charge and T is the absolute temperature, the V_T is proportional to absolute temperature (PTAT).

$$V_{ref} = R_4\left(\frac{V_{BE}}{R_2} + \frac{KV_T}{R_3}\right) \tag{1}$$

From (1), it is found that the output voltage is independent of temperature and power supply variations. If the gain K is set correctly, the stable voltage reference (V_{ref}) can be achieved by summation of the CTAT and PTAT voltages.

Proposed circuit

The DVCC symbol is shown in fig.2. is four terminals building block, which is described by following matrix equation:

$$\begin{bmatrix} V_X \\ I_{Y_1} \\ I_{Y_2} \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \pm 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y_1} \\ V_{Y_2} \\ V_Z \end{bmatrix} \tag{2}$$

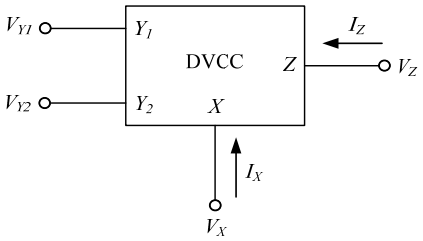

Fig. 2. DVCC symbol

From electrical characteristics of DVCC follow equation (2), the voltage (V_X) at X terminal is equal to different voltage of V_{Y1} and V_{Y2} terminals, the current (I_X) at X terminal is transferred to the output current (I_Z) at Z terminal. An ideal properties of DVCC are infinite input resistance at the Y_1, Y_2 and Z terminals and zero resistance at X terminal. As a result of features mentioned above, the op-amp is used for voltage summation in the conventional BGR circuits, can be replaced by DVCC.

The internal schematic of proposed DVCC is shown in fig. 3.

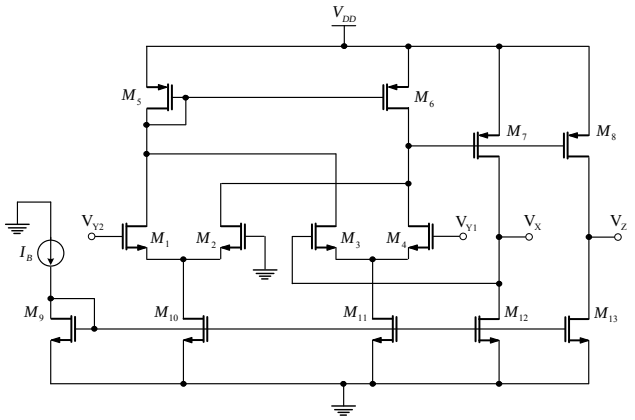

Fig. 3. CMOS Differential Voltage Current Conveyor (DVCC)

Temperature dependence of BJT.

A typical BJT, the voltage across base-emitter can be expressed as

$$V_{BE} = V_T \ln \frac{I}{I_S} \tag{3}$$

$$I_S = CT^{\gamma} e^{-\frac{V_{G0}}{V_T}} \tag{4}$$

$$V_T = \frac{kT}{q} \tag{5}$$

where I_S is saturation current, C and γ are temperature-independent constants, V_{GO} is Band-gap voltage of silicon (1.205V), V_T is thermal voltage, k is Boltzmann's constant ($1.38*10^{-23}$ J/ºK), q is magnitude of electron charge ($1.6*10^{-19}$ C) and n is slope factor.

Substituting equations (4) and (5) into (3) then differentiating with respect to temperature, the result is

$$\frac{\partial V_{BE}}{\partial T} = \frac{1}{T}\left[V_{BE} - \frac{k}{q}\left(\frac{V_T V_{GO}}{T} + \gamma\right)\right] \tag{6}$$

Equation (6) shows that the base-emitter voltage (V_{BE}) decreases by increasing the temperature and V_{BE} has a negative temperature coefficient. The thermal voltage (V_T) has a positive temperature coefficient of $0.086mV/°C$ can be written as

$$\frac{\partial V_T}{\partial T} = \frac{k}{q} \tag{7}$$

Bandgap core circuit analysis

The bandgap core circuit shown in fig. 4 consists of two resistors and two BJTs, different from other reports [2-3, 7-11, 16-17, 20]. In literature, a bandgap core circuits were designed by voltage setting of V_{Y1}=V_{Y2}, current I_1=I_2, resistance R_X=R_2 and very large emitter area of BJT for generating the CTAT and PTAT currents. The currents I_1 and I_2 are sum of I_{CTAT} and I_{PTAT}.

In this paper, The BGR core circuit is designed by setting of voltage only node V_{Y2} under conditions of temperature cancellation of I_{PTAT} and I_{CTAT} which are the currents flow through resistors R_1 and R_2, respectively. The proposed BGR core circuit is defined to operate under condition of

$$I_1 = I_2 \tag{8}$$

$$V_{Y1} = V_{Y2} \tag{9}$$

The $V_{BE_{Q1}}$ is equal to

$$V_{Y1} = V_{BE_{Q1}} = V_T \ln \frac{I_1}{I_S} \tag{10}$$

The $V_{BE_{Q2}}$ is equal to

$$V_{BE_{Q2}} = V_T \ln \frac{I_{R1}}{mI_S} \tag{11}$$

Define the $V_{Y1} = V_{Y2}$

$$V_{BE_{Q1}} = V_{Y2} = V_{R1} + V_{BE_{Q2}} \tag{12}$$

The voltage across V_{R1} is proportional to V_T and has a positive temperature coefficient can be written as:

$$\Delta V_{BE} = V_{R1} = V_T \ln \frac{I_1}{I_S} - V_T \ln \frac{I_{R1}}{mI_S} = V_T \ln \frac{mI_1}{I_{R1}} \tag{13}$$

where m is emitter area ratios of Q_1 and Q_2. From eq. (13), it is seen that the m parameter of proposed circuit can be reduced by controlling the current ratios of I_1 and I_{R1}, this is simple practical method for reducing the emitter area of Q_2. Thus, the current I_{PTAT} can be expressed as

$$I_{PTAT} = I_{R1} = \frac{V_T}{R_1} \ln \frac{mI_1}{I_{R1}} \tag{14}$$

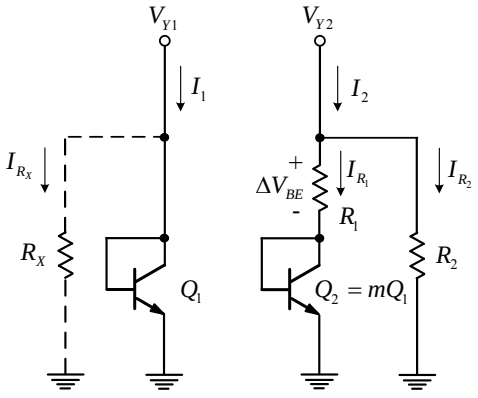

Fig. 4. Bandgap core circuit

The current I_{CTAT} or I_{R2} is equal to:

$$I_{CTAT} = I_{R2} = \frac{V_{Y2}}{R_2} = \frac{V_{Y1}}{R_2} = \frac{V_T}{R_2}\ln\frac{I_2}{I_S} = \frac{V_{BE_{Q1}}}{R_2} \quad (15)$$

$$I_2 = \frac{V_T}{R_1}\ln\frac{mI_1}{I_{R1}} + \frac{V_{BE_{Q1}}}{R_2} \quad (16)$$

From equation (16), it is clearly seen that the currents I_{PTAT} and I_{CTAT}, without the resistor (R_X) which is connected to node V_{Y1}. Thus, this design can be reduced the number of resistor and resistor mismatch in bandgap core circuit.

Table 1. Components and transistor dimensions used in the design.

Components	Size :W/L(μm) and Values
$M_{1\text{-}4}$	50/5
$M_{5\text{-}6}$, $MP_{1\text{-}4}$	10/5
$M_{7\text{-}13}$,	5/5
$MN_{5\text{-}6}$	20/5
Q_1	Area=1
Q_2	Area=6
R_1	30k
R_2	475k
R_3	1k
R_4	500k
R_5	150k

Circuit design

The proposed BGR circuit using CMOS DVCC is shown in fig. 6. The current I_X at X terminal is controlled by resistor R_3 and transferred to the output current (I_Z) at Z terminal as the DVCC properties. The current I_Z will be mirrored to I_{D6} which is set equal to I_1, I_2 and I_{out} due to the gate of transistors (MP_1-MP_4) are connected to a common node. The electrical characteristics of the DVCC from eq. (1) can be rewritten as

$$V_X = V_{Y1} - V_{Y2}\,,\; I_{y1} = 0\;\; I_{y2} = 0\,,\; I_Z = I_X \quad (17)$$

The output current (I_Z) of DVCC equal to I_X. Thus, the current I_2 can be expressed as

$$I_2 = I_X = \frac{V_{Y1} - V_{Y2}}{R_3} = \frac{V_T}{R_1}\ln\frac{mI_1}{I_{R1}} + \frac{V_{BE_{Q1}}}{R_2} \quad (18)$$

From eq. (18), the current I_2 is set equal to I_{out}. Thus, the V_{ref} can be expressed as

$$V_{ref} = \left(\frac{V_T}{R_1}\ln\frac{mI_1}{I_{R1}} + \frac{V_{BE_{Q1}}}{R_2}\right)R_5 \quad (19)$$

The temperature independent voltage reference (V_{ref}) are sum of the currents I_{PTAT} and I_{CTAT} multiplied by the resistance R_5. Therefore, the voltage levels of reference voltage (V_{ref}) can be obtained by changing the value of resistance (R_5).

Simulation Results

To confirm the circuit performance and theoretical validity of the proposed circuit verified through PSPICE simulation results using TSMC 0.35μm CMOS technology, the NPN transistors employed in the proposed circuit were simulated by using the parameters of NR200N bipolar transistors. The Fig. 5. shows reference voltage of about 500mV and voltage variation less than 0.6mV, at temperature range from 0-100ºC. The temperature coefficient of about 20ppm/ºC and power dissipation is only 56.6uW.

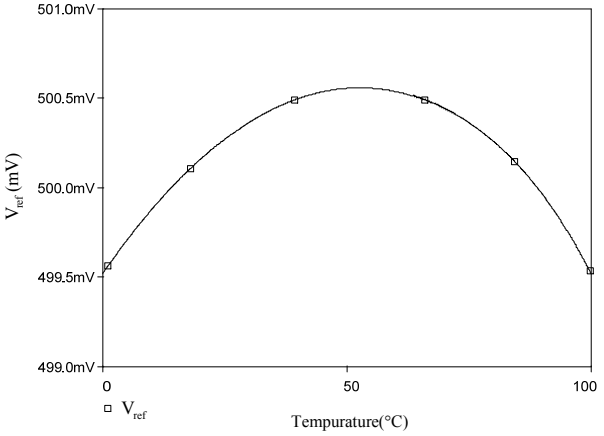

Fig. 5. Temperature dependence of output reference voltage

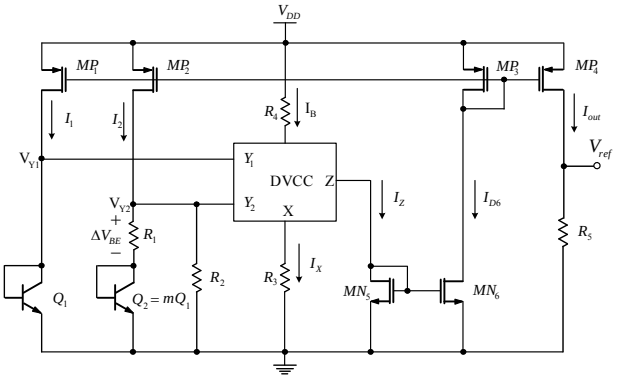

Fig. 6. Schematic of the proposed bandgap voltage reference circuit

Fig. 7. shows the currents of I_{R1} or I_{PTAT} and I_{R2} or I_{CTAT} has a positive and negative temperature coefficient, respectively, at operating temperature range from 0-100ºC. The current I_{R1} is summed with I_{R2} to create a reference current of I_2 and is set equal to I_1 and I_{out}, then flows through a resistance (R_5) to generate the reference voltage of V_{ref}.

Fig. 8. shows the voltages at each node of the proposed circuit. The BGR circuit operation, the start-up circuit can be operated at supply voltage of about 1.2V. The voltages V_{Y1} and V_{Y2} are controlled to the same voltage. The proposed circuit can be achieved the stable reference voltage (V_{ref}), although the supply voltage is varied from 1.2V to 4.0V.

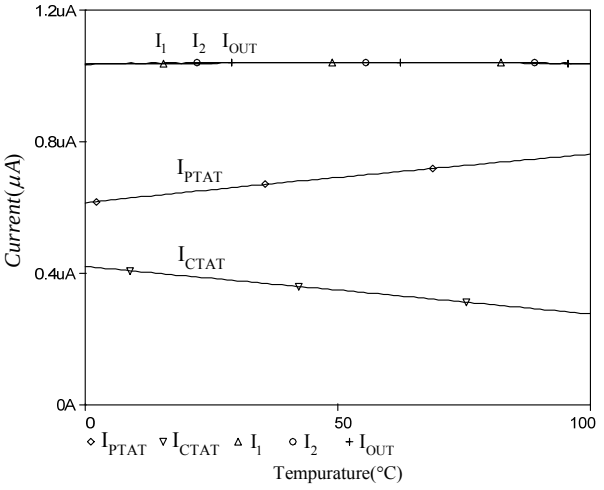

Fig. 7. Current flows through each branch

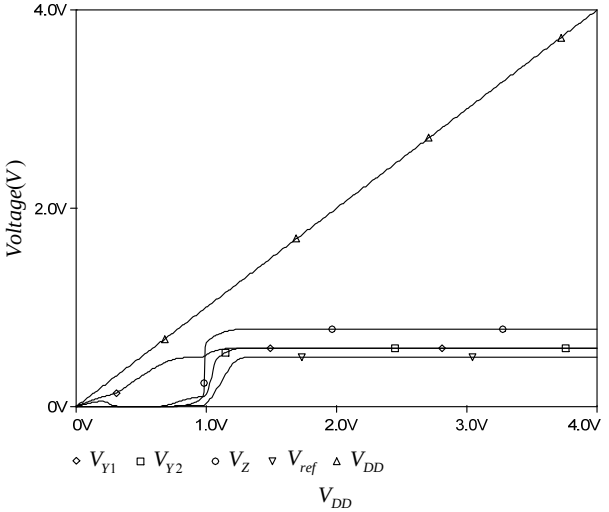

Fig. 8. Supply voltage variations at each node of the proposed circuit.

Conclusions

The Bandgap voltage reference circuit using CMOS differential voltage current conveyor has been presented. The current in any branches are easily controlled by the current I_X. The emitter area of Q_2 (m parameter) can be greatly reduced by controlling the current ratio of I_1 and I_{R1}. This design can be reduced the number of resistor and resistor mismatch of R_2 which is set equal to R_X. The minimum supply voltage has been achieved of about 1.2V and power dissipation is only 56.6uW. The reference voltage (V_{ref}) can be set at any level from almost 0V to V_{DD} by changing the resistance value (R_5). The simulation results show that the proposed circuit is suitable for low-power and low-voltage applications.

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