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Measurement subsystem for evaluation of local atomic clocks quality

Abstract. *We present the design, implementation and test results of a new measurement system for continuous evaluation of atomic clocks quality and selection of the best one as a local reference clock that operation is coordinated with the governmental time scale created in National Metrology Institute. The described system is developed as a part of the project called Legal Time Distribution System performed within European program EUREKA.*

Streszczenie. *W artykule opisane są projekt, sposób realizacji oraz wyniki badań eksperymentalnych systemu pomiarowego do ciągłej ewaluacji jakości atomowych źródeł zegarowych i wyboru źródła referencyjnego, którego działanie jest koordynowane z urzędową skalą czasu. Opisany system został opracowany jako część projektu System Dystrybucji Czasu Urzędowego realizowanego w ramach europejskiego programu EUREKA.* (***Podsystem pomiarowy do weryfikacji parametrów lokalnych atomowych źródeł sygnału zegarowego***)

Keywords: precise time metrology, time and frequency distribution, time-to-digital converters, programmable devices.
Słowa kluczowe: precyzyjna metrologia czasu, dystrybucja czasu i częstotliwości, przetworniki czasowo-cyfrowe, układy programowalne.

Introduction

Dynamic development of information society requires still more and more precise synchronization of communication systems, financial processes, electronic signatures, traffic management systems, etc. Many operations within areas mentioned above have to be performed based on certified time scale, created and made available to users by National Metrology Institutes (NMIs), for example by Central Office of Measures (Główny Urząd Miar) in Poland. In order to provide access of any institution, or even individual user, to legal and highly precise time scale a unique Legal Time Distribution System (LTDS) is being developed within the European program Eureka. In this article we present a novel measurement subsystem for permanent evaluation of local clock sources quality and selection of the reference one. In further part of this text it is called the Clock Evaluation Subsystem (CES). The CES is a main part of the End User Unit (EUU) of LTDS.

The LTDS involves two main segments, i.e. the control segment that is located in NMI, and the users segment, which includes users of certified time that are equipped with special EUUs. The control segment (fig. 1) contains: (1) Global Navigation Satellite System (GNSS) receiver that evaluates relation between global time scale distributed via satellites and time scale created in NMI, with the use of Common View method [1]; (2) control and computing system that calculates time difference between NMI time and local time, generated in EUU; (3) end user communication unit that provide safe, coded data transmission between control segment and EUU; (4) data storage unit that collects measurement data; and (5) web presentation unit that allows to present operation data of individual EUUs.

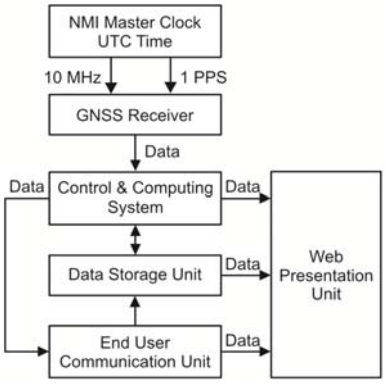

Fig.1. Control segment of LTDS

End User Unit

The EUU provides the user with access to legal and precise time scale. Typical way to achieve this goal is based on synchronization of locally created time scales to the national time scale. The EUU (fig. 2) contains: (1) CES; (2) GNSS receiver; (3) Network Time Protocol (NTP) or Precision Time Protocol (PTP) server; and (4) control computer. The control computer sends/receives data to/from NMI via Ethernet and also controls the rest of modules of the EUU. The main aims of the CES are continuous verification of parameters of local clocks, evaluation their stability, and finally selection of the most stable as a local reference clock. The GNSS receiver measures the phase difference of the local clock signal versus the reference signal synchronized to GPS/Galileo system. The result of measurements can be used to adjust the frequency and synchronize the phase of a local clock. On the basis of the active local reference clock signal, the time server distributes the time information using the NTP/PTP protocol. There are also direct 1 PPS and 10 MHz output signals, which are available to the local user.

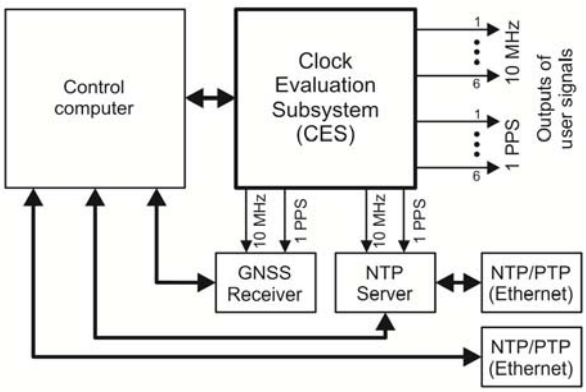

Fig.2. Simplified block diagram of EUU

Clock Evaluation Subsystem

The designed CES (fig. 3) consists of: (1) a set of three miniature atomic clocks LN CSAC (*Low Noise Chip Scale Atomic Clock*) [2]; (2) three-channel time-interval counter; (3) programmable output signals distributor; (4) local reference atomic clock and the control unit.

Three-channel time interval counter is based on timestamps measurement method, where 1 PPS pulses generated by three atomic clocks are simultaneously registered on a common time scale. Obtained resulting file

of timestamps might be taken as a source of knowledge about stability of the clocks. The knowledge is typically applied to: (1) select the clock, which is synchronized to the legal time scale in the best way, as a source of local time scale, (2) calculate correcting values for precise frequency adjustment of clocks involved.

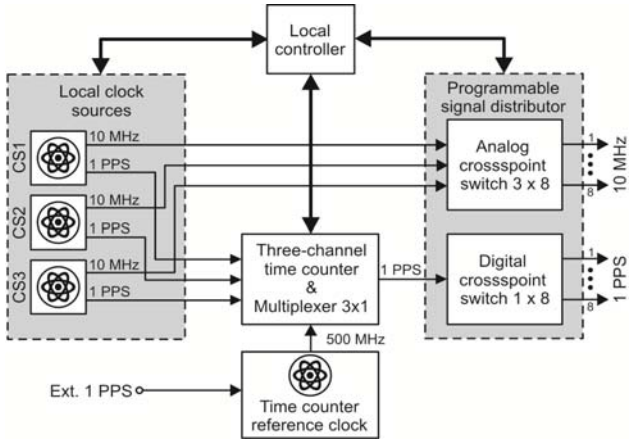

Fig.3. Block diagram of CES

The measurements are performed with the use of 500 MHz reference clock signal generated by the fourth miniature atomic clock and low-noise frequency synthesizer. It might be optionally synchronized by an external 1 PPS signal.

The control unit provides communication between all components of the CES and the control computer of EUU. There are sixteen reference signals available to the user at the CES outputs, i.e. eight 10 MHz sinusoidal waveforms and eight 1 PPS signals in TTL standard. They are provided by the selected clock and coordinated to the legal time scale.

All parts of the CES are placed on a single printed board and enclosed in the standard Rack 2U case (Fig. 4)

Fig.4. External view of CES

Local clock sources and signal distributors

The quality of local clock sources is verified through the continuous measurement of their time drifts in relation to the reference clock. The data transferred to NMI are used to compute timing systematic parameters and long-term stochastic characterization for each of the clock. This allows tuning local clocks to minimize time and frequency offsets and drifts with regard to the NMI reference clock.

In order to realize these functions by the system, it is necessary to use the local clock sources with ability to adjust their output frequency. In the EEU, which should be characterized by the best metrological parameters, three Quantum LN CSACs (*Microsemi*) [2] were applied as local clock sources.

The LN CSAC combines the accuracy of an atomic clock with a compact size and low power (below 275 mW). It provides 1 PPS pulses and 10 MHz sine wave signal with short-term stability ADEV < 2E-11 @ 1 sec. The LN CSAC contains a standard RS-232 serial interface typically used to control and calibrate the unit. It also allows for adjusting the output frequency within the range of 10 MHz ± 0.2 Hz. Communication with each of the local clock sources is done via the RS-232 interface.

The 1 PPS pulses from each local clock source are connected to inputs of the FPGA chip containing three-channel time interval counter and programmable selector of 1 PPS signal. The 10 MHz signals from local clock sources are connected to the analog cross point switch. Since the output signals of the CES are 1 PPS pulses and 10 MHz sine wave, then the programmable multichannel signal distributor includes two independent outputs: analog and digital, controlled by the local controller.

The choice of a valid 1PPS signal from local clock sources is done with the aid of 3x1 multiplexer built-in the FPGA device. The FPGA output signal is then connected to digital part of the signal distributor, designed with 1x8 fanout buffer and 8 independent 3-state TTL standard buffers. The 10 MHz sine wave signals from local clock sources are connected directly to analog part of the signal distributor. All input signals are initially conditioned by a tunable amplifiers in order to obtain the amplitude of signals equaled to 1 V (rms) at the load of 50 Ω, at all outputs of the distributor. The output buffers are made with the aid of low-noise operational amplifiers.

Time Interval Counter

The time counter contains three independent measurement channels and operates on combination of a timestamps method and double stage interpolation [3]. The principle of operation is shown in figure 5.

The period counter operates continuously counting each rising edge of the reference clock period (T_0). When 1 PPS pulse appears at input of the time counter, the content of the period counter (N) is latched. Multiplying N by the value of period of the reference clock ($N \cdot T_0$), the coarse part of a timestamp (TS) is created. Simultaneously, the first interpolation stage identifies in which segment of the four-phase clock the input pulse appears (T_{fine1}), while the second interpolation stage precisely quantizes the time interval between rising edge of registered pulse and the nearest edge of the four-phase clock (T_{fine2}). Continues operation of the period counter ensures common time scale generation while the double-stage interpolation provides picoseconds resolution and precision [4].

The designed time interval counter was implemented in a Spartan-6 FPGA device manufactured by *Xilinx*. The simplified block diagram is shown in figure 6.

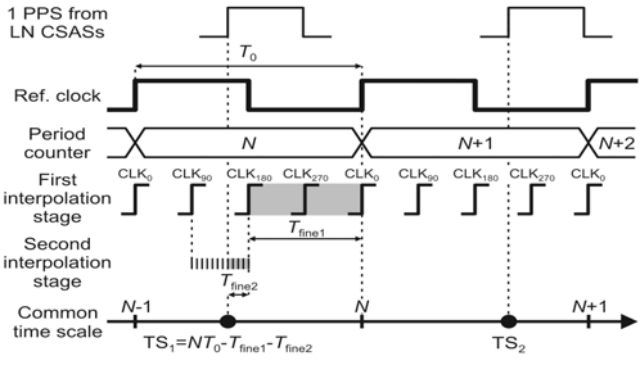

Fig.5. Time interval counter operation principle

As only 1 PPS pulses are registered in each channel, the period counter has to provide common time scale within a measurement range up to 1 s. Thus, assuming reference clock of 500 MHz frequency, 29-bit binary counter is needed (range $2^{29} \cdot 2$ ns ≈ 1.07 s). If the binary counter range is exceeded then it starts counting from the beginning and the overflow flag is generated.

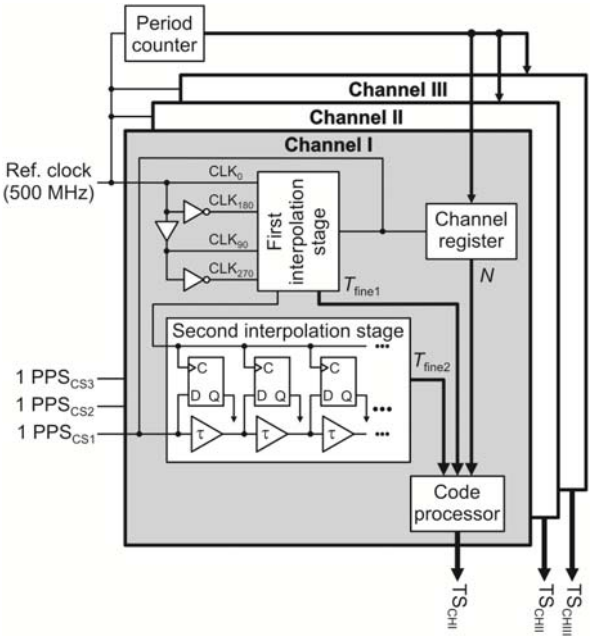

Fig.6. Block diagram of three-channel time interval counter

When 1 PPS pulse from any atomic clock generator occurs at the counter input the content of the period counter is latched in a channel register. The same pulse is used to identify clock segment in the first interpolation stage (T_{fine1}). The four-phase clock is generated by delay buffer and inverters manually placed and routed in FPGA chip [5].

In the second interpolation stage the measured pulse propagates through a tapped delay line and reaches subsequent outputs after delays of τ (propagation time of a single delay element). Each tap is connected to flip-flop data port. Besides clock segment identification, the first interpolation stage also produces latching signal that causes registration of the states of flip-flops data ports. The number of flip-flops (n) that latched high logic state ('1') is proportional to the measured time interval ($T_{fine2}=n\cdot\tau$,). The delay line in the second interpolation stage is based on carry chain multiplexers that give minimum propagation time between subsequent elements among all FPGA logic resources [5].

Measurement results from the channel register, the first and the second interpolation stages are collected and evaluated in a code processor unit to get final timestamp value [6].

Measurement tests

To perform comprehensive measurement tests of designed system, the CES was placed in a thermal chamber PL-2J (*ESPEC*) and connected to PC computer via USB interface (fig. 7). For most tests the ambient temperature was set at 22°C. The control application configures the CES to initialize measurement and collects registered timestamps. Additionally, to get precision of the three-channel time counter itself, for a single test the time interval generator Model 745 (*Berkeley Nucleonics Corporation*) was used. The measurement test pulses from LN CSACs was followed by a few hours of warming-up of atomic clocks.

The time counter resolution and its nonlinearities can be evaluated by performing a statistical code density test [7]. For this purpose a built-in calibrator generates asynchronous pulses with regard to the time counter reference clock (500 MHz) that are registered by the counter during CES initialization process. Then, obtained data is recalculated to get a transfer characteristic for each measurement channel. According to the transfer characteristics the time counter resolution is 18.7 ps, 20.4 ps and 17.9 ps for channels I-III, respectively.

The time coding delay line implemented in FPGA device is characterized by irregular quantization step sizes. The example plots for differential and integral nonlinearities (DNL and INL, respectively) for channel I are shown in figure 8. Relatively large number of wide quantization steps (DNL>>0) decreases the counter precision.

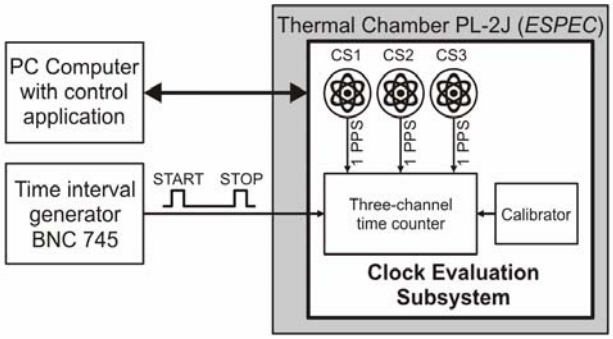

Fig.7. Test setup

The LN CSACs provide only 1 PPS and 10 MHz signals. Thus to identify counter precision we applied to the CES a pair of pulses with variable time relation. The value of measured time interval between START and STOP pulses varied from 1 µs to 1 s. For each measurement 100 timestamps for both START (TS_{START}) and STOP (TS_{STOP}) pulses were collected. Finally, the counter precision (σ) was calculated as a standard deviation of 100 results of TS_{STOP}-TS_{START}. The test was repeated for all channels.

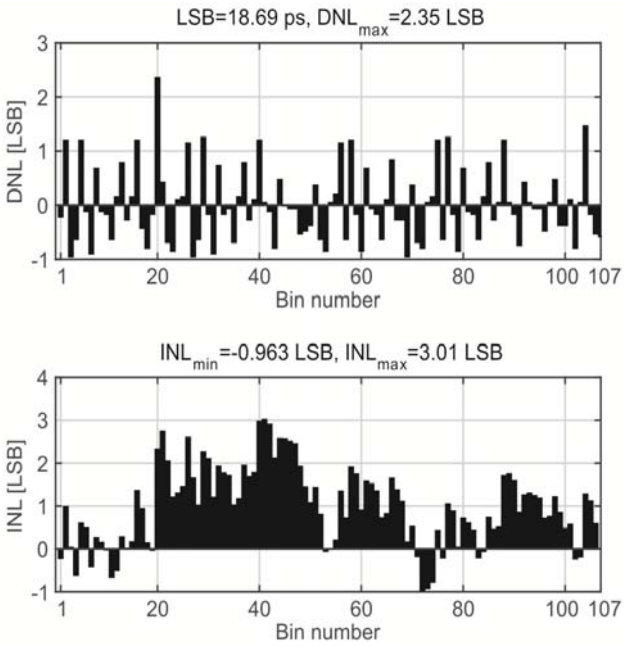

Fig.8. Time interval counter DNL and INL characteristics

Obtained precision of the time counter does not exceed 16 ps within the range up to 10 ms (fig. 9). For longer time intervals precision is limited by the time interval generator reference clock stability. The 1 PPS pulses from LN CSACs are registered with precision of about 115 ps. It is limited mainly by an extra jitter caused by a buffer that has to be implement between each LN CSAC and the time counter to provide appropriate current efficiency.

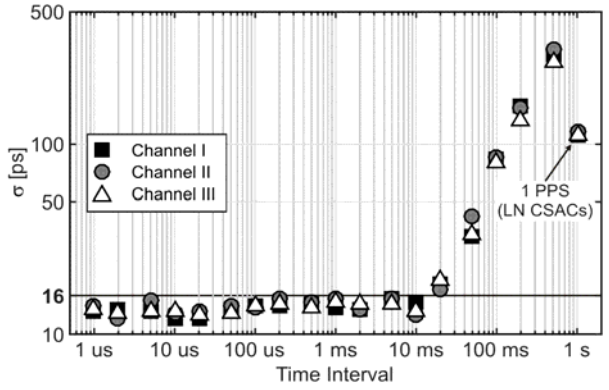

Fig.9. Time interval counter precision

In the next test we collected timestamps associated with 1 PPS pulses from three LN CSACs (CS1 – CS3) in a 1 h-long measurement. The time interval was calculated as a difference between two neighboring timestamps from the same measurement channel. Results are presented in figure 10.

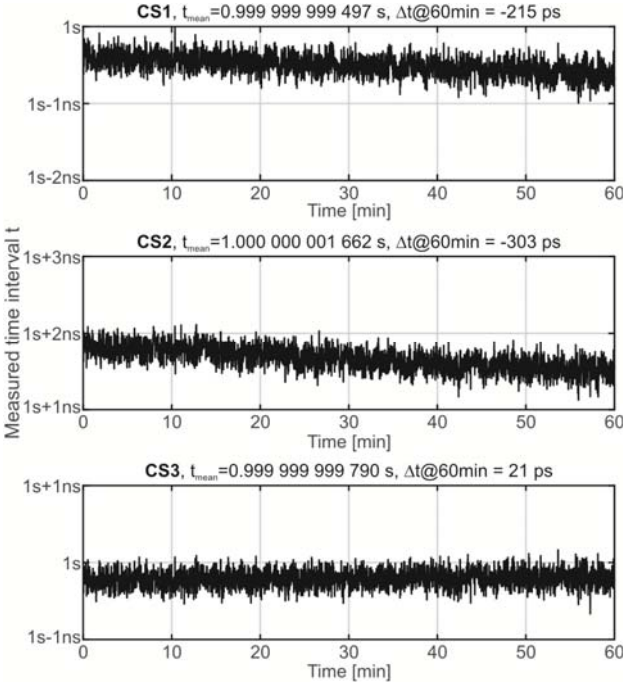

Fig.10. 1 h-long measurements of 1 PPS pulses

Each LN CSAC has a bit different nominal frequency that can additionally change over time, which is especially visible for CS2. Based on this data, the LN CSACs can be adjusted to synchronize their phases and frequency with the legal time scale.

The LN CSACs operate in limited temperature range (from -10°C to +35°C) and the CES is designed for the use in a laboratory conditions, i.e. stable ambient temperature, no vibrations, etc. Thus, we perform temperature test within a narrow temperature range (from +10°C to +30°C, with 2°C step). In each temperature the CES was warmed-up by 0.5 h. Then we performed the calibration process and measurements of 1 PPS pulses. As in the previous test, the time interval was calculated as a difference between two neighboring timestamps from the same measurement channel. Figure 11 presents the CES precision calculated as a standard deviation of 100 measurements for each point. Obtained values varied from about 100 ps to 125 ps. However, there is no evident trend and visible differences come from random nature of the measurement process.

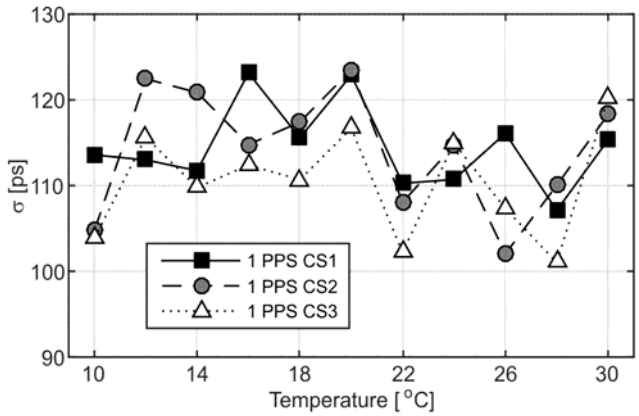

Fig.11. Temperature test

Conclusion

This paper presents the design, operation and test results of a measurement system, which is a part of pioneer Legal Time Distribution System, and allows for dynamic selection of reference atomic clock source that creates local time scale coordinated with a national time scale. This system is based on a time interval counter that permanently evaluates the spread of 1 PPS pulses from three atomic clocks with precision of about 115 ps.

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