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Analysis of circuits for effective stimulation in neurobiological experiments

Abstract. *This paper reports on the development of the amplifier for neurobiological experiments, for fast transition between the stimulation and recording phases. Schematic-level design and parameters are presented, as well as the implementation of three methods of stimulus artifact reduction. Finally, simulation results are shown for performance comparison of these methods.*

Streszczenie. *Artykuł opisuje projekt wzmacniacza do zastosowań w eksperymentach neurobiologicznych, gdzie szybkie przełączanie pomiędzy fazą stymulacji i fazą odczytu jest bardzo istotne. Zaprezentowany jest schemat układu, jego parametry, implementacja trzech metod redukcji artefaktów stymulacyjnych, oraz wyniki symulacji porównujących te metody. (**Analiza układów elektronicznych do efektywnej stymulacji w eksperymentach neurobiologicznych**).*

Keywords: stimulation, artifacts, neurobiological experiments.
Słowa kluczowe: stymulacja, artefakty, eksperymenty neurobiologiczne.

Introduction

Dedicated integrated circuits for stimulation and recording in neurobiological experiments are important tools that allow for better understanding of the nervous system operation. Additionally, these circuits enable the development of methods for the treatment of neural diseases (such as epilepsy, depression, blindness and Parkinson disease) and the construction of brain-computer interfaces that facilitate the daily functioning of disabled people [1, 2].

Electrical properties of the electrodes used in microelectrode arrays, together with the parameters of stimulus pulses (necessary to initiate the action potential), cause the presence of residual voltage on the electrode. As a result, this leads to the risk of saturation of recording amplifier and the lack of possibility of cell response recording throughout periods on the order of few milliseconds after the end of stimulus pulse (so called "stimulation artifacts"). The minimization of duration of the artifacts ("dead time") is currently an important and still developing research topic. Among various hardware-based artifact reduction methods described in the literature, there are some implemented in integrated circuits, with more or less satisfactory results.

Blum, Brown *et al.* [3, 4] proposed the circuit shown in Fig. 1. It uses two strategies of artifact reduction. First of them is discharging the electrode to the voltage equal to electrochemical potential of the electrode in feedback loop (after the end of stimulus pulse). Second of them is a modification of the bandwidth of the recording amplifier for few ms after the end of stimulus pulse. Several versions of integrated circuits that use these strategies were designed and measurement results show that the recording of neuron responses on the stimulating channel is possible 2-3 ms after the stimulus pulse, and after 500 µs on the neighbouring channels.

Hottowy *et al.* [5, 6] proposed a slightly different electrode discharging technique (see Fig. 2). During the recording phase, the voltage of the electrode is sampled and stored in 10 pF capacitor. Next, before the start of stimulation, the recording amplifier and the capacitor are disconnected from the electrode. After the stimulus pulse, the electrode voltage is recovered by the use of the capacitor that stores the potential that was present on the electrode before the stimulation was started. Moreover, triphasic current stimulus pulse is used instead of the most common biphasic one, which allows for the residual voltage reduction and – as a result – the reduction of the artifact. The reported artifact recovery times are 55 µs for the stimulating electrode and 5 µs for the neighbouring electrodes [6].

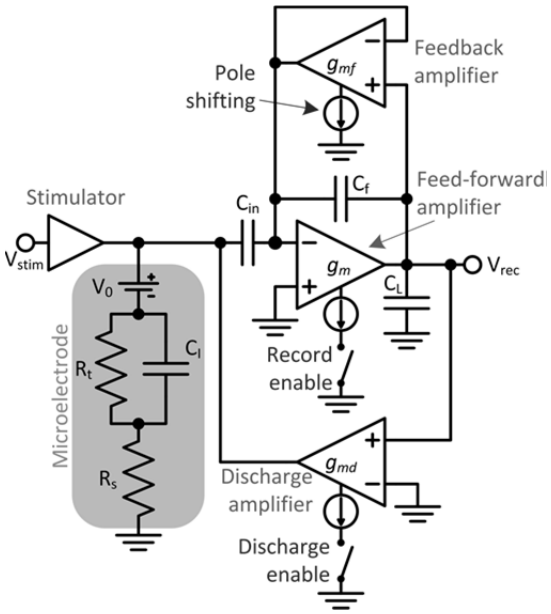

Fig.1. Schematic of fast artifact recovery circuit proposed by Blum, Brown *et al.*: electrode discharging in feedback loop and pole shifting methods are implemented

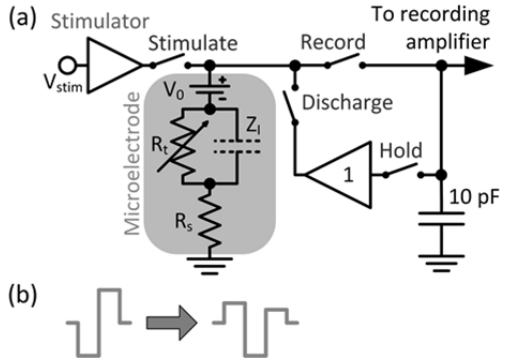

Fig.2. Schematic of fast artifact recovery circuit proposed by Hottowy *et al.*: (a) electrode discharging using sample-and-hold technique, (b) utilization of triphasic stimulus pulse instead of the biphasic one

In this paper, we analyse the circuit combined of three artifact reduction methods. Also its current implementation in submicron CMOS technology is presented. Simulation results are shown that compare the performance of these methods. Finally, the conclusions are drawn.

Design of the circuit

The purpose of our research is to design a circuit that combines the most effective methods allowing for fast transition between the phases of stimulation and recording. One of the configurations that are considered is shown in Fig. 3. It includes the following solutions: 1) sampling the voltage of the electrode before the start of stimulation and discharging the electrode to the value of this voltage after the end of stimulus pulse, 2) increasing the lower passband frequency of the recording amplifier for a short time after the end of discharging, and 3) selection of stimulus pulse parameters that will ensure the minimisation of the artifact (currently, multiphasic pulse is considered). Moreover, the possibility of independent control of stimulus pulse parameters (current amplitude and the polarity) is planned to be provided in order to make the generation of various stimulation patterns possible.

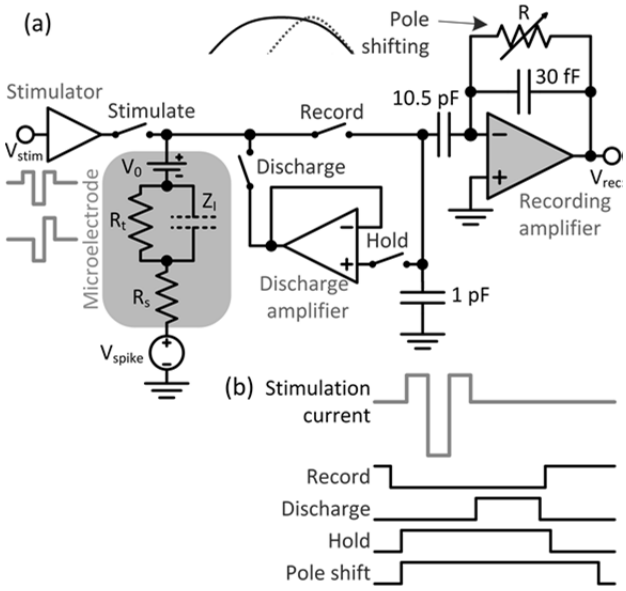

Fig.3. Proposed circuit for artifact minimization: (a) schematic of the circuit, (b) control signals. V_{spike} represents the neuron activity

The development of the project is a continuation of previous works [7, 8]. In its current state, two amplifiers that form the core of the circuit are designed, with the use of submicron CMOS 180 nm technology. This is the basic setup that allows for qualitative comparison of the performance of implemented artifact reduction methods. Stimulator is modelled by an ideal current source, while switches are modelled by two-state elements with open switch resistance equal to 1 kΩ, and closed switch resistance equal to 100 GΩ. The microelectrode is represented by three-element model (Z_{I} is the interfacial impedance, R_{t} is the charge transfer resistance, R_{s} is the spreading resistance) with V_0 equal to the electrochemical potential. The resistance R provides DC feedback for the recording amplifier and is used for the control of its bandwidth. For standard recording channels' operation mode (i.e. lower cut-off frequency set to 300 Hz) its value is equal to 16.9 GΩ. When the pole shift is enabled, resistance R is changed to 2 GΩ, resulting in the lower cut-off frequency shift to 2.1 kHz. Results of amplifiers' parameters are summarized in Table 1.

Schematics of the recording amplifier and the discharge amplifier are shown in Fig. 4. They are based on the classical two-stage CMOS operational amplifier topology. The recording amplifier was designed with regard to power and noise minimization requirements of electronic circuits for the neurobiological experiments. The design of discharge amplifier was a compromise between power, area, stability and speed. It includes additional transistor (M_{10}) that allows overcoming the output current limitation for the rising slope of the output voltage (equal to 50 nA – the bias current of source follower stage, limited by M_9 transistor).

The design of both amplifiers includes the offset correction circuit. Its principle of operation is based on adding or subtracting small current to or from one of the nodes of differential pair. Offset correction is important for the discharge amplifier, since it is responsible for the measurement of small voltage offsets (for example, for the parameters of microelectrode and stimulus pulse used in the following section, the values of electrode's overpotential – a voltage on interfacial capacitance that needed to be discharged – were on the order of tens of millivolts).

Table 1. Amplifiers' parameters

	Recording amplifier	Discharge amplifier
Power consumption [μW]	5.9	3.0
Bandwidth [kHz]	0.3-8.6 2.1-10.4 (pole shift)	0-300
GBW [MHz]	1.43	0.22
Open loop gain [dB]	89.1	88.5
Closed loop gain [V/V]	346	1
Phase margin	89°	69°

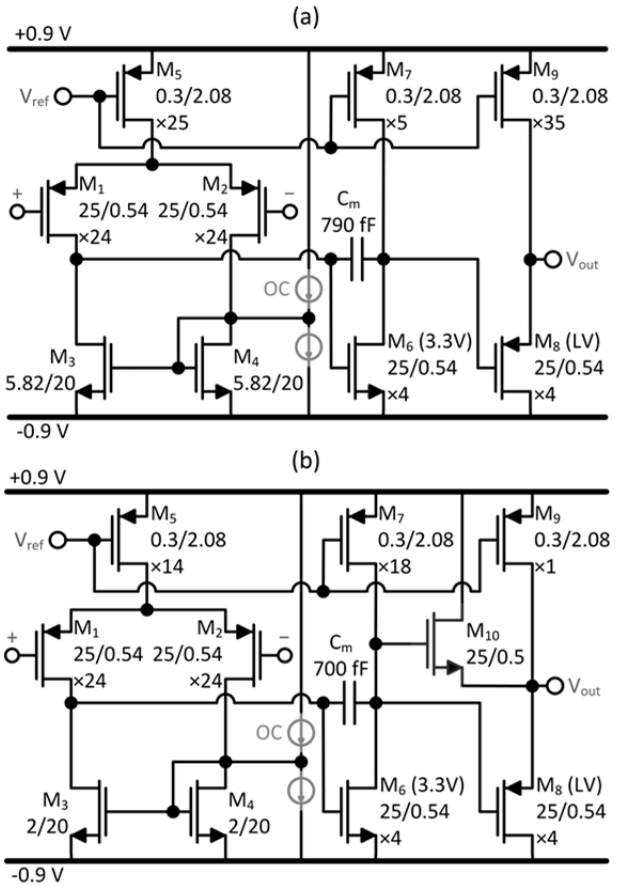

Fig.4. Schematics of: (a) recording amplifier, (b) discharge amplifier. All dimensions are given in μm. OC represents the offset correction circuit

Simulation results

The purpose of simulations presented in this section was to compare the performance of three stimulation artifact reduction methods that were implemented in the circuit discussed above. Therefore, a typical signal of neuron response was used with amplitude equal to 200 μV. The assumed value of electrode's electrochemical potential V_0 was 50 mV. Interfacial impedance Z_I was represented by the pseudocapacitive constant-phase element (CPE) approximated by the RC ladder to provide characteristics close to $36\times10^7 \cdot (j\omega)^{-0.86}$ [5, 9-11]. The remaining parameters were assumed to be: R_t = 1.5 MΩ and R_s = 80 kΩ.

The basic setup of stimulation pattern was standard biphasic, charge-balanced, cathodic-first pulse with no interphase delay, with the length of each phase equal to 100 μs and the amplitude equal to 1 μA. When the utilization of triphasic stimulus pulse as a method for stimulus artifact reduction was tested, the length of each phase was also equal to 100 μs, and the current amplitudes for consecutive phases were equal to 0.6:-1:0.4 μA.

Fig. 5 presents the comparison of stimulation artifact reduction performance for the methods implemented in the circuit. The signals on the output of the recording amplifier are shown for various cell response delays (start of the response in the range of 10 μs – 1.6 ms after the end of stimulus pulse, i.e. the peak of the response occurred in the range of about 200 μs – 1.8 ms after the stimulation, respectively). In all cases, the stimulus pulse ended at time t = 0.

First, the results are shown where no artifact reduction technique was applied (see Fig. 5a). Acceptable quality of recording is achieved for responses starting later than 1.5 ms after the stimulation, when the derivative of non-response component of the signal starts to be negative.

When charge-balanced, triphasic stimulus pulse is used, the circuit recovers from artifacts much faster. As it is shown in Fig. 5b, the peak of non-response component of the signal occurs for t ≈ 240μs and spikes that start about this time are noticeable. The best recording quality is achieved after about 1 ms.

When electrode discharging method was tested in the simulations, the discharge phase lasted from the end of stimulus pulse to the start of cell's response. Previous simulations (when the interfacial impedance was represented by a simple capacitive Stern model instead of the CPE) suggested that discharging the electrode from the moment when stimulus pulse ends to the expected moment of neuron response is the best approach. Current results for CPE, however, show that longer discharge period does not necessarily mean better recording quality. Actually, in Fig. 5c it is hard to distinguish spike-related component from artifact-related component of the recorded signal. This topic is discussed later in the paper.

For pole shifting method (Fig. 5d), the peak of non-response component of the recorded signal occurs for t ≈ 330μs. Acceptable recording quality is achieved for spikes starting after about 500 μs and the best results are obtained about 1 ms after the stimulation.

Fig. 6 presents simulation results that illustrate the proportions of recorded neural responses for the discussed methods of artifact reduction (with two slightly different microelectrode model parameters: R_t = 1.65 MΩ and R_s = 63.8 kΩ [12]). In this case, all responses started at the same time, 600 μs after the end of stimulus pulse. In contrast to the previous results, for which the discharge period was approximately equal to the spike delay, now the duration of discharging was set independently of this delay. As it can be seen in the figure, the smallest artifact-related

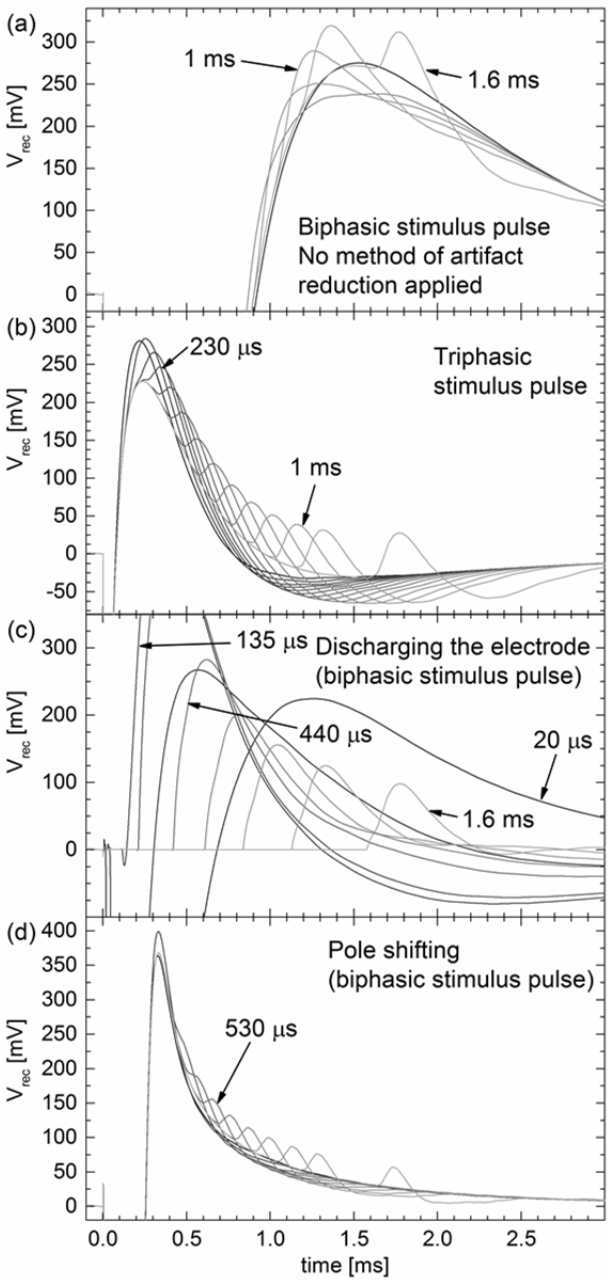

Fig.5. Simulation results: the responses of neuron cell (for various delays between the end of stimulation and the start of response) recorded by the amplifier when no artifact reduction is applied in comparison with the recordings for three methods of artifact reduction used separately: (a) results for biphasic pulse stimulation when no method of artifact reduction is used, (b) utilization of triphasic pulse, (c) electrode discharging (the time of discharging was approximately equal to the value of cell response delay), (d) pole shifting method

component is present for triphasic stimulus pulse. This method provides the best recording quality. The performance of pole shifting is comparable; however, the bandwidth modification causes a significant reduction in the amplitude of the recorded response.

Results for various durations of electrode discharging show interesting behaviour. At the beginning, when the discharge period is rising from zero to some "critical" value (125 μs in this particular case), the positive part of artifact-related component of the recorded signal is also increasing. Furthermore, its extremum appears faster. The second effect is desirable, the first is not. As a result, there is an

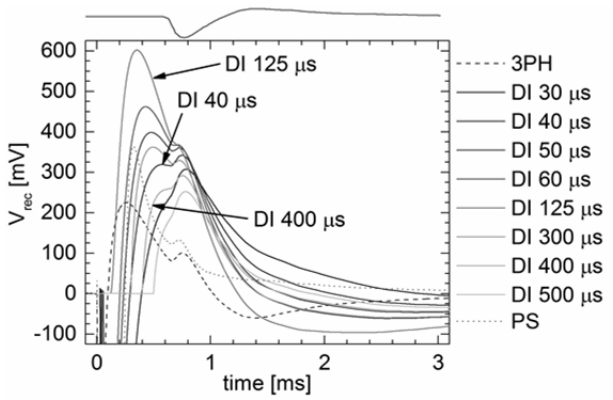

Fig.6. Simulation results: the comparison of responses of neuron cell recorded by the amplifier for three methods of artifact reduction (3PH – triphasic stimulus pulse, DI – discharging the electrode for a given period, PS – pole shifting). In all cases the cell response started 600 µs after the end of stimulation (its peak value occurred about 200 µs later). The shape of response signal is shown above the top axis

intermediate value of discharge duration that provides the best possibility of extracting the useful cell response signal from the artifact. In the presented case, 40 µs may be designated as such a value. Further increasing the discharge duration causes the positive part of artifact-related component to start to decrease. Yet again, there is some value between the defined critical value (125 µs) and the delay of neural response (600 µs) that provides the best recording results (approx. 400 µs in this case). Further analysis of the results shows that the recording quality for discharge periods equal to 40 µs and 400 µs is similar. Therefore, there is no reason to choose the second value, since its additional consequence is that the recording amplifier remains blind for the period ten times longer than in the case of first value.

The described behaviour does not appear for purely capacitive model of interfacial impedance. Such a model would be therefore too simple for stimulus artifact modelling. Incorporation of CPE into the model is a necessity.

Discussion of the results

The results presented in the previous section show superiority of the triphasic pulse method of artifact reduction over electrode discharging and pole shifting. However, since the responses of neuron cells may occur even faster than 200 µs after the stimulation [5], the performance in all presented cases is too slow.

In previous simulations capacitive Stern model of interfacial impedance was used. Such an approach leads to *wrong conclusions*, namely: 1) stimulation artifacts may be cancelled almost completely by the utilization of 0.5:-1:0.5 µA triphasic stimulus pulse, 2) it is good to discharge the electrode as long as possible before the expected moment of cell response. *In more realistic model*, incorporation of CPE shows that electrode discharging may be effective only for a limited range of discharge durations. The observed behaviour of simulated recorded signals may be better understood when the analysis of electrode's overpotential waveform is taken into account. It is, however, beyond the scope of this paper.

Having the above in mind, we propose to combine the described methods to develop a solution that will not be affected by the electrode's parameters variations and will have low power consumption and good performance, regarding time transition between stimulation and recording. Before this goal is accomplished, the relationship between an optimal configuration of the presented fast artifact recovery methods and the electrode parameters needs to be established.

Summary

The analysis of the circuit for stimulus artifact reduction using multiple techniques was presented. Simulation results were described, which compare the performance of these techniques. Further research will be concentrated on the optimization of stimulation protocol and stimulus pulse parameters for more precise electrode model and the design of the remaining circuit components in CMOS technology.

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