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An universal test station for multichannel integrated neural amplifiers based on LabVIEW environment

Abstract. *Modern technology allows for design of sophisticated measurement systems utilizing hundreds of independent recording channels. That imposes necessity of complex system functionality validation procedures development. The article describes an universal test system dedicated for tests of multichannel integrated circuits implemented in submicron technologies. Preliminary measurement results of a multichannel integrated circuit dedicated for advanced neurobiological experiments are also presented in the article.*

Streszczenie. *Współczesne technologie umożliwiają budowę systemów składających się z setek niezależnych torów pomiarowych o rozbudowanej funkcjonalności. Nakłada to konieczność przeprowadzenia szeregu testów weryfikujących ich działanie. Artykuł prezentuje projekt uniwersalnego systemu testującego opracowanego na potrzeby projektowanych, w technologiach submikronowych, wielokanałowych układów scalonych. W artykule przedstawiono również wyniki wstępnych pomiarów układu przeznaczonego do złożonych eksperymentów neurobiologicznych. (**Projekt uniwersalnego stanowiska do testów wielokanałowych scalonych wzmacniaczy sygnałów neurobiologicznych opartego o środowisko LabVIEW**).*

Keywords: multichannel integrated circuits, test procedures, multifunction measurement card, LabVIEW.
Słowa kluczowe: wielokanałowe układy scalone, testowanie, wielofunkcyjna karta pomiarowa, LabVIEW.

Introduction

Current technology progress allows to develop integrated systems for various types of applications that can be used in physics, biomedicine or industry. These systems can be built of microsensors that are combined with integrated electronics occupying small area and having complex functionality (i.e. ability to adjust their main parameters in a wide range). Furthermore, these devices may consist of hundreds of active sites that can be controlled individually. As a result to develop a final system one needs to perform wide range of tests covering a device modes of operation validation. Example of such systems are multichannel integrated circuits (IC) dedicated to sophisticated neurobiological experiments. These are mainly neural amplifiers and stimulators built of hundreds of active sites that allow user to record for instance Action Potentials (AP), Local Field Potentials (LFP) or even to stimulate electrically neural system cells [1-6].

Due to demanding neurobiological experiments, integrated circuits must fulfill strict requirements concerning parameters' tuning range, modes of operation and their uniformity from one active site to another. Therefore, the ICs must undergo complex test procedures before their final experiment adaptation.

The article presents an architecture of a measurement system and universal test procedures that can be applied in order to perform wide range of tests for variety of ICs. The measurement system is implemented in LabVIEW environment and employs National Instruments (NI) multipurpose measurement card. The measurement results of a 100-channel IC fabricated in CMOS 180nm process are presented.

Section II of the article contains description of a multichannel IC dedicated to neurobiology experiments, Section III presents the test station architecture, main concerns regarding universal test procedures, and software implementation in LabVIEW environment. The measurement results are presented in Section IV while Section V consists of a conclusion.

Architecture of the IC

Neural amplifiers are capable of registration of different types of signals like AP or LFP. A frequency band of the LFP signals is from below 1 Hz to 500 Hz while AP signals from about 300 Hz to 7 kHz. LFP amplitudes span from below 10 μV to 5 mV and AP from about 10 μV to 500 μV. This implies a need for a flexible registration channels bandwidth which should be adjusted individually for each channel. Furthermore due to many experiments' requirements the main system parameters should have high uniformity from one active site to another. Therefore it is prerequisite for the system to allow for its main parameters correction whenever its uniformity is deteriorated by a fabrication process, variability of measurement environment, etc..

One of commonly used approaches for system uniformity improvement are digital blocks supporting analog parts of a chip. Digital registers are used to perform crucial IC parameters correction during a device calibration procedure (i.e. cut-off frequencies, voltage gains, voltage offsets, stimulating currents, etc.) and to change its operating mode (registration, stimulation, test phase).

Digital blocks are the most variable parts between ICs versions (due to different ICs requirements) and are crucial during design of universal test procedures. The Fig. 1 presents a view of exemplary multichannel IC that is dedicated to neurobiological signals recording and current stimulation of neural cells. Its main blocks are: recording and stimulation channels, analogue multiplexer and digital blocks for both IC communication and its main parameters setting.

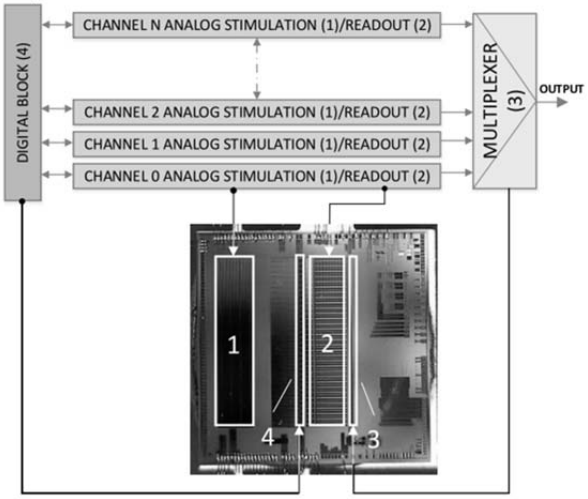

Fig.1. Architecture of the exemplary IC dedicated to neurobiological experiments

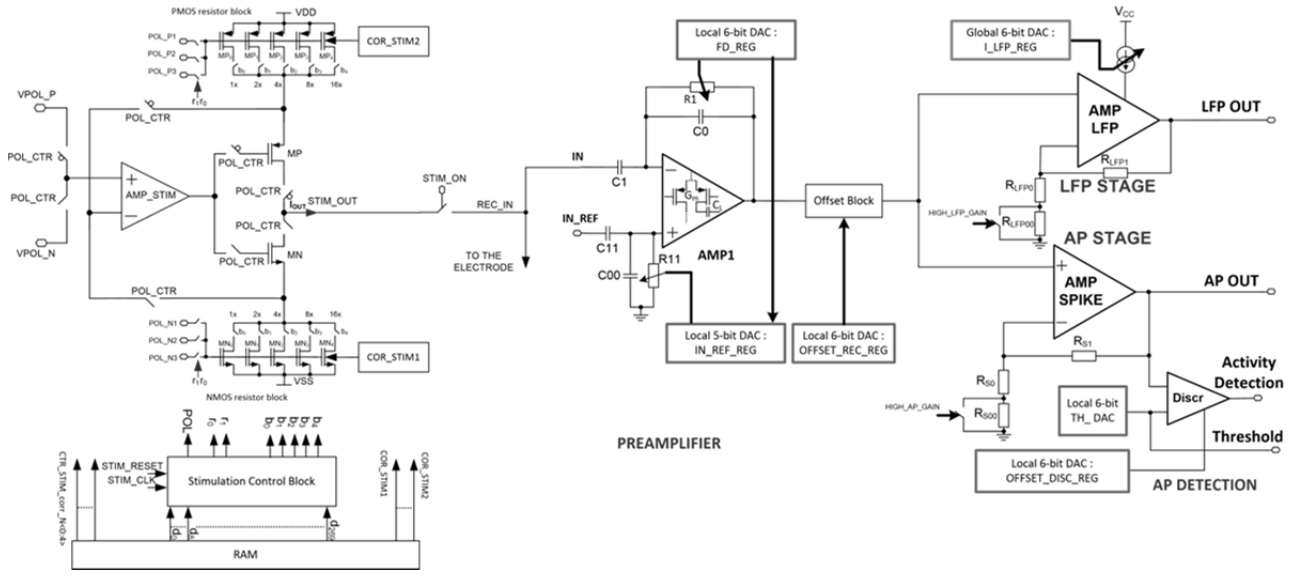

Fig.2. Schematic idea of the proposed IC's channel

One of the ICs that was tested by the Authors consisted of hundred of recording/stimulation channels each supported by the digital registers configured by peripheral devices. A schematic idea of the single channel is presented in the Fig. 2. The recording part of the IC is built of four stages: preamplifier, amplifiers for AP and LFP signal conditioning and discriminator for detection of the AP signals. A user is able to change the recordings' channel lower cut-off frequency with the use of FD_REG D/A converter controlled by the digital register. To improve preamplifier's input symmetry an additional IN_REF_REG D/A converter is used [7]. In order to perform further signal conditioning the AP, LFP and DISCR blocks are used. The user can change: voltage gain (inputs HIGH_LFP_GAIN, HIGH_AP_GAIN), upper corner frequency of the LFP stage (I_LFP_REG C/A converter), voltage offset of the recording channel (OFFSET_REC_REG C/A converter), threshold and voltage offset of the discriminator (TH_DAC, OFFSET_DISC_REG).

The stimulation channel, controlled by the digital circuitry, is responsible for generation of bipolar current pulses. The user is able to change a stimulation current range (inputs POL_P1 - POL_P3, POL_N1 - POL_N3), its value (bits b_0-b_4), and its polarity (input POL_CTR). A spread of current values from channel to channel may be minimized by performing correction procedures using the correction DACs (COR_STIM1, COR_STIM2). Additionally RAM memory availability in each of the stimulating channels allows to generate different current patterns (see Stimulation Control Block in the Fig. 2).

Design of the test system

Main requirements for the designed test station were its flexibility and mobility. Authors chose LabVIEW environment and National Instruments multipurpose measurement card as the main tools for satisfying these requirements. The main advantage of LabVIEW is that it uses build-in function palettes that can be extended with ones implemented by a software engineer what significantly simplifies a process of complex software development. Additionally, polymorphic VIs are worth mentioning as these can perform the same action (i.e. write chip, convert registers data) for various IC models basing on a VI input data. Therefore, abovementioned features were used to implement IC communication palettes for each model of the ICs.

The test station consists of a PC equipped with LabVIEW, USB-6351 measurement card, a power supply and an IC's isolation cubicle. The USB-6351 card's analog/digital I/O configuration allowed us to employ it for communication with digital registers of an IC, test signals generation and an IC output signal registration. The card is light (1.42 kg) and small (26.4 × 17.3 × 3.6 cm) what makes it portable and easy to install on the test station. Moreover device drivers are compatible with various models of NI measurement cards what gives possibility of hardware replacement without any modifications of the test software.

Development of testing procedures

First stage during development of a test procedure is splitting general action into smaller and comprehensive steps. These steps should be separated from programming or hardware requirements and should represent characteristic points of a test based on a source of a problem and general knowledge. The Fig. 3a shows an example of frequency response test represented as series of universal actions executed commonly regardless of a tested device.

Subsequently each step is analyzed in order to find its easiest software and hardware implementation. One of the most important points is separation of actions strictly connected with an IC model like e.g. registers data conversion, read/write signals generation. The IC specific blocks are thus independent functions that are easily replaceable and expandable. Remaining parts of the process are split into blocks in accordance with general programming rules and are fixed parts of the test software. The Fig. 3b presents block diagram of the test software module that is mostly responsible for hardware control. It reflects conversion of four general test steps from Fig. 3a into their software implementation. Diagram's parts in bold are strictly connected with an IC model and need to be modified for each new IC prototype.

Finally a hardware part of the test station is chosen. The most important factors are number of digital inputs/outputs required for PC-IC communication establishment and sample rate of a measurement card (considering frequency response tests as one of the most frequently performed). After completion of abovementioned steps all elements need to be combined into one, user friendly and maximally flexible test station.

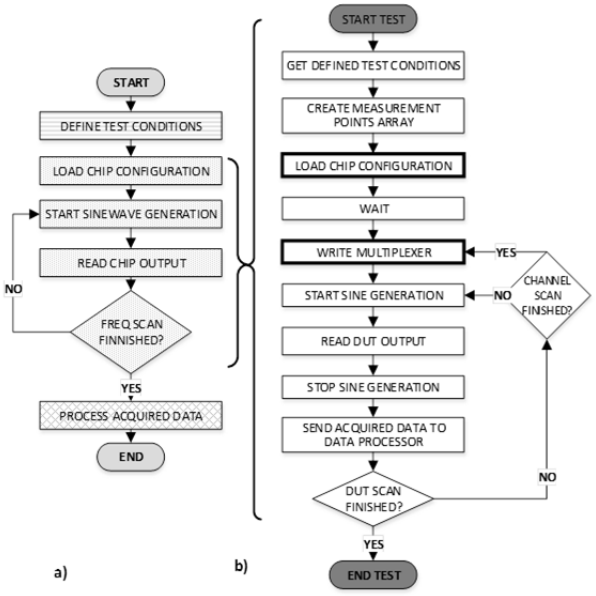

Fig.3. a) Block diagram of frequency response test steps, b) block diagram of the Main Controller module

Appropriate software architecture is a crux allowing developer to handle multiple test cases as well as several ASICs architectures. Process of architecture design is strictly connected with previously prepared test steps. Test software dedicated to advanced ICs tests should fulfill following requirements: handle PC-IC communication, generate test signals and record an IC output data, process a large amount of data and represent it on graphs or as calculated parameters (e.g. gains, cutoff frequencies).

The Authors proposed an architecture consisting of three modules: Main Controller (MC), User Interface (UI) and Data Processor (DP). The modules are based on queue driven state machine architecture (see Fig.4).

The User Interface module consists of two threads. One of them reacts to user actions while the other handles communication with the MC as well as the application front panel updates. Important part of the UI implementation is adequate controls grouping. Chip configuration controls are changeable parts of the interface depending on an IC model thus should be separated from fixed parts of the UI. This approach provide not only simplification of module development but also ease of an IC configuration data access from each part of the application.

The Main Controller connects all modules. It is also responsible for hardware control and communication with an IC. It is the most expanded module of the application and handles most of the test procedure steps. Despite that realization of this module can not be overcomplicated to maintain desirable level of the system flexibility. The Authors aimed to limit number of the sate machine cases responsible for an IC configuration procedures. As a result only two cases need to be updated for every new IC model. These are parts of code performing an IC settings conversions and digital signals generation. Other cases deal with principals of frequency response testing and hardware control. Hardware is controlled by universal drivers providing possibility of fast device replacement. Nonetheless, drivers are grouped into more general functions (VIs) to add possibility of changing hardware provider or moving to a more advanced platform like National Instruments PXI.

The Data Processor is a module dedicated to measurement data analysis. Due to a large amount of data acquired during a test procedure results are not stored in the application memory but are streamed to a TDMS file during a data acquisition process. The DP is dependent on the MC and each data analysis process is triggered by this module. It is independent from an IC model changes and remains unaltered unless additional parameters extraction is required. The DP reads data from a TDMS file, processes it, extracts required parameters, generates graphs, and saves it to a binary or a text file. The only data remaining in the application memory is a part necessary for the UI updates. All additional parameters are stored in a temporary directory but user can choose to save them in any other directory. If not saved by the user, files are removed from a disk after measurements or during application shutdown.

Communication based on queues gives possibility of new, controlled by the MC, modules insertion. Additional modules might perform automated reports generation, hardware adjustments or simultaneous tests of several devices. This approach keeps the software scalable for further development.

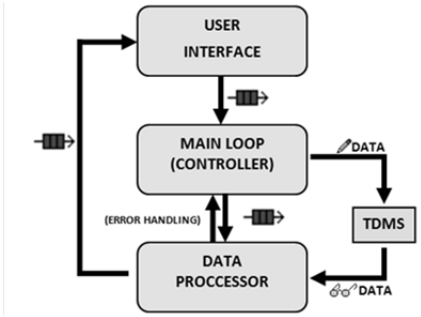

Fig.4. The test application architecture

Measurement results

In order to verify design assumptions tests of a 100-channel neural recorder and stimulator have been conducted. The Fig. 5 shows preliminary results of the frequency response test of the recording channels and results of the lower corner frequency correction.

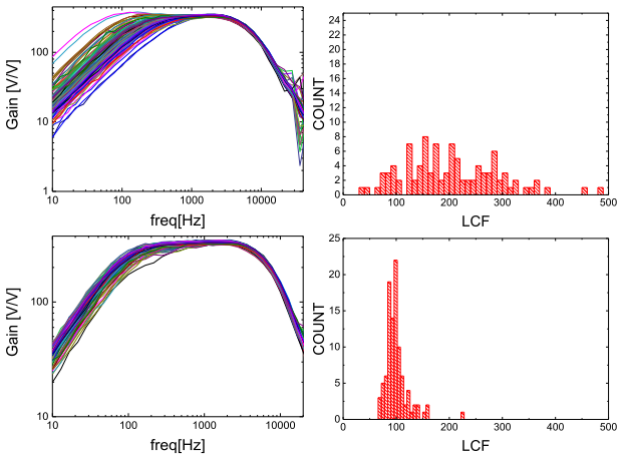

Fig.5. Frequency response and lower cutoff frequency test of an 100-channel neural amplifier: upper row – before lower cutoff frequency correction, lower row – after lower cut-off frequency correction

The proposed system architecture is flexible and easy to adapt to different tests of ICs. Therefore its simple modification allowed us to perform measurements of the input referred noise for different recording channels' settings (see Fig. 6). The same test system equipped additionally with precise ammeter (HP 34401A) was used to verify performance of current stimulators. The Fig. 7 presents measurement results of current changes for 100 channels while sweeping bits b_0-b_4 (see Fig. 2).

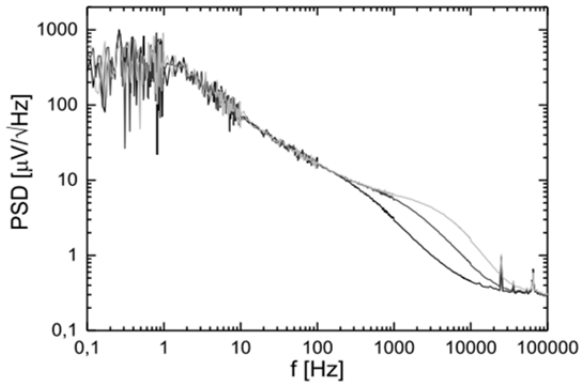

Fig.6. Power spectral density measurement results for three different upper corner frequencies

It is worth mentioning that only minor changes in the test system described are required in order to prepare it for tests of a new model of an IC. Considering two variants of ICs characterized by major differences in their architecture (see Fig. 8) only two cases of the MC (see Fig. 3) require modifications. These are parts of code responsible for an IC configuration and its multiplexer controlling. Hence update of just a few SubVIs if sufficient to adapt the system for tests of a new IC model.

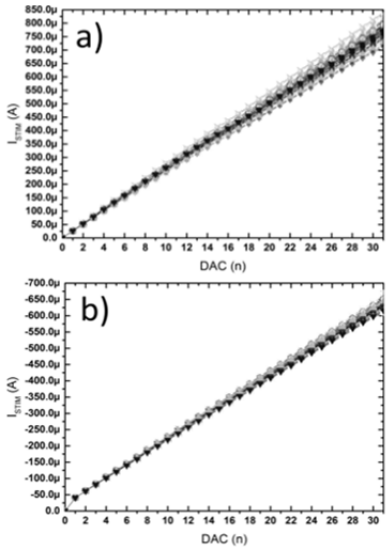

Fig.7. Stimulating currents measurement results for different current polarities: a) anodic and b) cathodic currents

Obtained measurement results allowed the authors to analyze effectiveness of correction algorithms applied to the tested circuit. As it can be seen in the Fig. 5 the lower corner frequency spread decreased significantly after the IC calibration. Performed tests verified also the IC project assumptions regarding its noise level and generated current uniformity. Noise power spectral density and its dependency on upper corner frequency setting of the second amplifying stage of the recording channel is shown in the Fig. 6. The currents measurements (see Fig. 7) are aimed to adjust anodic and cathodic current levels for the purpose of cells current stimulation. Basing on them prospective calibration algorithms may be implemented.

Each of the presented test types were performed as independent procedures. Resulting data was analyzed in order to verify tested die efficiency. After verification of the IC project assumptions the tests may be integrated and performed as an automated series of quality assurance steps.

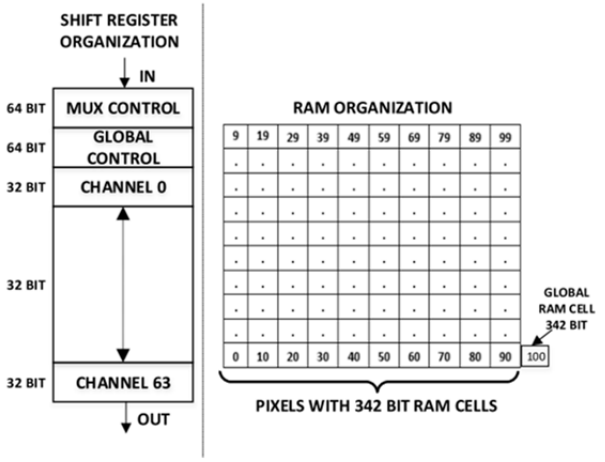

Fig.8. Variations of digital registers organization in multichannel ICs

Conclusions

The test station presented in the article meets the requirements of both mobility and flexibility. It can be easily adjusted to multiple ICs' architectures. Due to the off-the-shelf components and universal measurement devices utilization it gives possibility of extension for typical test procedures as well as for migration to a higher class measurement equipment.

The station was used during tests and correction procedures of various ICs and proved to be user friendly, flexible, highly efficient and easy to adapt for different ICs and tests.

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