ATILA SKANDARNEZHAD[1], AMANGALDI KOOCHAKI[1], YAGHOOB MOHAMMADMORADI[1], ABDOLAZIZ KALTEH[1]

Department of Electrical Engineering, Aliabad Katoul Branch, Islamic Azad University, Aliabad Katoul, Iran (1)

doi:10.15199/48.2016.03.02

Lagrangian Modelling of a Synchronous Step-Down Converter by Considering the Parasitic Elements

Abstract. *This paper introduces a new technique to model a synchronous buck converter in the closed loop compensated conditions by Lagrange equation. In the design process of converters it is desirable to assess as many critical design parameters and parasitic effects by simulation as possible, since the control is hard to tune after fabrication. The main advantage of this method is its versatility and simple implementation. In this work, switch conduction loss of an integrated, synchronous buck converter is identified to have significant influence on control loop dynamics. Thus, an equivalent small-signal model for the close loop frequency response accounting for switch conduction loss is developed. Finally, the model is validated against the frequency response obtained by periodic stability analysis which can account for parasitic effects and loading. Very good agreement between the extended model and the simulation results obtained.*

Streszczenie. *W artykule opisano modelowania z wykorzystaniem równań Lagrange synchronicznego przekształtnika typu buck. Straty przełączania są identyfikowane jako wpływające na dynamikę. Analizowano okresową stabilność z uwzględnieniem efektów pasożytniczych.* ***Modelowanie synchronicznego przekształtnika z wykorzystaniem równań Lagnrange u uwzględnieniem efektów pasożytniczych****.*

Keywords: Averaged Model, Buck Converter, Lagrange Equation, P-I Compensator.
Słowa kluczowe: równania Lahgrange, przekształtnik synchroniczny typu buck.

Introduction

During the past decades, power electronic research has focused on the development of new families of inverter topologies used in portable applications. Power stages of PWM converters are highly nonlinear systems because they contain at least one transistor and diode, which operate as switches [1-3]. The simplest way to reduce the voltage of a DC supply is to use a linear regulator such as a 7805, but linear regulators waste energy as they operate by dissipating excess power as heat. Buck converters, on the other hand, can be remarkably efficient such 95% or higher for integrated circuits, making them useful for tasks such as computer processor and other low voltage applications [4].

The converters usually require control circuits to regulate the dc output voltage against load and line variations. Typical control aspects of interest are frequency response, transient response, and stability. Linear control theory is well developed and may offer valuable tools for studying the dynamic performance of PWM converters [5]. However, in order to apply this theory, nonlinear power stages of PWM converters should be averaged and linearized, where the Lagrange equation is used here.

The EL equation was developed in 1750's by Euler and Lagrange in connection with their studies of the tautochrone problem. In Lagrange mechanics the evolution of a physical system is described by the solutions to EL equation activity of the system [6]. This method has the advantage that it takes the same form in any generalized coordination comparing with Newton's low. The electrical system is analogous to mechanical system [7]; therefore one can apply the EL equation on it in the similar way. Some analogies can be expressed within pairs such: (voltage ↔ force), (current ↔ velocity), (resistor ↔ damper), (inductor ↔ mass) and (capacitor ↔ spring). Here the objective is to build a model for the switched electrical circuits that also is applicable to circuits without switches. The non-conservative EL dynamics of an electrical circuit can be classically characterized by the following formulas.

$$(1)\qquad \frac{d}{dt}\left(\frac{\partial \ell(q,\dot{q})}{\partial \dot{q}}\right)-\frac{\partial \ell(q,\dot{q})}{\partial q}=-\frac{\partial \psi(\dot{q})}{\partial \dot{q}}+\chi(q)\lambda+F_q$$

$$(2)\qquad \ell(q,\dot{q})=\tau(q,\dot{q})-\nu(q,\dot{q}) \quad , \quad \chi(q)\dot{q}^T=0$$

In the above equations, phrase of (q') is the vector of electric current and q represents its time integral or electric charge. The scalar function ℓ is the lagrangian operator of system that is the difference between the kinetic energy (denoted by τ) and the potential energy (denoted by υ) of the system. The symbol ψ is the Raleigh dissipation function of the system and the vector F_q represents the forcing function associated with each state variable coordinate. Letter λ is the intermediate help variable and χ introduces the constrain forces matrix that is normally can be defined by Kirchhoff current law [8].

This paper introduces a way to simplification and modelling of the two stage single phase inverter structure by averaging the switch network. In spite of other works that consider the switch network ideal, this work adds the parasitic elements of the switch network into modelling process. The dependent sources are used to model the ideal switching network and the law of conservation of energy is used to model the transistor on-resistance, the diode forward resistance and the diode offset voltage. By replacing the switching network in a PWM converter by its small signal model, a small signal model of the entire power stage is obtained.

Synchronous buck converter analysis and modelling

Usual buck converter scheme is presented in Fig.1. The disadvantage of the conventional buck converter is its weak efficiency at high output currents.

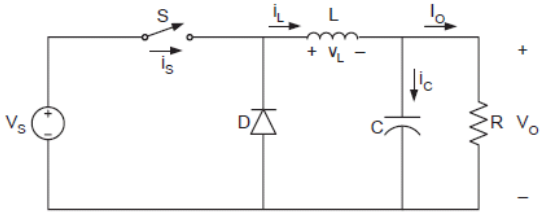

Fig.1. Usual buck converter circuit

A buck converter topology with a synchronous rectifier is shown in Fig.2. This circuit is obtained by replacing the diode with an n-channel MOSFET. In general, diodes have an offset voltage V_F and thus their forward voltage is relatively high and may become comparable with the output

voltage in low voltage applications. In contrast, MOSFET do not have an offset voltage. If the on-resistance of a MOSFET is low, the forward voltage drop across the MOSFET is very low, reducing the conduction loss and yielding high efficiency. Some low breakdown voltage MOSFET's have the on-resistance as low as 0.006Ω [9].

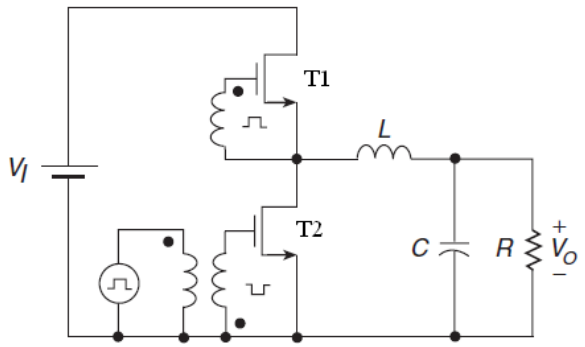

Fig.2. Synchronous buck converter circuit

In addition, operation in DCM can be avoided because the channel of the transistor can conduct current in both directions. The synchronous buck converter operates in CCM even down to no load. The two MOSFET's are driven in a complementary manner where one transformer output is non-inverting and the other is inverting. The synchronous buck converter suffers from a cross-conduction or shoot-through effect resulting in high current spikes in both transistors [10]. This produces high losses and reduces the efficiency. A non-overlapping driver can produce a dead time and reduce the cross-conduction loss. During the dead time periods, the inductor current flows through the lower MOSFET body diode. An external Schottky diode can be connected in parallel with the low side MOSFET to shunt the body diode and to prevent it from affecting the converter performance. The added Schottky diode can have a much lower current rating because it only conducts during the short dead time when both switches are off [11].

In the proceeding discussions, d symbol states the transistors position function and can be specified as formula 3. Where T and D are switching period and duty ratio respectively and t_k represents a sampling instant as below.

(3) $$d(t)=\begin{cases}1, & for\ \ t_k \le t \le t_k + D.T\\ 0, & for\ \ t_k + D.T \le t \le t_k + T\end{cases}$$
$$; t_{k+1} = t_k + T \ \ ; k = 0,1,2,....$$

First suppose that the transistor T_1 is on or d(t)=1, in this case the EL quantities are readily found to be:

(4) $$\tau_1(q,\dot{q}) = \frac{1}{2} L\ \dot{q}_L^2 \ \ ; \ \upsilon_1(q,\dot{q}) = \frac{1}{2}\frac{q_C^2}{C}$$

(5) $$\ell_1(q,\dot{q}) = \tau_1(q,\dot{q}) - \upsilon_1(q,\dot{q}) = \frac{1}{2} L\ \dot{q}_L^2 - \frac{1}{2}\frac{q_C^2}{C}$$

(6) $$\psi_1(q) = \frac{1}{2} r_T \dot{q}_L^2 + \frac{1}{2} r_L \dot{q}_L^2 + \frac{1}{2} r_C \dot{q}_C^2 + \frac{1}{2} R(\dot{q}_L - \dot{q}_C)^2$$

(7) $$F_{qL}^1 = E \ ; \ F_{qC}^1 = 0$$

r_T, r_L and r_C are the equivalent series resistors of transistor, inductor and capacitor respectively. Similarly, one can derive the EL quantities when the transistor T_2 is on or d(t)=0 where are stated below.

(8) $$\tau_0(q,\dot{q}) = \frac{1}{2} L\ \dot{q}_L^2 \ \ ; \ \upsilon_0(q,\dot{q}) = \frac{1}{2}\frac{q_C^2}{C}$$

(9) $$\ell_0(q,\dot{q}) = \tau_0(q,\dot{q}) - \upsilon_0(q,\dot{q}) = \frac{1}{2} L\ \dot{q}_L^2 - \frac{1}{2}\frac{q_C^2}{C}$$

(10) $$\psi_0(q) = \frac{1}{2} r_T \dot{q}_L^2 + \frac{1}{2} r_L \dot{q}_L^2 + \frac{1}{2} r_C \dot{q}_C^2 + \frac{1}{2} R(\dot{q}_L - \dot{q}_C)^2$$

(11) $$F_{qL}^0 = E \ ; \ F_{qC}^0 = 0$$

By averaging the Lagrange equations of (4)-(7) with (8)-(11), can present the state equation of the system as below:

(12) $$X = [x_1, x_2] = [i_{L1}, v_C] = [\dot{q}_{L1}, \frac{q_C}{C}]$$
$$\dot{X} = AX + BU \ ; Y = CX + DU$$

(13) $$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}-\frac{r+r_C}{L_1} & \frac{r_C}{L_1}\\ \frac{1}{C} & -\frac{R+r_C}{L_2}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix} + \begin{bmatrix}\frac{d}{L_1} & -\frac{1-d}{L_1}\\ 0 & 0\end{bmatrix}\begin{bmatrix}E\\ 0\end{bmatrix}$$

Where r is sum of inductor and transistor or $r=r_L+r_T$.

Then by dissolving the state equation in the s domain can extract the dynamic transfer functions of the output voltage respect to other key variables where are presented in formulas (14) to (18).

(14) $$Y(s) = \left[C(SI - A)^{-1} B + D\right] X(s)$$

(15) $$G_v(s) = \frac{v_o(s)}{v_i(s)} = d.\frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}}$$

(16) $$G_d(s) = \frac{v_o(s)}{d(s)} = V_I.\frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}}$$

(17) $$Z_o(s) = \frac{v_o(s)}{i_o(s)} = (R \,||\, r).\frac{(1 + \frac{s}{\omega_z})(1 + \frac{s}{\omega_{zl}})}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}}$$

Where, G_v is the audio success-ability transfer function, G_d is control to output ratio and Z_o is the equivalent impedance seen from converter output. For example G_d is illustrated in Fig.3. So sub-function parameters are:

(18) $$\omega_o = \frac{1}{\sqrt{LC}}; \ \omega_z = \frac{1}{r_C.C}; \omega_{zl} = \frac{r}{L}; \ Q = \frac{R}{\sqrt{\frac{L}{C}}}$$

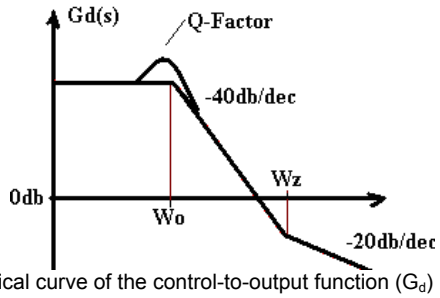

Fig.3. Typical curve of the control-to-output function (G_d)

Voltage controlled converter with PI compensator

The studied converter overall circuit is shown here. Converter output voltage first will be divided by R_1 and R_2, and then its difference with reference voltage applies to U_1 error amplifier, afterward U_2 compare the compensator error with fixed frequency ramp signal, finally the U_2 output controls the transistor states in the complementary manner.

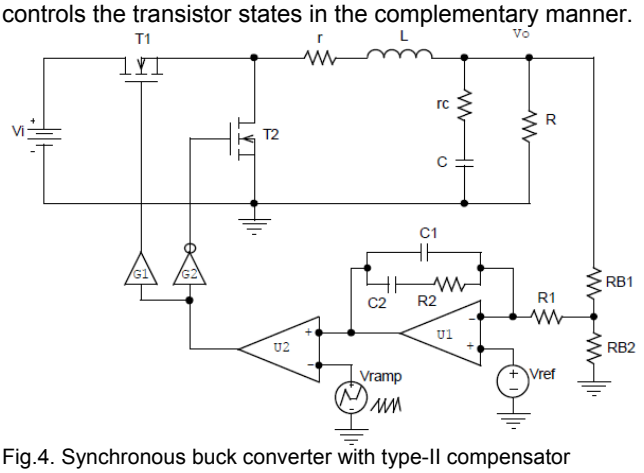

Fig.4. Synchronous buck converter with type-II compensator

Hence, the converter overall block diagram could be presented in the form shown in Fig.5.

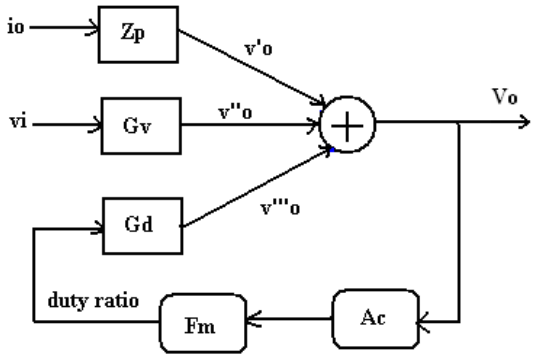

Fig.5. Converter overall block diagram

It is requisite to determine the compensator (A_C) and modulator (F_m) functions before the converter closed-loop analysis. Fig.6. shows the A_C Circuitry and its transfer function is stated in formula 19.

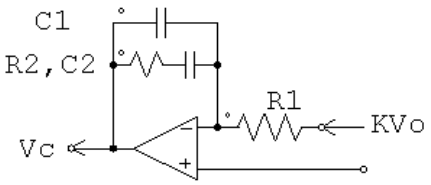

Fig.6. Compensator circuitry

$$A_C(s)=\frac{v_C(s)}{v_O(s)}=\frac{\beta(s+\omega_{Zc})}{s(s+\omega_{Pc})} \tag{19}$$

$$\beta=\frac{k}{C_2(R_1+R_{B1}\parallel R_{B2})};\omega_{Zc}=\frac{1}{R_2C_1};\omega_{Pc}=\frac{1}{R_2(C_1\parallel C_2)}$$

Modulator compares the v_C with ramp signal amplitude v_{Rm} and makes the duty ratio, so its function would be:

$$\frac{v_C}{v_{Rm}}=\frac{d}{1}\Rightarrow F_m=\frac{d}{v_C}=\frac{1}{v_{Rm}} \tag{20}$$

The control block diagram is a three input and single output system driven by three independent sources: v_r, v_i and i_o.

The ac component of the input voltage v_i can be viewed as a disturbance caused by a low frequency ripple voltage variations of the line voltage. For a constant dc output voltage v_r is 0. The loop gain of converter, system transfer functions and output voltage in the closed loop condition is:

$$T(s)=A_C.F_m.G_d=$$

$$=\frac{\beta(s+\omega_{Zc})}{s(s+\omega_{Pc})}.\frac{1}{v_{Rm}}.V_I.\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \tag{21}$$

$$Z_{Pcl}=\frac{Z_P}{1+T};G_{Vcl}=\frac{G_V}{1+T};G_{dcl}=\frac{G_d}{1+T} \tag{22}$$

$$v_o=G_{Vcl}.v_i+G_{dcl}.v_r+Z_{Pcl}.(-i_o) \tag{23}$$

Formula 23 could be illustrated as Fig. 7.

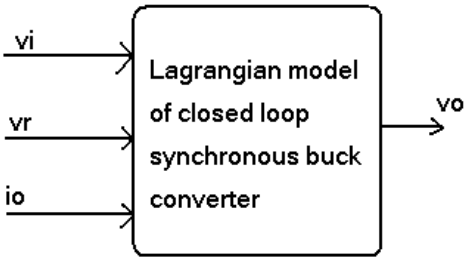

Fig.7. illustration of formula 23

To determine the influence of step change of any three variables (v_i, v_r, i_o) on the converter output voltage, it is sufficient to multiply the corresponding transfer function by the changed amplitude in s domain as stated by the following formulas [12].

$$\Delta v_o(t)=\ell^{-1}(\frac{G_V}{1+T}.\Delta v_i) \tag{24}$$

$$\Delta v_o(t)=\ell^{-1}(\frac{G_d}{1+T}.\Delta v_r) \tag{25}$$

$$\Delta v_o(t)=\ell^{-1}(-\frac{Z_P}{1+T}.\Delta i_o) \tag{26}$$

Where ℓ^{-1} is the inverse-laplacian operator.

The delay time (t_d) introduces by power transistors driver and pulse width modulator can be described by the function $H_d(s)$ from dc to half of the switching frequency (0 – $f_s/2$) that is approximated in formula (27).

$$H_d(s)=e^{-st_d}=\frac{1-\frac{st_d}{2}}{1+\frac{st_d}{2}}=\frac{s-\frac{2}{t_d}}{s+\frac{2}{t_d}}=\frac{s-\omega_y}{s+\omega_y};\omega_y=\frac{2}{t_d} \tag{27}$$

Then, delayed loop gain transfer function will be as formula (28).

$$T_d(s)=H_d(s)T(s)=H_d(s).A_C.F_m.G_d \tag{28}$$

Simulation results

This section involves the discussed converter simulation results that are done by Pspice and Matlab software's.

The task of the feedback compensation network is to shape the loop gain such that it has a crossover frequency

at the desired place with enough phase and gain margins for a good dynamic response, line and load regulation, and stability.

First consider the converter shown in Fig.4 with values stated in Table.1.

Table 1. The converter components value

Converter components		Controller components	
Part	Value	Part	Value
		R_{B1}	40KΩ
V_I	20V	R_{B2}	10KΩ
L	0.05mH	R_1	100Ω
r_L	0.1Ω	R_2	25KΩ
C	33uF	C_1	10pF
r_C	0.01Ω	C_2	1.5nF
R	2Ω	V_{ref}	1V
r_T	0.1Ω	V_{ramp}- max	2V
V_{out}- desired	5V	f_s	250 KHz
		t_d , delay	0.1us

By using formulas (18-20) and (27), one can compute the converter model frequencies and factors where are stated in the following table.

Table 2. the converter model frequency specifications

Symbol	Value	Symbol	Value
ω_o	24.61K rad/sec	ω_{Zc}	4Meg rad/sec
ω_z	3.03Meg rad/sec	ω_{Pc}	26.66K rad/sec
ω_{zl}	4K rad/sec	β	16.46K sec^{-1}
Q	1.62	ω_y	20Meg rad/sec
		F_m	0.5

Fig.8. exhibits Bode plot of the open loop converter control-to-output ($G_d(s)$) transfer function.

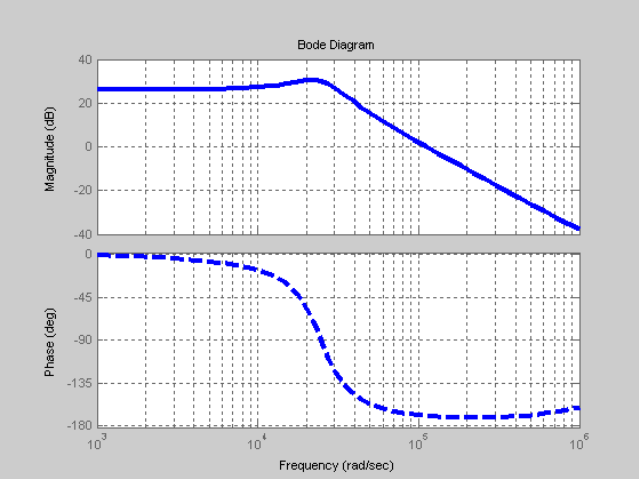

Fig.8. Bode plot of the control-to-output gain (open loop)

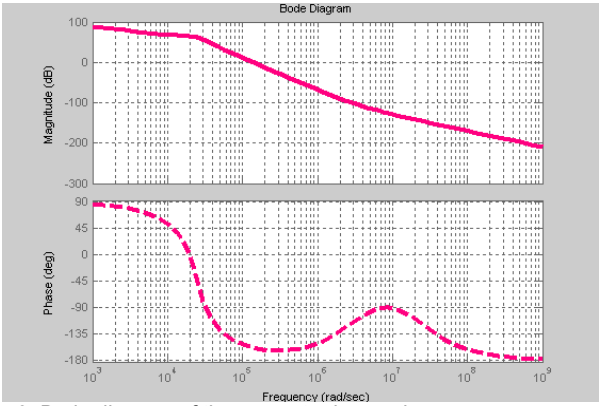

Fig.9. Bode diagram of the converter loop gain

Fig.9 shows the bode diagram of the converter loop gain T(s). As it seen, cross over frequency is about 150K rad/sec (23.87 KHz) or lower than one-tenth of the switching frequency. Also phase margin of the loop gain is about 30° where makes a suitable stable boundary.

For the abridgement, no further transfer function plots such as $G_v(s)$, $G_{vcl}(s)$, $Z_o(s)$ are presented here.

Using formula (24), one can easily find the influence of step change of input voltage on the output voltage. The transient component of the output voltage $v_o(t)$ can be obtained using inverse laplace transform of $v_o(s)$.

Fig.10 shows a step response of the output voltage to a change in input voltage (namely audio success-ability).

Circuit simulation result is denoted by "sim" and Lagrange modelling result is denoted by "mdl".

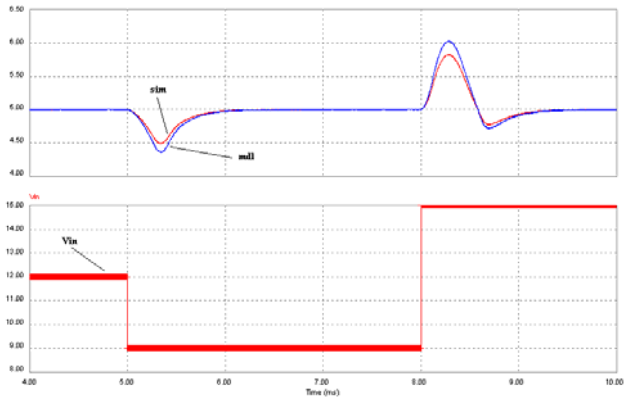

Fig.10. Response of output voltage to step change in input voltage

Similarly, using formula (25) one can find the output voltage response to reference voltage where is depicted in Fig.11. Here V_{ref} changes from 5V to 8V at time 8ms.

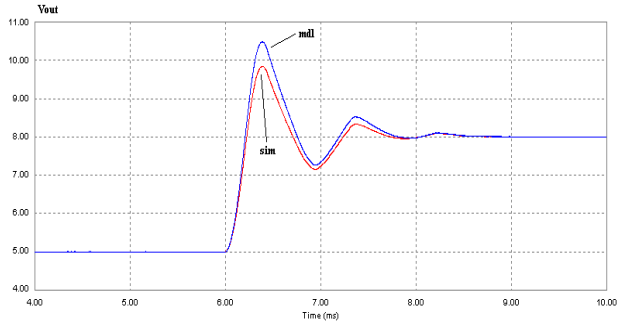

Fig.11. Response of output voltage to step change in reference

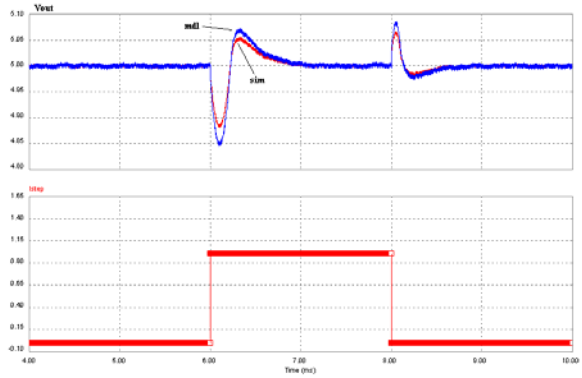

Fig.12. Response of the output voltage to load current changes

Step changes in the load current are obtained using an active load that acts like a current sink. Formula (26), represents the output load influence on the output voltage. Fig.12 shows a step response of the output voltage to a step change of output current which steps up from 0A to 1A at t=8ms and then steps down from 1A to 0A at t=12ms respectively. For this purpose we parallel a pulse current

along with output load R_L. For decreasing the overshoot in Fig.12 It is feasible to add some phase boost in the controller function to increase the phase margin.

Conclusion

This paper introduces a powerful tool for modelling the voltage controlled synchronous buck converter using Lagrange energy equation. Physical essence of this method introduces better insight to system operation comparing with traditional state space method where almost is a mathematical tool.

Dynamic behaviour of the converter is analysed in both frequency and time domain such as transfer functions and step response. Furthermore, full order dynamic model is improved by taking into consideration the parasitic elements such as switch, inductor and capacitor equivalent resistors.

A type-II compensator is employed in the feedback loop to stabilize the output voltage from fluctuations of source and load changes. Since this method relying on averaging then the yielded model is validate up to half of the switching frequency according to nyquist theorem.

Finally, the obtained simulation results confirm the superiority of this method over other traditional techniques. In the near future, this dynamic model will be verified by applying experimental results.

Authors

Atila Skandarnezhad, eskandarnejad@aliabadiau.ac.ir
Faculty Member of Electrical Engineering,
Department of Electrical Engineering, Aliabad Katoul Branch, Islamic Azad University, Aliabad Katoul, Iran.

Amangeldi Kochaki, koochaki@aliabadiau.ac.ir
Faculty Member of Electrical Engineering,
Department of Electrical Engineering, Aliabad Katoul Branch, Islamic Azad University, Aliabad Katoul, Iran

Yaghoob Mohammadmoradi,
MohammadMoradi@aliabad.ac.ir
Faculty Member of Electrical Engineering,
Department of Electrical Engineering, Aliabad Katoul Branch, Islamic Azad University, Aliabad Katoul, Iran.

AbdolAziz Kalteh, kalte@aliabadiau.ac.ir
Faculty Member of Electrical Engineering,
Department of Electrical Engineering, Aliabad Katoul Branch, Islamic Azad University, Aliabad Katoul, Iran.

* The correspondent E-mail is:
eskandarnejad@aliabadiau.ac.ir

REFERENCES

[1] Zdanowski M., Rąbkowski J., Barlik R., High frequency DC/DC converter with Silicon Carbide devices - simulation analysis, *Przegląd Elektrotechniczny*, 02(2014), 201-205.

[2] Bogusz P., The laboratory stand for testing of light electric vehicles drives - design and implementation, *Przegląd Elektrotechniczny*, 01(2014), 16-20.

[2] Shepherd W., Zhang L., Power Converter Circuits, Marcel Dekker, New York, 2004.

[4] Kursun V., Narendra S., Vivek K., Friedman G., Efficiency Analysis of a High Frequency Buck Converter for On-Chip Integration with a Dual-VDD Microprocessor, ESSCIRC 2002, 743-746.

[5] Gajowik T., Rafał K., Bobrowska M., Bi-directional DC-DC converter in three-phase Dual Active Bridge Topology, *Przegląd Elektrotechniczny*, 05(2014), 14-20.

[6] Curry, J., Hamiltonian and Lagrangian Mechanics, Vol.1, ed.2, CSI Publishing, USA, 2013.

[7] Hand L. N. and Finch, J. D., Analytical Mechanics, Camb. Univ. Press, UK, 1999.

[8] Ramirez, S. H., et al., Passivity-Based Control of Euler-Lagrange Systems, Springer, London, 1998.

[9] Kazmierczuk, M. K., Pulse Width Modulated DC-DC Power Converters, Wiley, Ohio, 2008.

[10] Joseph N., Control and Analysis of Synchronous Rectifier Buck Converter for ZVS in Light Load Condition, International Journal of Advanced Research in Electrical,Electronics and Instrumentation engineering 02(2013), NO.06, 2440-2447.

[11] SiC ZERO RECOVERYÒ Schottky Diode Reliability at Extremely High Voltage Slew Rates, CPWR-RS01, Rev A, "www.cree.com".

[12] Jardini J.A., and et al., Power flow control in the converters interconnecting AC-DC meshed systems, *Przegląd Elektrotechniczny*, 01(2015), 46-49.