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A Fully-Balanced Current-Tunable Integrator with CAPRIO Technique

Abstract. *This paper describes the improvement of an integrable fully-balanced wide-frequency current-turnable integrator with Caprio technique. The architecture of the circuit is relatively simple and symmetrical with different signals. The circuit of our interest are the integrator circuits as the basic functional circuit for current mode filters and the Caprio technique translated to integrator for an implementation of low input impedance differential current input. After the hand setting of the circuit parameters of Caprio technique, they were optimized to improve total harmonic distortion and intermodulation performance. The proposed conversion circuit is simple, very suitable for application and implementing. Experimental and simulation results found in a good with theoretical analysis are included.*

Streszczenie. *W artykule opisano zrównoważony, szerokoczęstotliwościowy integrator wykorzystujący technikę CAPRIO. Układ może być stosowany w filtrach z wejściem prądowym o małej impedancji.* ***Zrównoważony integrator strojony prądowo wykorzystujący technikę CAPRIO****.*

Keywords: fully-balance, Caprio technique, sensitivities, harmonic distortion.
Słowa kluczowe: integrator, technika CAPRIO.

Introduction

Integrators are most important circuits in many applications such as the integrated receivers [1], quadrature sinusoidal oscillators [2,3], digital modulators [4] and PID controllers [5]. It is usually desirable to have the fully balanced circuits with different signals [6,7]. The various techniques of differential integrator circuits have previously been reported in the literatures [1–9]. These techniques have many advantages such as linearity circuits, wide dynamic range, wide band, current tunable, simple circuit, low total harmonic distortion and low power consumption. Fully balanced techniques can suppress even order harmonics. However, such techniques total repeatedly suffered from high amplitude of even order harmonics and limited harmonic distortion. After the analysis of different current mode building circuit, we selected the npn transistor as a current follower and the Caprio technique as differential input current follower [10-11]. Because of the cross-coupled translinear configuration Caprio's quad has inherent base-emitter voltage (VBE) cancellation and provides a very linear voltage-to-current conversion [11].

In this paper, a fully-balanced current-tunable integrator with Caprio technique is introduced using two simple fully balanced devices, i.e. a conventional first order lowpass filter and a first order lowpass filter with Caprio's quad circuit. The even order harmonics can be suppressed by Caprio's quad circuit. The sensitivities of the circuit are summarized. Other Gm-C approachs are also compared and discussed.

The proposal for a fully-balanced current-tunable Integrator with linearization

Fig.1 shows the basic circuit configuration of a fully-balanced current-tunable integrator with Caprio's quad (A_{int}). All npn transistors Q1 to Q10 are matched. The circuit consists of two fully balanced components, i.e. a first order lowpass filter with Caprio's quad circuit A_{LPF1} consists of Q1,Q2,Q5-Q8,Q9,Q10 and a first order lowpass filter A_{LPF2} consists of Q3,Q4,Q5-Q8. Firstly, the differential amplifier of a perviouslys reported [12-14] circuit A_{LPF1} is modified with Caprio's technique and consists of a different pair (Q1, Q2), a Caprio's quad (Q9, Q10), a current sink I_f and the four loading diode-connected transistors Q5 to Q8. The input voltage of A_{LPF1} is a small-signal voltage v_{AB} between the bases of transistors (Q1, Q2). The small-signal output voltage v_{DE} of A_{LPF1} is taken across the emitters of transistors (Q5, Q6) between nodes D and E.

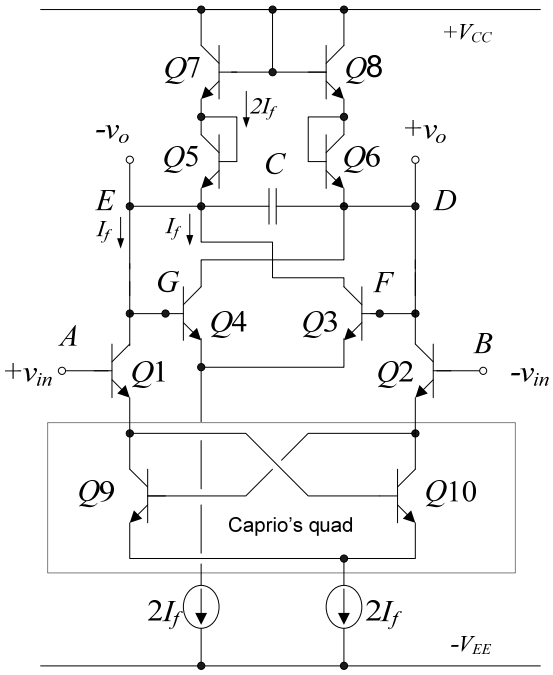

Fig.1. A fully-balanced current-tunable integrator with Caprio's quad

Secondly, the first order lowpass filter A_{LPF2} is a previously reported [15-17] lowpass filter circuit consists of a differential pair (Q3, Q4), a capacitor C, a current sink I_f and the same four loading diode-connected transistors Q5 to Q8 of A_{LPF1}. The small-signal input voltage of v_{DE} of A_{LPF2} between the bases of transistors (Q3, Q4) is obtained from the small-signal output voltage vo of A_{LPF1}. The small-signal output voltage of A_{LPF} is taken across the emitters of transistors (Q5, Q6) between nodes D and E.

In Caprio's cross-quad, all four transistors Q1, Q2, Q9 and Q10 have the npn transistor and are perfectly matched can be seen from Fig.1. The gate-source voltages for Q9 to Q1 are the same as the gate-source voltages for Q10 to Q2 since the current flowing through the left branch of the cross quad is the common to Q9 to Q1, while the current flowing

through the right branch is common to Q10 to Q2. Caprio proposed a precision differential voltage-current converter linearization technique [10].

Finally, the transfered function of fully-balanced current-tunable Gm-C integrator with Caprio's quad is $A_{int}=V_o/V_{in}$ where $V_{in}=V_{AB}$ and $V_o=V_{DE}$. It can be seen from Fig.1 that the circuit is fully balance with Caprio's quad.

Circuit Realization and Analysis

Referring to Fig.1, A current sink I_f passing through the transistor Q1, Q2, Q3, Q4, Q9 and Q10 where $r_{e1}=V_T/I_f$ is the small-signal emitter resistance of transistor Q1, Q2, Q3, Q4, Q9 and Q10, and V_T is the usual thermal voltage of approximately 25 mV associated with an PN junction at room temperature. On the other hand, current sink $I_f+I_f=2I_f$ passing through the transistor Q5, Q6, Q7 and Q8 where $r_{e2}=V_T/(2I_f) = r_{e1}/2$ is the small-signal emitter resistance of transistor Q5, Q6, Q7 and Q8.

Firstly, the different amplifier with Caprio' quad circuit (A_{LPF1}) is considered. The output voltage v_{DE} of A_{int} is obtained through superposition, i.e. $v_{DE}=v_{o1}+v_{o2}$. The voltage v_{01} is the output voltage v_{DE} of A_{LPF1} when the input voltage v_{AB} of G is activated, i.e. $v_{AB}=v_{in}$ but the input voltage V_{FG} of A_{LPF2} is temporary deactivated or separately connected to an ac ground, i.e. $v_{FG}=0$. In contrast, the voltage v_{02} is the output voltage v_{DE} of A_{LPF2} when the input voltage v_{AB} of A_{LPF2} is activated, i.e. $v_{FG}=v_{DE}$ but the input voltage v_{AB} of A_{LPF1} is temporary deactivated or separately connected to an ac ground, i.e. $v_{AB}=0$.

On the other hand, voltage v_{01} can be found at $v_{FG}=0$. Therefore, the input voltage v_{AB} of A_{LPF1} enables a small-signal emitter current $i_{e1}=v_{AB}/(4r_{e1})$ passing through the emitters of Q1, Q2, Q9 and Q10. The resulting small-signal collector current of Q1 and Q2 is $i_{c1}\cong i_{e1}$. Most of i_{c1} passes through a loading impedance $Z=4r_{e2}/(1+s\tau)$ formed by Q5-Q8 where $\tau=4r_{e2}C=2r_{e1}C$ is the small-signal emitter resistance of either Q5, Q6, Q7 or Q8. The resulting output voltage of A_{LPF1} is $v_{o1}\cong i_{e1}Z$, therefore $A_{LPF1}=v_{o1}/v_{AB}=½(1+s\tau)$ represents a first order lowpass filter with Caprio' quad circuit.

On the other hand, voltage v_{02} can be found at $v_{AB}=0$. Therefore, the input voltage v_{FG} of A_{LPF2} enables a small-signal emitter current $i_{e2}=V_{FG}/(2r_{e1})$ passing through the emitters of Q3 and Q4. The resulting small-signal collector current of Q3 and Q4 is $i_{c2}\cong i_{e2}$. Most of i_{c2} passes through the same loading impedance $Z=4r_{e2}/(1+s\tau)$ formed by Q5-Q8. The resulting output voltage of A_{LPF2} is $v_{o2}\cong i_{e2}Z$, therefore $A_{LPF2}=v_{o2}/v_{FG}=1/(1+s\tau)$ represents a conventional first order lowpass.

Finally, the output voltage v_{DE} of A_{int} is $v_{DE}=v_{o1}+v_{o2}=v_{AB}/2(1+s\tau)+v_{FG}/(1+s\tau)$. As $v_{DE}=v_{FG}=v_o$ and $v_{AB}=v_{in}$, therefore $A_{int}=v_o/v_i$ represents a fully-balanced current-tunable Gm-C integrator with Caprio's quad of the form

$$A_{\text{int}}=\frac{1}{s\tau} \quad (1)$$

The corner frequency of (1) is $\omega_0=1/\tau=1/(4r_{e2}C)$ where $r_{e2}=V_T/(2I_f)$. The corner frequency ω_0 is current tunable by I_f of the form

$$\omega_o=\frac{I_f}{2CV_T} \quad (2)$$

caprio's Redue the even order by Volterra series

Caprio technique appears as a perspective current mode, differential input topology with very low input impedance and wide bandwidth. Through a Volterra series analysis, the third-order intermodulation components (IM3) of the output voltage V_{out} at frequency $f+2\Delta f$ can be expressed as

$$IM3_{Cap}\approx\left|\frac{A_{in}^2}{8g_m^3R_{ee}^3V_T^2}\frac{f}{f_T}\right| \quad (3)$$

The parameters A_{in}, g_m, R_{ee}, f_T can be obtained using the procedure described in [16]. IIP3 can be solved from eqs. (3) by setting $IM3_{Cap}$ = 1 as follows

$$VIIP3_{Cap}\approx 2\sqrt{2V_T}\sqrt{\frac{g_m^3R_{ee}^3f_T}{f}} \quad (4)$$

where $VIIP3_{Cap}$ represents the third-order input referred intercept point voltage of Caprio's Quad. $VIIP3_{Cap}$ can be further simplified as

$$VIIP3_{Cap}\approx\sqrt{\frac{f_TI_T^3R_{ee}^3}{fV_T}} \quad (5)$$

where I_T is the overall current consumption.

Sensitivities

Generally, a sensitivity of y to a variation of x is given by $S_x^y=[\partial y/\partial x][x/y]$ where y is a parameter of interest and x is a parameter of variation [19]. Since, the thermal voltage V_T, capacitance C and current sink I_f also represent effect of temperature on the corner frequency ω_0, as shown in equation (2). Therefore, Table 1 shows the sensitivity S_x^y where (x, y)=(C, ω_0), (V_T, ω_0) or (I_f, ω_0). Consequently, it can be seen from Table 1 that the sensitivities of ω_0 are relatively constant between –1 to 1. Such sensitivities are unlike existing approaches [20,21].

Table 1. Sensitivity S_x^y where (x, y)=(C, ω_0), (V_T, ω_0) or (I_f, ω_0).

$S_C^{\omega_o}$	$S_{I_f}^{\omega_o}$	$S_{V_T}^{\omega_o}$
-1.0	1.0	-1.0

Simulation Results

The performance of the circuit shown in Fig.1 has been simulated using a PSpice [22]. The npn transistors are modeled by CA3127, whose transition frequency f_T is at 300 MHz. Fig.2 illustrates magnitude (dB) and phase shift (degrees) of v_o/v_{in} versus frequency (Hz) obtained from the simulation using, for example, capacitor C = 0.08μF and I_f = 0.8 μA, 8 μA, 80 μA and 800 μA.

It can be seen from Fig.2 that, the corresponding frequency ω_o, where the magnitude of v_o/v_{in} becomes 0 dB for individual values of I_f are at 120 Hz, 3.80 kHz, 55 kHz and 555 kHz, respectively, and the corresponding phase shifts for individual values of I_f are all approximately -89 degree.

Fig.3 depicts the simulation results of both the corner frequencies (Hz) and the corresponding phase shift (degrees) of v_o/v_{in}, where the magnitude of v_o/v_{in} becomes 0 dB, versus the bias current I_f(A), using capacitor C = 0.08 μF. For the comparative purposes, the ideal (expected) results are also included. It can be seen from Fig.3 that both the expected and the simulated results are consistent, and the frequency f_o is linearly current-tunable over a "wide-frequency" sweep range of approximately 3 orders of magnitude.

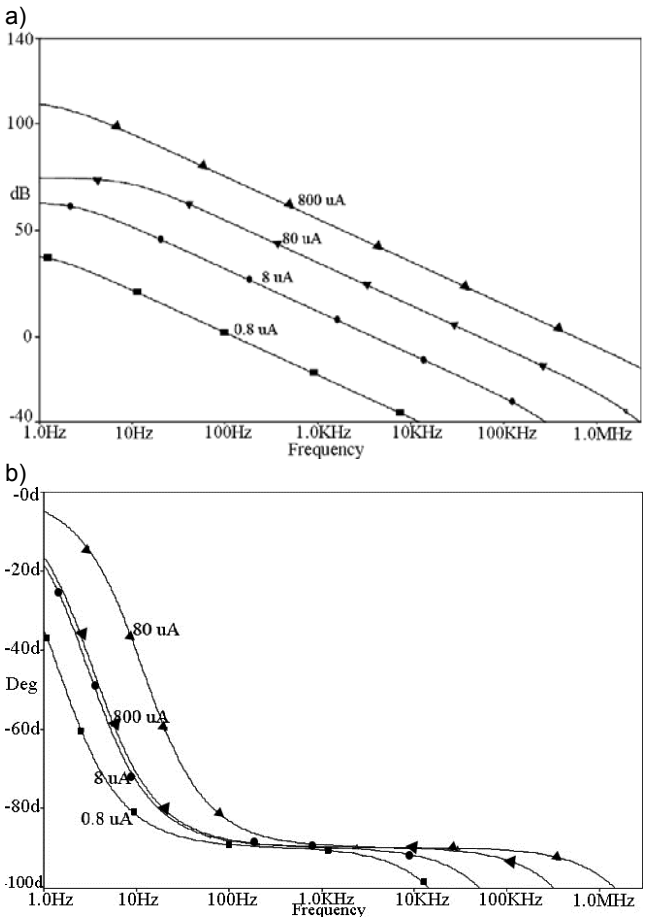

Fig.2. Magnitude (dB) and phase shift (degree) of v_o/v_{in} versus frequency (Hz) using the capacitance C = 0.08 μF and current I_f = 0.8 μA, 8 μA, 80 μA, and 800 μA

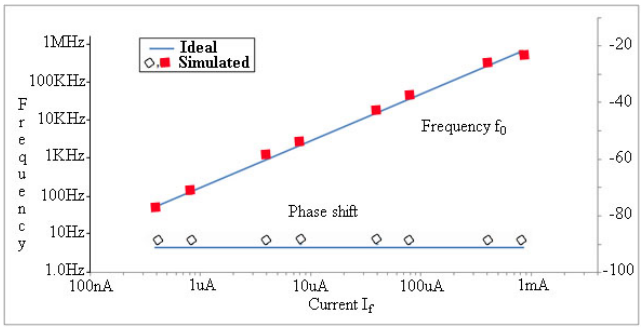

Fig.3. Corner frequency (Hz) and the corresponding phase shift (degree) of v_o/v_{in} versus the bias current I_f(A) , using a fixed capacitance C of value 0.08 μF

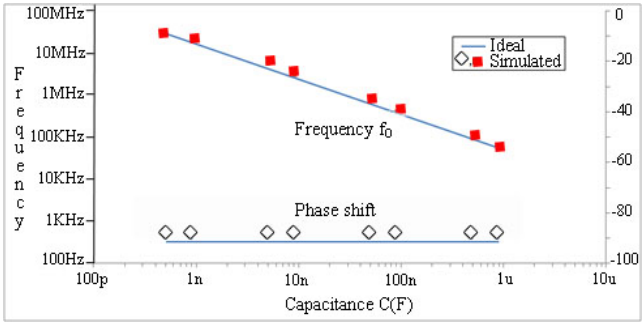

Fig.4. Corner frequency (Hz) and the corresponding phase shift (degree) of v_o/v_{in} versus the capacitance C(F), using a fixed bias current I_f value 800 μA.

Fig.4 shows the simulation results of both the corner frequencies (Hz) and the corresponding phase shift (degrees) of v_o/v_{in}, where the magnitude of v_o/v_{in} becomes 0 dB, versus the capacitance C, using a fixed bias current I_f of value 800 μA. For the comparative purposes, the ideal (expected) results are also included. It can be seen from Fig. 4 that both the expected and the simulated results are linear and consistent, by using a minimum frequency setting capacitance of 40 pF, the upper frequency f_o can be expected at 29 MHz.

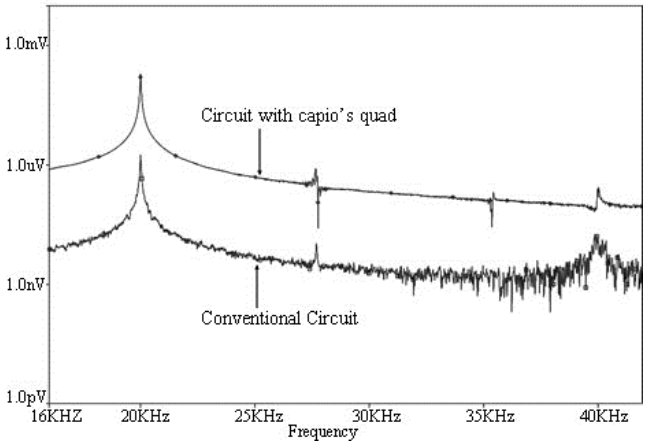

Fig.5. illustrates harmonic spectrums comparison of conventional circuit and circuit with Caprio's quad

Fig. 5 shows the simulation results of the two harmonic spectrums. The conventional circuit consist of transistor Q1 to Q8 where the transistor Q9 and Q10 of the Caprio's quad are short circuit. The results show that the conventional circuit is high harmonics at 27 kHz, 35 kHz, and 40 kHz. An improved circuit with Caprio's quad results in reducing those high harmonics. Consequently, the total harmonic distortions (THD) are reduced from 4.32 % to 1.94 %.

Conclusion

A fully-balanced current-tunable integrator with Caprio technique has been proposed. The architecture of the circuit is symmetrical with different signals. The circuit is also relatively simple and integrable on-chip. Both simulated and ideal results are consistent. It is a simple procedure that has been presented for approximating the transfer characteristic of linearized bipolar emitter-coupled pairs. Sensitivities of either the ω have been constant between –1 to 1 independent of variables. The comer frequency is highly linearly current-tunable over a wide-frequency sweeping range of three orders of magnitude. The maximum useful corner frequency is around 29 MHz. By using better transistors of much higher F_t (e.g. in the region of several GHz) and much smaller value of C (e.g. using stray capacitance), much higher values of the corner frequency. It results in reducing even harmonics distortion, as suggested by Caprio's technique.

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