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An Analysis Of Overload Conditions In Mosfet-Based Power Resonant DC-DC Step-Up Converters In Switched Capacitor Voltage Multiplier Topology

Abstract. *This paper presents an analysis of operation of resonant DC-DC converter in topology of Switched Capacitor Voltage Multiplier (SCVM) under overload conditions. The SCVM operates as a charge pump, thus the energy transfer rate is limited and depends on the switched capacitance and the switching frequency. However an overload of the converter introduces specific operation conditions that can require a special control. The presented research results have an important significance for selection of components of SCVM as well as switching strategy, because the overload can occur as a result of load decrease as well as during the start of the converter. In the paper analytical, simulation and experimental results are presented for the Mosfet-based 200 Watt SCVM.*

Streszczenie. *W artykule przedstawiono analizę możliwości pracy w stanie przeciążenia układu rezonansowego przekształtnika mocy DC-DC podwyższającego napięcie w topologii powielacza napięcie (SCVM – Switched Capacitor Voltage Multiplier). Układ o przełączanych kondensatorach działający na zasadzie pompy ładunku ma ograniczaną moc zdeterminowaną pojemnością przełączanych kondensatorów oraz częstotliwością przełączeń. Jednak przeciążenie przekształtnika wywołuje specyficzny stan pracy, który może wymagać specjalnego sterowania. Badania mają istotny wpływ na dobór sterowania w układzie SCVM, ponieważ przeciążenie może występować jako skutek wpływu odbiornika, ale również przy starcie układu. W artykule przedstawiono badania analityczne, symulacyjne oraz eksperymentalne przekształtnika tranzystorowego SCVM z tranzystorami Mosfet, w zakresie mocy do 200 watów. (**Analiza stanu przeciążenia przekształtników rezonansowych DC-DC o przełączanych kondensatorach podwyższających napięcie zrealizowanych w technice Mosfet w topologii powielacza napięcia**).*

Słowa kluczowe: Przekształtnik wielopoziomowy, przekształtnik DC-DC, przełączane kondensatory, pompa ładunku
Keywords: Multilevel converter, DC-DC converter, switched-capacitor, voltage multiplier, charge pump

Introduction

DC-DC power electronic converters in a switched-capacitor technology can be implemented in systems with high voltage gain required as well as high power switching mode converters achieved with the use the thyristor-based technology. A charge pump concept is well established in low power circuits but can also be adopted into power electronic area in dedicated topologies and design [1]-[12]. In this type of a power electronic converter the high efficiency, reliability and low cost can be achieved by the utilization of a proper topology [2]-[12], dedicated switches, and in the vast majority of instances in resonant circuits to achieve limitation of currents, zero current switching operation and sufficient quality factor and high efficiency.

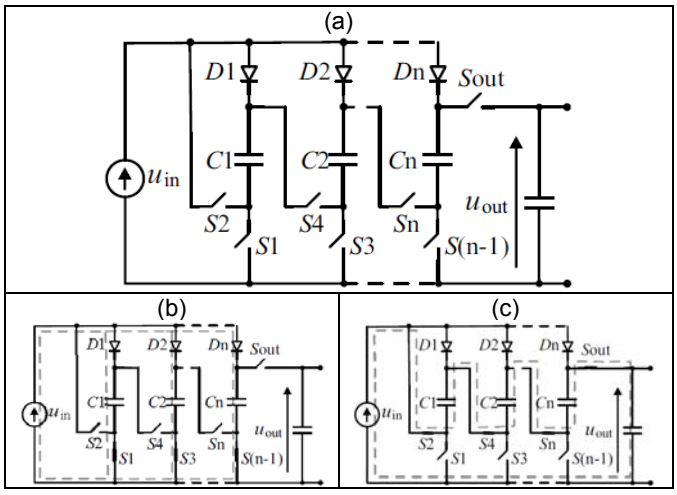

Fig.1. DC-DC converter in the Switched Capacitor Voltage Multiplied topology (a), and stages of charging (b) and discharging of switched capacitors (c).

The switched capacitor multipliers concept differs from the well-established flying capacitor multi-cell converters [13]-[15]. Fig.1 presents a topology of a switched-capacitor voltage multiplier (SCVM), and the current flow in stages of charging and discharging of switched capacitors.

In order to achieve ZCS conditions and sufficient quality factor resonant circuits need to be created in the circuits where a switched capacitor is recharging. When the converter operates as thyristor-based it is favorable to install a central choke on the input [11], [12]. The Mosfet-based converter can operate with high frequency with the use of parasitic or air inductances. In this case the major inductance can be placed in series with the switched capacitor to be utilized both in the charging and discharging stage. The paper focuses on such solution of Mosfet-based SCVM with the inductance placed in series with a switched capacitor and diode in the output switch branch (D_{out}), as it was presented in Fig. 2.

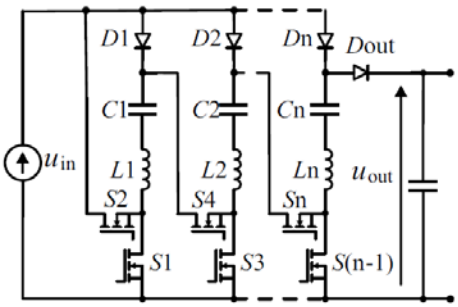

Fig.2. A Mosfet-based SCVM converter with chokes in ZCS circuits and output diode.

Operation of the SCVM and Limit of load

The converter operates in two stages:
- Stage of charging of switched capacitor enabled by switch $S_{1(3,\,5\,...)}$ and diodes (Fig.1b).
- Stage of discharging of switched capacitor and charging the output capacitor enabled by switch $S_{2(4,\,6\,...)}$ (Fig. 1c).

In order to achieve low losses in recharging cycle of a switched capacitor an oscillatory circuit can be created by the application of inductance. The inductance can originate from parasitic parameters of circuits, in low power

converters, or can be designed as an air choke or typical choke, in high power converters. The switching frequency (f_S) is designed below the resonant frequency of LC circuits:

(1) $$f_S < f_0 = \frac{1}{2\pi\sqrt{LC}}$$

where C and L indicates a switched capacitor value and inductance of a cell

The energy is transferred to the output in the discharge stage from the charged switched capacitors and the source. The energy stored in the switched capacitors:

(2) $$\Delta W_C = \frac{1}{2} Cn\left(U_{C\max}^2 - U_{C\min}^2\right)$$

Where: n is the number of cells (n=1 in the analyzed case)

A voltage and current in the switched capacitor circuits are the following, for the zero initial current:

(3) $$u_C = (U_{C\min} - U_{in})\cos\omega_0 t + U_{in}$$

(4) $$i_C = \frac{U_{in} - U_{C\min}}{\rho}\sin\omega_0 t$$

Where: I_0 is an initial current, U_0 is an initial voltage, $\omega_0 = 2\pi f_0$, and ρ is a characteristic impedance of the switched capacitor's charging circuit.

A charging process ends for $\omega_0 t = \pi$, and then the capacitor voltage reaches maximum. Thus from (3) it follows that:

(5) $$U_{C\max} - U_{C\min} = 2U_{in}$$

Using (5) the equation (2) can be presented as follows:

(6) $$\Delta W_C = 2CnU_{in}\left(U_{C\max} - U_{in}\right)$$

The energy transferred to the output in the discharge stage (Fig. 1) is the same as stored in a single capacitor:

(7) $$W_{in\_d} = 2CU_{in}\left(U_{C\max} - U_{in}\right)$$

The power of source is the following (using (3) and (4)):

(8) $$P_{in} = f\left(\Delta W_C + W_{in\_d}\right) = 2CU_{in} f_S (n+1)\left(U_{C\max} - U_{in}\right)$$

The energy transfer rate in the SCVM depends on the switched capacitance and the switching frequency. For the rated power the switched capacitor can operate with nearly full discharging to optimize its volume, thus $U_{C\min}$=0, $U_{C\max}$-$2U_{in}$. It determines the minimum capacitance as a function of power, voltage and frequency:

(9) $$C_{\min} = P_{in}/[2U_{in}^2 f_S(n+1)]$$

Then, the limit of power of the SCVM is the following:

(10) $$P_{in\max} = 2CU_{in}^2 f_S (n+1)$$

When the SCVM reaches the limit of power the switched capacitor can be fully discharged. For higher load power (lower output resistances) or lower switching frequency the operation of the converter varies and the converter goes into specific overload conditions.

An overload conditions in a Mosfet-based SCVM

A Mosfet-based SCVM creates specific conditions in overload mode due to bi-directional conduction of switches. The Mosfet-based SCVM will be analyzed in a case of a single cell converter (Fig. 3). Most of the demonstrated phenomenon are scalable to a n-level converter.

According to the idea presented in Fig. 1 the converter operates be charging and discharging the switched capacitors which is demonstrated in Fig. 4 and Fig. 5 on steady state waveforms in a case of rated load as well as in the overload conditions. When the converter is overloaded the voltage on the switched capacitor reaches zero before the oscillation ends, i.e. during the inductor current flow. As a consequence the switched capacitor is recharging to a negative value. This voltage makes it possible to switch-on the diodes D_1 and diode of S_2 Mosfet (D_{S2}). As a consequence the oscillation of current does not stop in a zero crossing point but starts in a reverse direction in the next half-period. During the charging of the switched capacitor its voltage becomes bigger than the output capacitor before the charging is completed which also triggers oscillation in reverse direction. Fig. 6 presents the stages of oscillation in an overload mode of the Mosfet-based SCVM. The overload can also occur at the start of the converter. Such a case is demonstrated in Fig. 7.

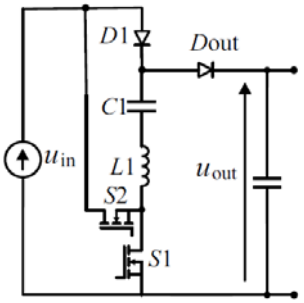

Fig.3. The analyzed case – the single-cell switched-capacitor DC-DC step-up converter.

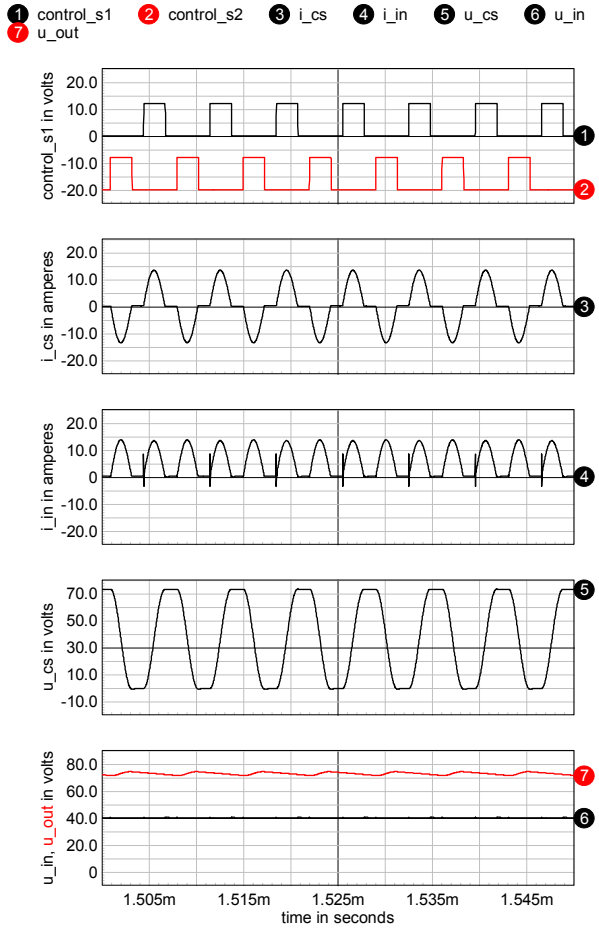

Fig.4. The steady state waveforms in the Mosfet-based SCVM under the rated load conditions. C_1=260nF, L_1=2uH, dead-time=1500ns, R_{out}=26.5Ω, P_{out}=200W, I_{Csrms}=7.6A, I_{Csmax}=13.3, I_{inrms}=7.6A, I_{S1rms}=5.6A, I_{S2rms}=5.2A, U_{Csmax}=73V, U_{Csmin}=-1V, U_{out}=72.6V, T_s=7.0us. ICAP/4 simulation results.

In the operation with too low output resistance the switched capacitor recharges to negative value via the switch S_2 diode. The phenomenon is not dangerous but can have some negative impact on the operation of the converter:

- The peak to peak value of the voltage of the switched capacitors is significantly increased,
- The rms value of currents of the switched capacitors, switches and the input current is slightly decreased,
- The output voltage and power are decreased,
- The converter operates in a hard switching mode which can cause failure or needs increased volume of heatsink.

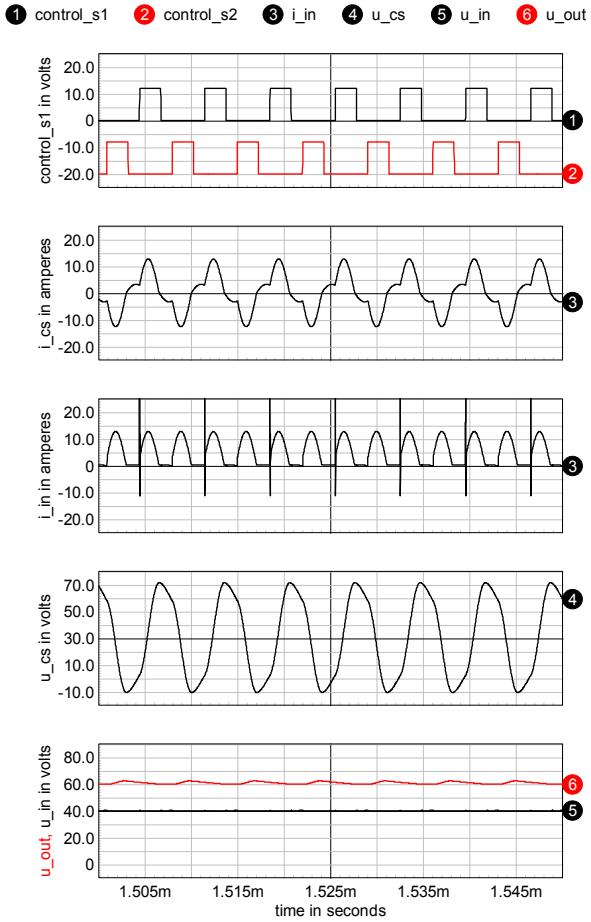

Fig.5. The steady state waveforms in the Mosfet-based SCVM under the overload conditions: C_1=260nF, L_1=2uH, dead-time=1500ns, R_{out}=20Ω, P_{out}=184W, I_{Csrms}=7.3A, I_{Csmax}=12.6, I_{inrms}=7.3A, I_{S1rms}=5.4A, I_{S2rms}=5.4A, U_{Csmax}=71.2V, U_{Csmin}=-10.7V, U_{out}=60.6V, T_s=7.0us. ICAP/4 simulation results.

Detection of the overload

The overload can be detected on the basis of the following parameters of currents and voltages in the converters:

- A voltage on switched capacitor reaches negative values. This is the most explicit symptom of the overload however it is necessary to measure the voltage of switched capacitor to use this function.
- A negative current flow through switches.
- If the SCVM is used as a converter with constant voltage ratio, the voltage drop below the rated range can alert against overload.
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The special switching pattern in the overload mode

The purpose of control of the overload is the following:

- An increase of power and voltage (approaching the rated values),
- Hard switching avoiding,
- Hard switching impact decrease by commutation in lower current.

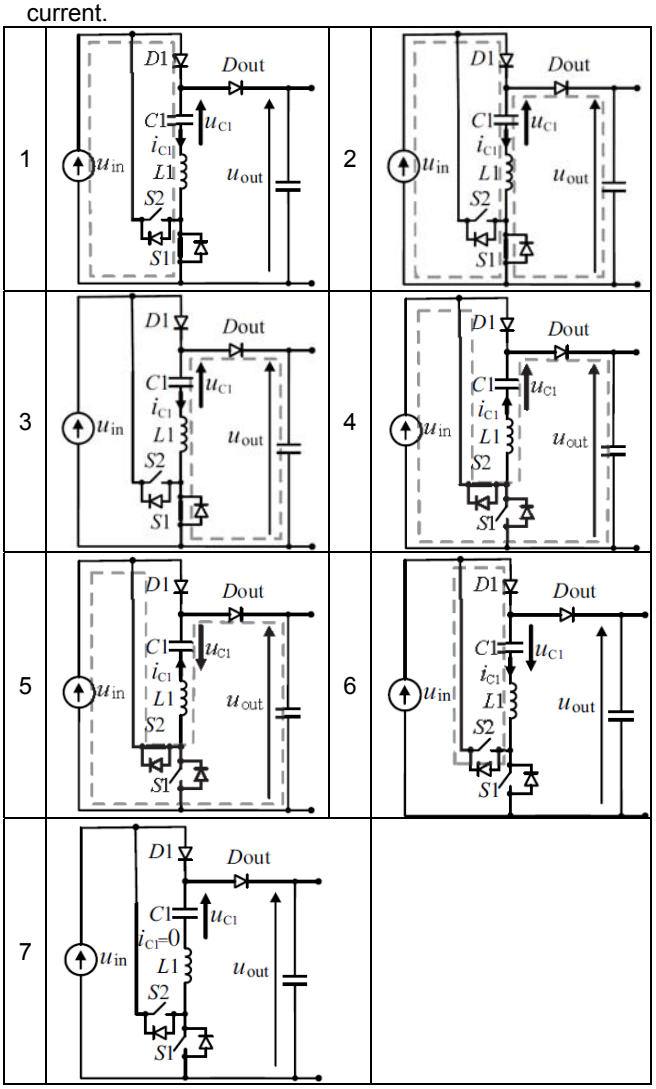

Fig.6. The possible stages of oscillation under the overload operation of the Mosfet-based single-cell SCVM when the current of switched capacitor is continuous.

To manage the overload the following modulation and control strategies can be proposed:

1. The switch S_2 can be turned off during the stage 4 or 5 (Fig. 6, Fig, 8). Switching off the S_2 terminates the current flow from the source and turns on the diode in S_1. Recharging of the switched capacitor to negative values is avoided and the switching frequency is increased which can increase the output voltage and approach to the rated value. The converter operates in hard switching mode.
2. The switch S_2 is switching on during the stage 3 (Fig. 6, Fig. 5) and switch S_1 during the stage 6. This action turns off the conducting diodes. The converter operates in hard switching mode but the moment of switching of corresponding switches determines additional power losses and the losses can be relatively slow if the switching occurs at the beginning or the end of the parasitic oscillation. The converter can operate in this mode in a natural way when the overload occurs.
3. The switch S_2 is not switched on until the stage 3 is finished and the switch S_1 is not switched on until the stage 6 is finished (Fig. 6, Fig. 9). This pattern protects against hard switching. The switching frequency is fairly low to enable that all the seven stages occurs (Fig. 6). this type of control may cause a decrease of switching frequency, a decrease of rated power and a deeper overload.

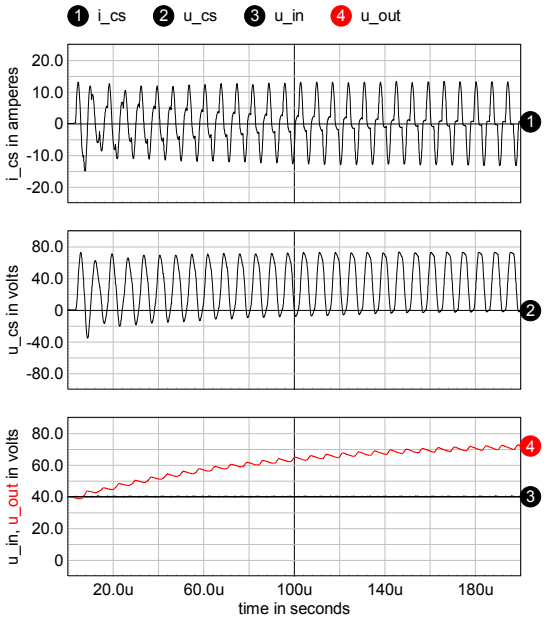

Fig.7. Waveforms during the start of the Mosfet-based single-cell SCVM. C_1=260nF, L_1=2uH, R_{out}=27.5Ω, P_{out_rated}=200W, T_s=7.0us, dead-time=1.5us. ICAP/4 simulation results.

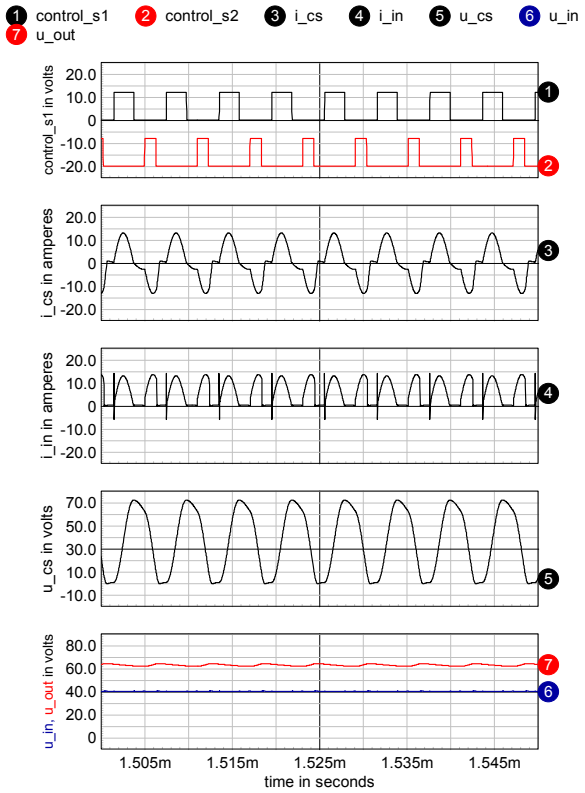

Fig.8 The steady state waveforms under the overload conditions. The idea of the special control by discharging impulse shorting. Hard switching operation of S2 switch. C_1=230nF, L_1=2uH, dead-time=1500ns, R_{out}=20Ω, P_{out}=196W, I_{Csrms}=7.9A, I_{Csmax}=12.9, I_{inrms}=7.7A, I_{S1rms}=5.9A, I_{S2rms}=5.3A, U_{Csmax}=71.9V, U_{Csmin}=-0.8V, U_{out}=62.7V, T_s=6.0us. ICAP/4 simulation results.

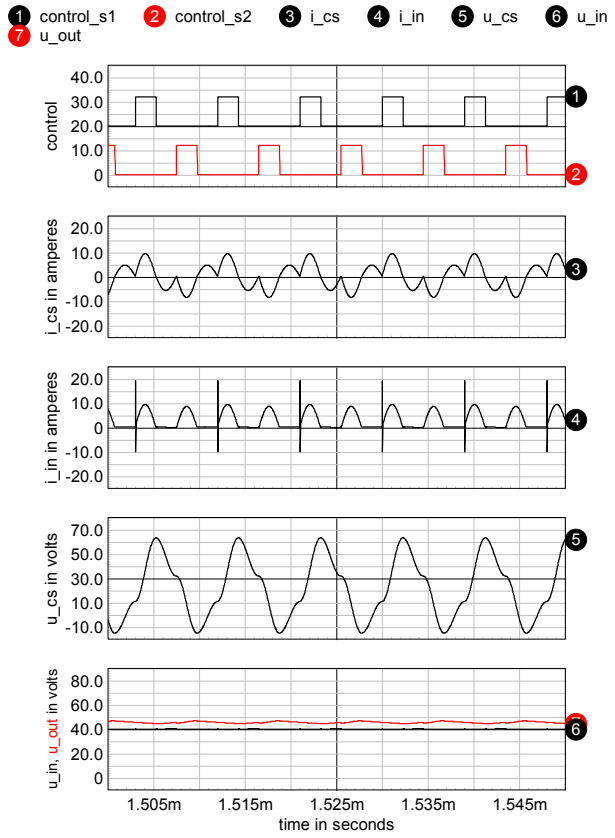

Fig.9. The steady state waveforms under the overload conditions. Special control by an increase of switching period. Soft switching operation. C_1=230nF, L_1=2uH, R_{out}=20Ω, P_{out}=103W, I_{Csrms}=5.2A, I_{Csmax}=9.4, I_{inrms}=4.55A, I_{S1rms}=4A, I_{S2rms}=3.5A, U_{Csmax}=63.1V, U_{Csmin}=-15.3V, U_{out}=45.3V, T_s=9.0us. ICAP/4 simulation results.

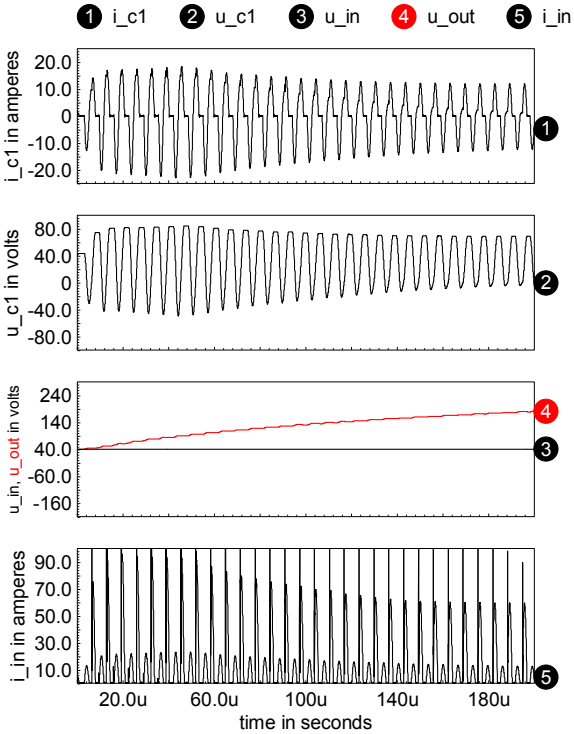

Fig.10. Waveforms during the start of the Mosfet-based five-cell SCVM. C_1=230nF, L_1=1.9uH, R_{out}=252Ω, T_s=.6.5us, dead-time=0.5us. ICAP/4 simulation results.

Multi-cell converter

In the multi-cell SCVM converter the majority of the problems will be similar to the single cell case. However some important differences can occurs during the overload:

- The more cells in SCVM that are implemented the bigger the difference between the input voltage (initial output voltage) and the rated output voltage. The start of the converter from the conditions where the output capacitor is discharged (U_{out}=U_{in}) (the charging process of the output capacitor) can be longer and more extensive. Furthermore, in the input current pulses of charging capacitor dominate. These pulses increase and have a very sharp rising slope when the charging process starts from nonzero and positive current conditions (Fig. 10).
- The current reverse during charging of the switched capacitor, presented in Fig. 6 (case 2), will occur when the voltage of the switched capacitor in the last cell (higher index) exceeds the output voltage. It can happen in a much bigger overload than in the case of a single cell converter.

In the multi-cell converter the special control, presented in Fig. 8, where the positive current of discharging switches is hard terminated, should be avoided. In such a case, in the multi-cell converter, the current of inductors is terminated by the discharging switch (even) of the next cell (closer to the output). Only the inductor in the last cell can be deenergized to the output, via the output diode, when the discharging switches are turned-off.

Experimental results

The experimental tests were carried out to confirm the operation of the converter in the ZCS conditions but also in the overload states. The results were achieved in the Mosfet-based the single-cell switched-capacitor DC-DC boost converter (Fig. 3) converter.

Fig.11 - Fig.13 present waveforms of the voltage on switched capacitor (u_{C1}) and its current (i_{C1}). The case presented in Fig. 11 demonstrates the ZCS conditions when the converter was not overloaded.

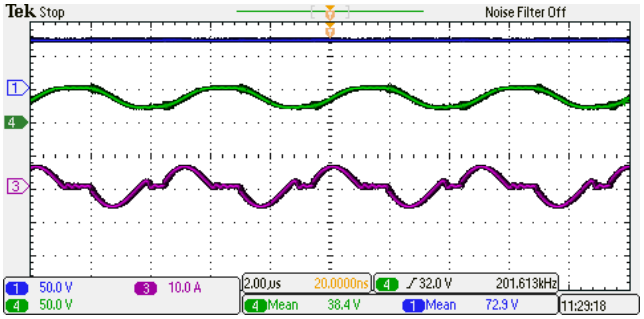

Fig.11. The steady state waveforms in the Mosfet-based SCVM under the ZCS conditions (underload). Experimental results of the single cell SCVM.

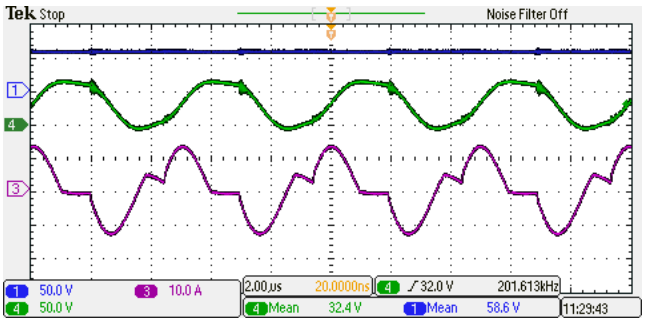

Fig. 12. The steady state waveforms in the Mosfet-based SCVM under the overload conditions. Experimental results of the single cell SCVM.

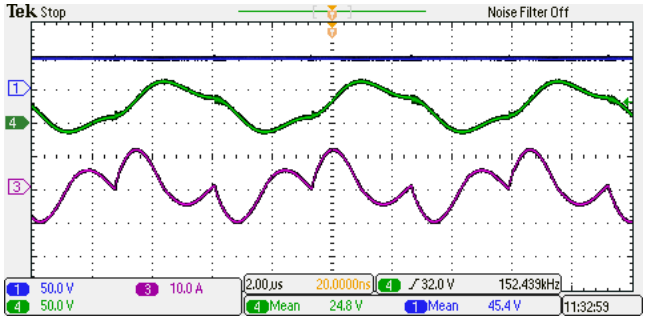

Fig.13. The steady state waveforms in the Mosfet-based SCVM under the overload conditions. Experimental results of the single cell SCVM.

The next results, presented in Fig. 12, regard the case when the converter is slightly overloaded. The voltage on switched capacitor becomes negative in the end of the discharging stage and its current does not stop crossing zero and flows in the opposite direction as in Fig. 6 case 6. Fig. 13 presents waveforms under the overload of the SCVM where the switching frequency was fairly low to observe the second oscillation of the current of the switched capacitor after its zero crossing. This is the case where all the stages of the overload operation is reached (Fig. 6).The experimental results presented in Fig. 11 – Fig. 13 confirm that the SCVM can operate under the overload but the operation differs from the rated case

Conclusions

The overload, in the meaning of too low load resistance may not be destructive but can cause a rise of temperature of devices due to hard switching mode. It also causes an increase in voltage on switched capacitor, a charge to the capacitor to negative value, a decrease in output voltage and the output power.

The overload can be managed by special controls that can reduce effect of hard switching or overload of the switched capacitor.

The overload can occur during the start of the converter as well as a consequence of too low resistance and then some of the proposed method can be used.

Very deep overload can cause the output voltage drop below the input voltage and shorting the source via the diode D_1 and D_{out}.

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REFERENCES

[1] Makowski M.S., Realizability conditions and bounds on synthesis of switched-capacitor DC-DC voltage multiplier circuits, *IEEE Trans. on Circuits and Systems I: Fundamental Theory and Applications,* 44 (1997), n.8, 684-691

[2] Dong Cao; Fang Zheng Peng, A family of zero current switching switched-capacitor dc-dc converters, Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE, 21-25 Feb. 2010, .1365,1372

[3] Yuanmao Ye; Cheng, K.W.E., A Family of Single-Stage Switched-Capacitor–Inductor PWM Converters, *IEEE Trans. on Power Electron.,* 28 (2013), n.11, 5196-5205

[4] Parastar A.; Seok Jul-Ki, High-Gain Resonant Switched-Capacitor Cell-Based DC/DC Converter for Offshore Wind Energy Systems, *IEEE Trans. on Power Electron.,* 30 (2015), n.2, 644-656

[5] Keiser O.; Steimer P.K.; Kolar J.W., High power resonant Switched-Capacitor step-down converter, Power Electron. Spec. Conf., PESC 2008,. 15-19 June 2008, 2772-2777
[6] Cervera A.; Evzelman M.; Peretz M.; Ben-Yaakov S., A High Efficiency Resonant Switched Capacitor Converter with Continuous Conversion Ratio, *IEEE Trans. on Power Electron.,* 30 (2015), n.3, 1373-1382
[7] Andersen R.L.; Lazzarin T.B.; Barbi I., A 1-kW Step-Up/Step-Down Switched-Capacitor AC–AC Converter, *IEEE Trans. on Power Electron.,* 28 (2013), n.7, 3329-3340
[8] Lazzarin T.B.; Andersen R.L.; Martins G.B.; Barbi I., A 600-W Switched-Capacitor AC–AC Converter for 220 V/110 V and 110 V/220 V Applications, *IEEE Trans. on Power Electron.*, 27 (2012), n.12, 4821-4826
[9] Beck Y., Singer S., Martinez-Salamero L., Modular Realization of Capacitive Converters Based on General Transposed Series–Parallel and Derived Topologies*, IEEE Trans. on Ind. Electron.*, 61 (2014), n.3, 1622-1631
[10] Kiratipongvoot S.; Siew-Chong Tan; Ioinovici A., Phase-Shift Interleaving Control of Variable-Phase Switched-Capacitor Converters, *Industrial Electronics, IEEE Trans. on Ind. Electron.*, 60 (2013), n.12, 5575-5584
[11] Surma P., Dobór wartości indukcyjności przekształtnika DC-DC o przełączanych kondensatorach, *Przegląd Elektrotechniczny* (2015), n.3, 190
[12] Kawa A.; Stala R.; Mondzik A.; Pirog S.; Penczek A., High Power Thyristor-Based DC-DC Switched-Capacitor Voltage Multipliers. Basic Concept And Novel Derived Topology with A Reduced Number of Switches., *IEEE Trans. on Power Electron.*, (2013), n.99, 1-1 (early access)
[13] Stala R; Pirog S.; Baszynski, M.; Mondzik A.; Penczek A.; Czekonski J.; Gasiorek S., Results of Investigation of Multicell Converters With Balancing Circuit—Part I, *IEEE Trans. On Ind. Electron.*, 56 (2009), 2610-2619
[14] Stala R; Pirog S.; Baszynski M.; Mondzik A.; Penczek A.; Czekonski J.; Gasiorek S., Results of Investigation of Multicell Converters With Balancing Circuit—Part II", *IEEE Trans. on Ind. Electron.,* 56 (2009), 2620-2628
[15] Stala R., The Switch-Mode Flying Capacitor DC/DC Converters With Improved Natural Balancing, *IEEE Trans. on Ind. Electron.*, 57 (2010), 1369-1382.