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# Surrogate-Based Multi-Objective Optimization of Compact Microwave Couplers

***Abstract**. This work presents a rigorous methodology for expedited simulation-driven multi-objective design of microwave couplers with compact footprints. The proposed approach is a viable alternative for computationally expensive population-based metaheuristics and exploits a surrogate-assisted point-by-point Pareto set determination scheme that utilizes—for the sake of computational efficiency—space-mapping-corrected equivalent circuit models. The technique is showcased using a complex design example of a compact rat-race coupler, for which a set of nine alternative design solutions is efficiently identified. The latter illustrate the best possible trade-offs between conflicting design objectives for the structure at hand, that is, operational bandwidth and layout area. The overall design cost corresponds to approximately twenty high-fidelity electromagnetic simulations of the miniaturized coupler.*

***Streszczenie**. W pracy zaprezentowano metodologię projektowania kompaktowych sprzęgaczy mikrofalowych w oparciu o efektywną numerycznie analizę wielokryterialną. Proponowane podejście stanowi atrakcyjną alternatywę dla populacyjnych metod metaheurustycznych i polega na wyznaczeniu poszczególnych rozwiązań Pareto-optymalnych poprzez jednokryterialną optymalizację z ograniczenami, wykorzystującą modele obwodowe i metodę odwzorowania przestrzeni. Przykładem zastosowania przedstawionej metody jest projekt zminiaturyzowanego sprzęgacza pierścieniowego, dla którego wyznaczono dziewięć konkurencyjnych rozwiązań układowych, przedstawiających kompromis pomiędzy sprzecznymi kryteriami projektowymi, tj. pasmem pracy i powierzchnią struktury. Całkowity koszt projektowania nie przekracza dwudziestu symulacji elektromagnetycznych zminiaturyzowanego sprzęgacza mikrofalowego. (**Wielokryterialna optymalizacja kompaktowych sprzęgaczy mikrofalowych przy użyciu metody modeli zastępczych**).*

**Index terms:** microwave circuit miniaturization, multi-objective optimization, simulation-driven design, surrogate-based optimization, space mapping.
**Słowa kluczowe:** miniaturyzacja układów mikrofalowych, optymalizacja wielokryterialna, symulacyjne metody projektowania, metoda modeli zastępczych, odwzorowanie przestrzeni.

## Introduction

Reliable design of compact microwave circuits for modern wireless communication systems is a challenging task that involves simultaneous adjustment of multiple designable parameters of the structure at hand to satisfy several, often conflicting, objectives such as size, bandwidth, phase response, etc. [1]. A common feature of such circuits, e.g., folded or fractal-shaped couplers [2], [3], is a high computational cost of their accurate electromagnetic (EM) analysis that results from geometric complexity of miniaturized layouts. This proves to be a fundamental issue for simulation-driven design of compact components, especially when using conventional design strategies, such as repetitive parameter sweeps or direct single-objective optimization, the latter requiring numerous EM simulations to obtain satisfactory results. On the other hand, alternative means of circuit analysis (e.g., exploiting transmission line theory) are grossly inaccurate and, for the most part, capable of merely providing initial design solutions. This is particularly the case for highly miniaturized microwave circuits with strongly coupled building blocks (e.g., [4]).

To some extent, these shortcomings can be alleviated by surrogate-based optimization (SBO) techniques, such as space mapping (SM), which have repeatedly demonstrated their computational superiority over commonly exploited direct optimization algorithms applied to design of conventional microwave circuits. SBO schemes benefit from low-cost surrogates that are well-aligned with the high-fidelity EM models through adaptive corrections [5]. Taking advantage of the fact that vast majority of numerical operations is executed at the level of the suitably enhanced low-fidelity models, whereas their high-fidelity counterpart is used exclusively for occasional design verification and the surrogate model update, the overall computational cost of the SBO process might be kept low.

As opposed to conventional microwave circuits, compact devices are typically developed using novel topologies, for which the relationship between the size of the structure and its electrical parameters cannot be established prior to design itself. This significantly increases the risk of design failure, especially when excessively stringent specifications are applied to the prototype circuit. To formally address this issue, multi-objective optimization is required; the process aims at finding a so-called Pareto set that represents the best possible trade-offs between non-commensurable objectives. The most popular solution approaches to this problem include the use of population-based metaheuristics, such as genetic algorithms [6], [7]. While capable of determining the entire Pareto set in one algorithm run, these methods are of limited use for design of compact circuits due to a large number of objective function evaluations involved in the process (typically tens of thousands [6]).

In this work, a procedure for rapid multi-objective design optimization of computationally demanding compact microwave couplers is provided. The proposed method is a surrogate-based optimization scheme that exploits an equivalent circuit model of the given structure, and space mapping as the fundamental tool of low-fidelity model correction to identify a discrete representation of the Pareto front which contains the trade-off solutions between the operational bandwidth and the layout area of the structure. The approach is demonstrated by a compact rat-race coupler design example.

## Case Study: Compact Rat-Race Coupler

In this section, we define a complex design problem of a compact rat-race coupler (RRC). It is used to demonstrate the application of the multi-objective optimization methodology presented in Section 3. An RRC is a popular microwave coupler that splits an input signal between the output ports with a 0°/180° phase shift or combines two input signals [2]. A conventional RRC is a ring-shaped structure that is composed of six 90°-sections of transmission lines (TLs), which makes it a suitable candidate for circuit miniaturization.

Let us consider a compact RRC shown in Fig. 1(a). Size reduction has been achieved here by replacing conventional TL sections with folded shunt-stub-based lines, whose parameterized layouts are given in Fig. 1(b). The coupler at hand can be sufficiently described by a vector of seven designable parameters $\boldsymbol{x} = [w\ d_1\ d_2\ l_1\ l_2\ l_3\ l_4]^T$. We choose a Taconic RF-35 dielectric substrate ($\varepsilon_r$ = 3.5, $h$ = 0.762 mm, tan$\delta$ = 0.0018) for circuit implementation. The operation frequency is set to $f_0$ = 1 GHz. For the above specifications, the width and the length of the coupler feeding lines are fixed to 1.7 and 15 millimeters, respectively.

The goal is to find a set of design solutions that represent the best possible trade-offs between the following objectives: $F_1$ – maximization of the operational bandwidth, where the bandwidth ($BW$) is defined as a symmetrical—with respect to the center frequency $f_0$—intersection of $|S_{11}|$ and $|S_{41}|$ that remain below the level of –20 dB, and $F_2$ – minimization of the layout area occupied by the coupler. An equal power division between the output ports at $f_0$ is not considered here as a separate design objective. Instead, it is ensured by means of a suitably defined penalty function included in $F_1$.

Surrogate-based optimization requires a fast low-fidelity model of a given structure that is also sufficiently aligned with its high-fidelity counterpart. Here, we use an equivalent circuit of Fig. 2 to serve this purpose. The high-fidelity model is implemented in CST Microwave studio [9] (~350,000 mesh cells, ~25 minute simulation time per design). The solution space is determined by the following lower/upper bounds: $\boldsymbol{l}$ = [0.2 0.1 0.1 10 10 0.1 0.1]$^T$ and $\boldsymbol{u}$ = [1.5 1.2 4 20 20 20 20]$^T$ (all dimensions in mm).

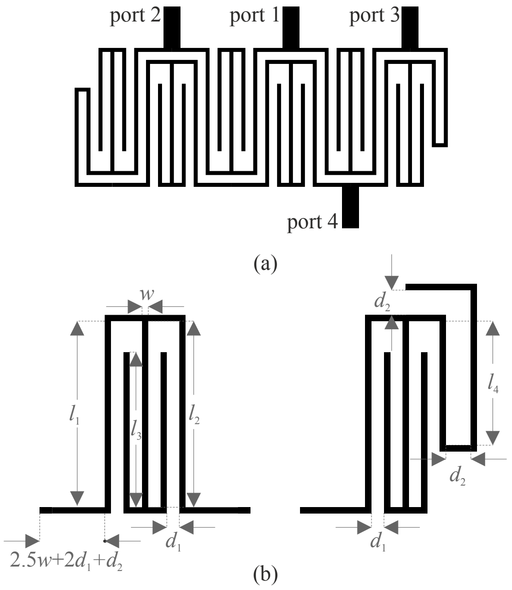



Fig. 1. (a) Layout of the example compact RRC [2]; (b) Parameterized layouts of shunt-stub-based TLs

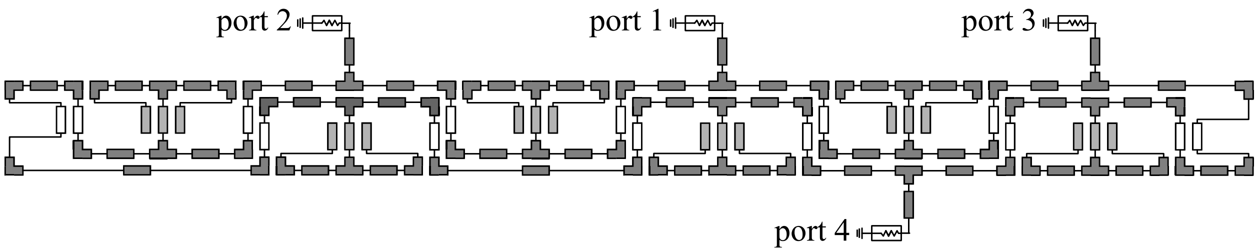



Fig. 2. Equivalent circuit model of the example compact RRC, implemented in Agilent ADS [8]. Highlighted components have different sets of implicit space mapping parameters $\boldsymbol{p}$ assigned to them (dark grey: $\varepsilon_1$, $h_1$; grey: $\varepsilon_2$, $h_2$, white: $\varepsilon_3$, $h_3$)

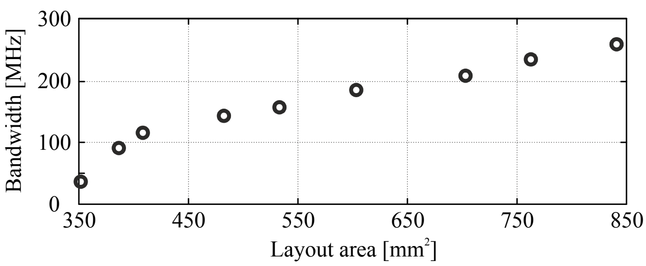



Fig. 3. Pareto-optimal set representing the best possible trade-offs between bandwidth and layout area of the compact RRC, acquired by means of the presented multi-objective optimization procedure

Although the methodology of Section 3 is demonstrated here using a compact RRC design example, it is also valid for other types of microwave circuits, provided that a sufficiently fast and accurate equivalent circuit model can be developed.

## Methodology

In this section, we formulate and discuss the methodology for computationally efficient multi-objective design optimization of compact microwave couplers.

### Problem Formulation

Let $\boldsymbol{R}_f(\boldsymbol{x})$ denote a response of a fine model of the structure under consideration, where $\boldsymbol{x}$ is a vector of its designable parameters. Typically, $\boldsymbol{R}_f(\boldsymbol{x})$ is obtained by a computationally expensive high-fidelity EM simulation, and represents complex $S$-parameters of the given design solution.

Let $F_k(\boldsymbol{R}_f(\boldsymbol{x}))$, where $k$ = 1, …, $N_{obj}$, be a $k$th design objective. Considering a class of compact microwave couplers, typical objectives include minimization of the layout area and maximization of the bandwidth, with a specified power division ratio at $f_0$.

The goal of a multi-objective scheme is to identify a representation of a so-called Pareto-optimal set $X_P$, which is composed of non-dominated designs such that for any $\boldsymbol{x} \in X_P$, there is no other design $\boldsymbol{y}$ for which the relation $\boldsymbol{y} \prec \boldsymbol{x}$ is satisfied. Design $\boldsymbol{y}$ dominates $\boldsymbol{x}$ ($\boldsymbol{y} \prec \boldsymbol{x}$) if $F_k(\boldsymbol{R}_f(\boldsymbol{y})) \le F_k(\boldsymbol{R}_f(\boldsymbol{x}))$ for all $k$ = 1, …, $N_{obj}$, and $F_k(\boldsymbol{R}_f(\boldsymbol{y})) < F_k(\boldsymbol{R}_f(\boldsymbol{x}))$ for at least one $k$) [10].

### Surrogate Model

The high-fidelity EM-simulated model of the structure under consideration is too expensive to be directly handled by any population-based metaheuristic algorithm, which typically requires tens of thousands objective function evaluations to converge [6], [9]. Thus, we exploit here a fast auxiliary equivalent circuit of Fig. 2 as the low-fidelity model $\boldsymbol{R}_c$ of the structure at hand. In order to increase the accuracy of $\boldsymbol{R}_c$, we apply implicit and frequency space mapping to construct a $\boldsymbol{R}_f$-well-aligned surrogate model $\boldsymbol{R}_s$, to be subsequently utilized in the optimization process. More specifically, the surrogate is defined as

$$\boldsymbol{R}_s(\boldsymbol{x}) = \boldsymbol{R}_{c.F}(\boldsymbol{x}; \boldsymbol{f}, \boldsymbol{p}) \tag{1}$$

where $\boldsymbol{R}_{c.F}$ is a frequency-scaled coarse model, whereas $\boldsymbol{f}$ and $\boldsymbol{p}$ denote frequency and implicit SM parameters, respectively. Let $\boldsymbol{R}_c(\boldsymbol{x}) = [R_c(\boldsymbol{x},\omega_1)\ R_c(\boldsymbol{x},\omega_2)\ \ldots\ R_c(\boldsymbol{x},\omega_m)]^T$, where $R_c(\boldsymbol{x},\omega_j)$ is evaluation of the circuit model at a frequency $\omega_j$. Then, $\boldsymbol{R}_{c.F}(\boldsymbol{x};\boldsymbol{f},\boldsymbol{p}) = [R_c(\boldsymbol{x},f_0 + \omega_1 \cdot f_1,\boldsymbol{p})\ \ldots\ R_c(\boldsymbol{x}, f_0 + \omega_m \cdot f_1,\boldsymbol{p})]^T$, with $f_0$ and $f_1$ being frequency scaling parameters. Here, the implicit SM parameters are $\boldsymbol{p} = [\varepsilon_1\ \varepsilon_1\ \varepsilon_1\ h_1\ h_2\ h_3]^T$ (substrate permittivity and thickness of equivalent circuit components). They are extracted to minimize misalignment between $\boldsymbol{R}_s$ and $\boldsymbol{R}_f$ as follows:

$$[\boldsymbol{f}^*, \boldsymbol{p}^*] = \arg\min_{\boldsymbol{f},\boldsymbol{p}} \| \boldsymbol{R}_f(\boldsymbol{x}) - \boldsymbol{R}_{c.F}(\boldsymbol{x}; \boldsymbol{f}, \boldsymbol{p}) \| \tag{2}$$

The improved accuracy of $\boldsymbol{R}_s$ is limited to the vicinity of the design $\boldsymbol{x}$, at which the implicit SM parameters have been extracted. Note that it is not possible to find a single set of SM parameters that would ensure surrogate model accuracy across the entire design space. As a consequence, in order to lead towards a satisfactory design, the surrogate has to be iteratively refined during the optimization process.

Optimization Procedure

For the sake of computationall efficiency, our design approach is based on a point-by-point identification of the Pareto set. First, we execute unconstrained optimization for $F_1$ objective only (here, bandwidth maximization). The optimum design $\boldsymbol{x}_p^{(1)}$ obtained this way is used to determine the feature space extreme point of the Pareto set as $(F_1(\boldsymbol{R}_f(\boldsymbol{x}_p^{(1)})); F_2(\boldsymbol{R}_f(\boldsymbol{x}_p^{(1)})))$.

In the subsequent steps, we set the threshold values for the second objective $F_2^{(j)}$, and optimize the structure w.r.t the first objective so that the above threshold value is preserved:

$$\boldsymbol{x}_p^{(j)} = \arg\min_{\boldsymbol{x},\, F_2(\boldsymbol{R}_f(\boldsymbol{x})) \le F_2^{(j)}} F_1\left(\boldsymbol{R}_f(\boldsymbol{x})\right) \tag{3}$$

Here, $\boldsymbol{x}_p^{(j)}$ is the $j$th design space element of the Pareto set. The process is continued until $F_1(\boldsymbol{R}_f(\boldsymbol{x}_p^{(j)}))$ is still satisfactory from the point of view of given design specifications.

The problem (3) is solved using the SM surrogate model (cf. Section 2.2) and it is itself realized as an iterative process

$$\boldsymbol{x}_p^{(j.k)} = \arg\min_{\boldsymbol{x},\, F_2(\boldsymbol{R}_s^{(j.k)}(\boldsymbol{x})) \le F_2^{(j)}} F_1\left(\boldsymbol{R}_s^{(j.k)}(\boldsymbol{x})\right) \tag{4}$$

where

$$\boldsymbol{R}_s^{(j.k)}(\boldsymbol{x}) = \boldsymbol{R}_{c.F}(\boldsymbol{x}; \boldsymbol{f}^{(j.k)}, \boldsymbol{p}^{(j.k)}) \tag{5}$$

and

$$[f^{(j.k)}, p^{(j.k)}] = \arg\min_{f,p} \| R_f(x^{(j.k)}) - R_{c.F}(x^{(j.k)}; f, p) \| \tag{6}$$

The starting point for the algorithm (4) is $\boldsymbol{x}_p^{(j-1)}$. Typically, two iterations of (4) are sufficient to obtain $\boldsymbol{x}_p^{(j)}$, which is because the starting point is already a good approximation of the optimum. In practice, the thresholds $F_2^{(j)}$ can be obtained as $F_2^{(j)} = \alpha \cdot F_2^{(j-1)}$ with $\alpha < 1$ (e.g., $\alpha = 0.95$), or $F_2^{(j)} = F_2^{(j-1)} - \beta$ with $\beta > 0$ (e.g., $\beta = 0.05 \cdot F_2^{(1)}$). Central-frequency equal power split between the output ports is secured by adding to $F_1$ in (4) the terms proportional to $(|S_{21}| + 3)^2$ and $(|S_{31}| + 3)^2$ (at $f_0$), which penalize the designs violating this requirement.

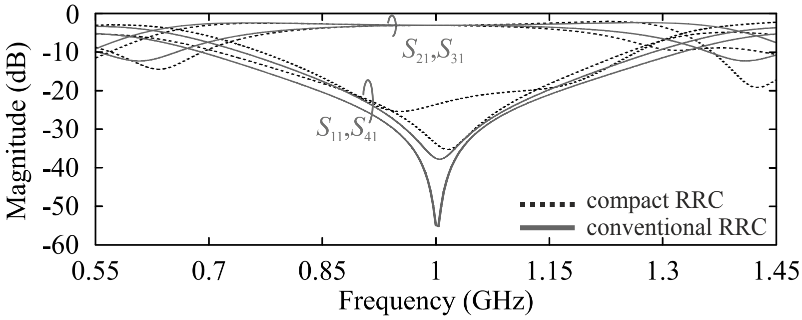
**Numerical Results**

The methodology of Section 3 is showcased here using a compact RRC design example described in detail in Section 2. The process (4) has been applied to identify nine Pareto-optimal design solutions, illustrating the trade-offs between bandwidth and the layout area of the structure under consideration. The first design, obtained without any area constraints, features $BW$ and the layout area of 258 MHz and 841 mm$^2$, respectively. Eight consecutive design solutions have been acquired by setting up $F_2^{(j)}$ to 800, 725, 650, 575, 500, 425, 400, and 375 mm$^2$, respectively. The last two threshold values have been set with higher resolution, after failing to obtain a positive value od $BW$ for the 350 mm$^2$ layout. Figure 3 shows the obtained representation of the Pareto-optimal set. Numerical results are listed in detail in Table I. One can observe that the scale of circuit miniaturization ranges from 86.4% to 94.3%, which corresponds to compact designs that offer broadest and narrowest bandwidths, respectively. Simulated characteristics of the selected design solutions are shown in Figures 4(a)–(c). The total cost of the design process corresponds to about twenty fine model evaluations, including the overhead related to multiple evaluations of the coarse model (the latter does not exceed 10 percent of the overall EM simulation cost). In comparison with any type of metaheuristic algorithm applied to direct optimization of the compact RRC fine model, the overall cost of the presented method is orders of magnitude lower.

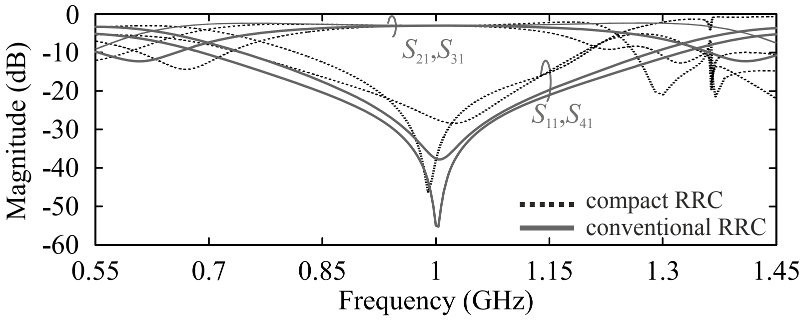
Table 1. Numerical Results of Multi-Objective Optimization of Compact RRC

| Designable parameters [mm] | | | | | | | Design objectives | | Miniaturization* [%] |
|---|---|---|---|---|---|---|---|---|---|
| $w$ | $d_1$ | $d_2$ | $l_1$ | $l_2$ | $l_3$ | $l_4$ | $BW$ [MHz] | Area [mm$^2$] | |
| 0.61 | 0.3 | 2.90 | 13.16 | 13.16 | 1.55 | 0.83 | 258 | 841 | 86.4 |
| 0.55 | 0.3 | 2.60 | 13.50 | 13.50 | 3.85 | 1.71 | 232 | 763 | 87.7 |
| 0.50 | 0.27 | 2.07 | 15.44 | 15.44 | 6.11 | 3.03 | 208 | 703 | 88.6 |
| 0.45 | 0.2 | 2.07 | 14.52 | 14.52 | 9.09 | 2.87 | 184 | 604 | 90.2 |
| 0.39 | 0.2 | 1.93 | 14.23 | 14.23 | 12.57 | 3.09 | 156 | 534 | 91.4 |
| 0.37 | 0.17 | 1.71 | 14.51 | 14.51 | 14.36 | 8.11 | 143 | 483 | 92.2 |
| 0.35 | 0.15 | 1.26 | 15.00 | 15.00 | 14.85 | 6.21 | 114 | 409 | 93.4 |
| 0.31 | 0.15 | 1.20 | 15.53 | 15.53 | 15.37 | 5.78 | 90 | 387 | 93.7 |
| 0.28 | 0.15 | 1.07 | 15.71 | 15.71 | 15.55 | 6.02 | 36 | 353 | 94.3 |

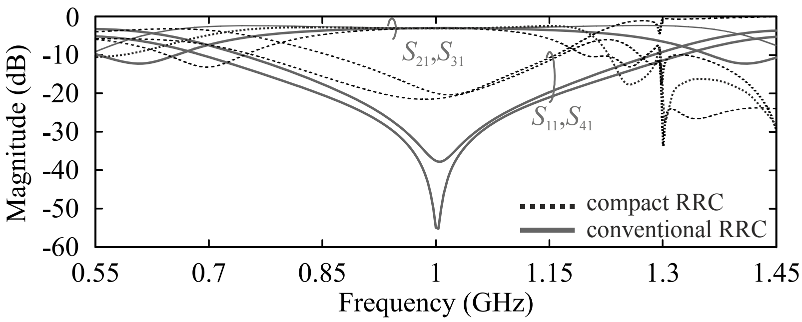
* - w.r.t. conventional RRC designed for $f_0$ = 1 GHz and the same substrate: radius = 44.39 mm, size = 6190 mm$^2$.




(a)




(b)




(c)

Fig. 4. S-parameters for selected design solutions with layout areas of: (a) 841 mm$^2$, (b) 534 mm$^2$, and (c) 353 mm$^2$. Characteristics of a conventional RRC have been added for comparison purposes

**Conclusions**

This work presents a technique for rapid multi-objective optimization of compact microwave couplers. The main components of the method include an iterative identification of the Pareto-optimal set, using a contrained single-objective SBO scheme with the space-mapping-corrected equivalent circuit model as the underlying surrogate model. Computational efficiency of the presented method is illutrated using a complex design example of a compact RRC. The obtained Pareto set demonstrates trade-offs between conflicing design objective, here, bandwidth and layout area.

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