Orapin CHANNUMSIN[1], Worapong TANGSRIRAT[2]

Rajamangala University of Technology Isan, Khon Kaen Campus (1), King Mongkut's Institute of Technology Ladkrabang (2)

doi:10.15199/48.2017.03.55

VDIBA-based sinusoidal quadrature oscillator

***Abstract**. An electronically tunable voltage-mode sinusoidal quadrature oscillator circuit, which is based on using the recently introduced active building block, namely voltage differencing inverting voltage buffered amplifier (VDIBA) has been presented. The presented quadrature oscillator uses two VDIBAs, one electronic grounded resistor, and two grounded passive capacitors, suitable for MOS-C realization. The circuit performs an single-element-controlled oscillator and provides the advantage features of independent electronic control of oscillation condition and oscillation frequency. The workability of the proposed circuit has been verified using PSPICE simulations based on VDIBA implemented in TSMC 0.25-μm CMOS technology, and the simulated results demonstrate a sufficient agreement with the theoretical conclusions.*

Streszczenie.** Zaprezentowano elektronicznie strojony sinusoidalny kwadraturowy generator wykorzystujący voltage differenting inverting buffered amplifier VDIBA.Generator wykorzystuje dwa układy VDIBA, jeden uziemiony rezystor i dwa uziemione kondensatory. **Sinusoidalny kwadraturowy generator wykorzystujący układy VDIBA

Keywords: Voltage Differencing Inverting Buffered Amplifier (VDIBA), quadrature oscillator, MOSFET-C realization, voltage-mode circuits.
Słowa kluczowe: generator sinusoidalny, układy VDIBA

Introduction

Sinusoidal quadrature oscillators with a number of 90° phase-shifted outputs find numerous applications in communication, control and instrumentation systems. As a result, a number of voltage-mode quadrature oscillator circuits have been reported in the technical literature using different active building blocks such as second-generation current conveyors [1], differential voltage current conveyors [2], current differencing buffered amplifiers [3-6], and current follower transconductance amplifier [7]. However, all of them make use of at least three external passive components. Some of them [1–5, 7] still employ floating passive components, which is not convenient for integration. The oscillator realizations in [1-5] also do not provide any inherent electronic control to the circuit parameters. In addition, the works in [1-2] use more than two active elements, while the work in [7] contains two kinds of active elements for its construction.

In [8], the new ideas of modern electronic active building blocks have been reviewed. A recent introduction to the list of versatile active building blocks is voltage differencing inverting buffered amplifier (VDIBA), which has been found as a useful circuit element in designing analogue signal processing circuits [9-12].

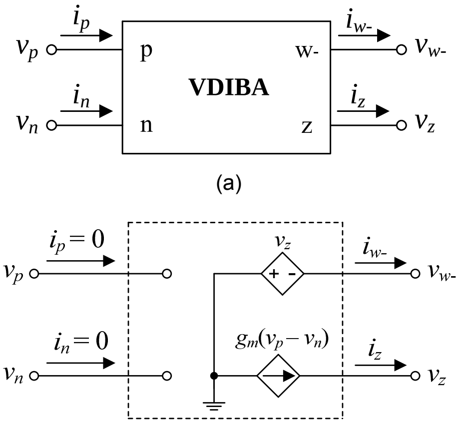
In this paper, an electronically tunable resistorless realization of the voltage-mode sinusoidal quadrature oscillator is described. The oscillator circuit employs only two VDIBAs, one voltage-controlled elelctronic resistor and two grounded capacitors, which can be further made fully integrated based on MOS-C realization. It also generates two sinusoidal output voltages with 90° phase shift, and exhibits an independent electronic control of the oscillation condition and the frequency of oscillation. The PSPICE simulation results using TSMC 0.25-μm CMOS process parameters have been provided to evauate the circuit performance.

Circuit description

Ideally, the symbolic representation and the behaviour model of the VDIBA are shown in Fig.1, where p and n are the input terminals and z and w- are the output terminals. It has been shown that the VDIBA device has two high-impedance voltage inputs v_p and v_n, a high-impedance current output i_z and a low-impedance inverting voltage output v_{w-}. Its voltage-current characteristics can be described by the following hybrid matrix :

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_{w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_{w-} \end{bmatrix} \tag{1}$$

where g_m is the transconductance gain of the VDIBA, which is normally controllable by electronic means.



(a)

(b)

Fig.1. The VDIBA
(a) schematic symbol (b) equivalent circuit.

The simple CMOS realization of the VDIBA is shown in Fig.2 [10]. The circuit consists of a differential pair with active loaded (M_1-M_4) and a unity-gain inverting voltage amplifier (M_5-M_6). In this configuration, the transconductance g_m of the VDIBA is controlled by the external DC biasing current I_B, and given by :

$$g_m = \sqrt{\mu C_{ox} \frac{W}{L} I_B} \tag{2}$$

where μ is the effective channel mobility, C_{ox} is the gate-oxide capacitance per unit area, W and L are channel width and length of the MOS transistor, respectively.

Fig.3(a) shows the circuit diagram of the proposed sinusoidal quadrature oscillator, which is based on the use of two VDIBAs, one electronic grounded resistor (M_{R1} and M_{R2}) and two grounded capacitors (C_1 and C_2). In Fig.3(a), it is interesting to note that the parallel connection of two NMOS transistors (M_{R1} and M_{R2}) operated in the triode region as shown in Fig.3(b) are used to realize the grounded electronic resistor (R_M) [13]. Its equivalent resistance can be given by :

$$R_M = \frac{1}{\mu C_{ox}\frac{W}{L}(V_C - 2V_T)} \tag{3}$$

where V_T is the threshold volatge of the NMOS transistor. The above relation reveals that the R_M-value is controllable electronically by adjusting the DC control voltages V_C.

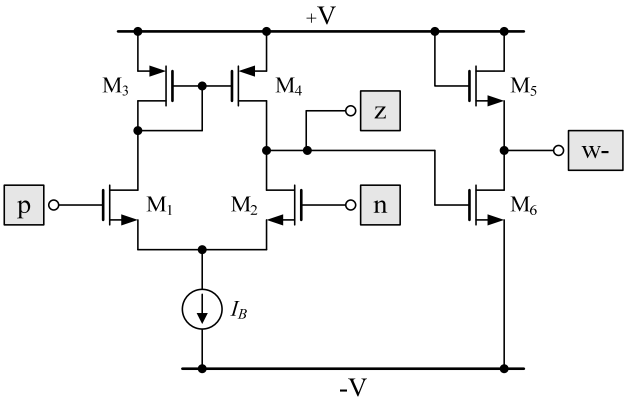
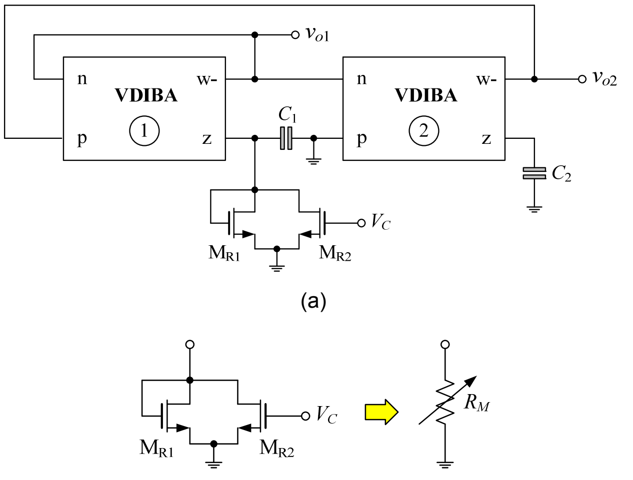


Fig.2. CMOS implementation of the VDIBA.



(a)

(b)

Fig.3. Proposed VDIBA-based sinusoidal quadrature oscillator. (a) schematic diagram (b) electronic grounded resistor using two MOS transistors.

Considering the proposed oscillator circuit of Fig.3(a), its routine analysis yields the following characteristic equation :

$$s^2 + \frac{s}{C_1}\left(\frac{1}{R_M} - g_{m1}\right) + \frac{g_{m1}g_{m2}}{C_1C_2} = 0 \tag{4}$$

where g_{mi} refers to the transconductance gain g_m of the i-th VDIBA (i = 1, 2).

From eq.(4), the oscillation condition and the frequency of oscillation (ω_o) can also be obtained as:

$$\frac{1}{R_M} = g_{m1} \tag{5}$$

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{6}$$

Eq.(5) shows that the oscillation condition can be controlled independently by tuning R_M. Since the value of R_M depends on the control voltage V_C, the oscillation condition is electronically controllable. On the other hand, the ω_o from eq.(6) is also electronically adjusted through the g_{m2}-value without affecting the condition of oscillation.

From Fig. 3(a), the relationship between two quadrature output voltages v_{o1} and v_{o2} can be expressed as:

$$\frac{v_{o2}}{v_{o1}} = \frac{g_{m2}}{sC_2} \tag{7}$$

which is represented that the phase difference between v_{o1} and v_{o2} is equl to 90°. Thus, the output voltages v_{o1} and v_{o2} are to be quadrature signals.

Tracking error analysis and sensitivity performance

Taking into account the non-ideal VDIBA, the hybrid matrix relationship given in Eq.(1) turns to :

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_{w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & -\beta & 0 \end{bmatrix} \cdot \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_{w-} \end{bmatrix} \tag{8}$$

where β is the non-ideal voltage gain of the VDIBA. Here, $\beta = 1 - \varepsilon_v$ and ε_v is the voltage tracking error. Re-analysis the proposed quadrature oscillator of Fig.3 using eq.(8), the characteristic equation is modified as :

$$s^2 + \frac{s}{C_1}\left[\frac{1}{R_M} - \beta_1 g_{m1}\right] + \left(\frac{\beta_1\beta_2 g_{m1}g_{m2}}{C_1C_2}\right) = 0 \tag{9}$$

In this case, the oscillation condition and the frequency of oscillation can be calculated as:

$$\frac{1}{R_M} = \beta_1 g_{m1} \tag{10}$$

$$\omega_o = \sqrt{\frac{\beta_1\beta_2 g_{m1}g_{m2}}{C_1C_2}} \tag{11}$$

From eq.(11), the sensitivity of ω_o with respect to its active and passive components can be evaluated as :

$$S_{\beta_1}^{\omega_o} = S_{\beta_2}^{\omega_o} = S_{g_{m2}}^{\omega_o} = S_{g_{m2}}^{\omega_o} = \frac{1}{2} \tag{12}$$

$$S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2} \tag{13}$$

All of which are equal to 0.5 in magnitude.

Parasitic element effects

In this section, the effect of VDIBA parasitic elements on the oscillator performance is investigated. The practical model of the VDIBA including its terminal parasitic impedances is shown in Fig.4. It has been shown that the practical VDIBA has high input impedances at ports p, n and z ($R_p//C_p$, $R_n//C_n$ and $R_z//C_z$) and a low-value parasitic serial resistance at port w- (R_w), respectively. Because the terminal z of the VDIBA-1 in the proposed circuit of Fig.3(a) is connected in parallel with an electronic grounded resistor R_M, the influence of the parasitic resistance R_{z1} can be merged. It is further noted that the proposed oscillator circuit employs external capacitors C_1 and C_2 parallel connecting at the terminals z_1 and z_2, respectively. As a result, the effects of the parasitic capacitances C_{z1} and C_{z2} can then be absorbed, owing to the fact that $C_1 >> C_{z1}$ and $C_2 >> C_z$). Therefore, the useful frequency range of the proposed oscillator in Fig.3(a) can be defined as the following region.

(14)
$$\frac{1}{R_{z2}C_2} << \omega << \frac{1}{R_M C_1}$$

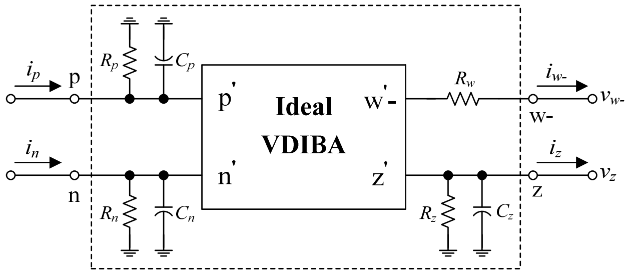


Fig.4. Practical model of the VDIBA including its parasitic impedances.

Circuit performance evaluation

The performance of the proposed quadrature sinusoidal oscillator circuit in Fig. 3(a) is evaluated through PSPICE simulation. In simulations, the CMOS VDIBA structure given in Fig.2 has been performed with TSMC 0.25-μm CMOS process parameters (threshold voltage V_{TH} = 0.4238 V, low field mobility U_0 = 425.646 cm^2/Vs, and gate oxide thickness T_{ox} = 5.714 nm for NMOS transistor, and V_{TH} = -0.5536 V, U_0 = 250 cm^2/Vs, and T_{ox} = 5.714 nm for PMOS transistor). The transistor aspect ratios were chosen as: (W/L) M_1-M_2, = 2.5μm/0.25μm, (W/L) M_3-M_4 = 5μm/0.25μm, (W/L) M_5-M_6 = 75μm/0.25μm, and (W/L) M_{R1}-M_{R2} = 2.5μm/0.25μm. The DC supply voltages were selected as: +V = -V = 0.75 V.

To demonstrate the workability of the proposed VDIBA-based quadrature oscillator circuit in Fig.3(a), the following circuit component values were chosen as : $I_B = I_{B1} = I_{B2}$ = 25 μA, V_c = 0.9 V, and $C_1 = C_2$ = 22 pF, resulting in $g_m = g_{m1} = g_{m2} \cong$ 190 μA/V, R_M = 5.3 kΩ and $f_o = \omega_o/2\pi \cong$ 1.37 MHz, respectively. The simulated transient responses for the sinusoidal output signals v_{o1} and v_{o2} of the proposed oscillator circuit of Fig.3(a) are depicted in Fig. 5, where the simulated f_o was found to be approximated as : $f_o \cong$ 1.34 MHz. Fig.6 also shows the simulated frequency spectrums for both outputs, giving the total harmonic distortion (THD) equal to 0.43%. It can be observed that the simulation results are in great agreement with the theoretical predictions. The total power consumption of the proposed circuit in Fig.3(a) was mentioned to be approximately 9.3 mW.

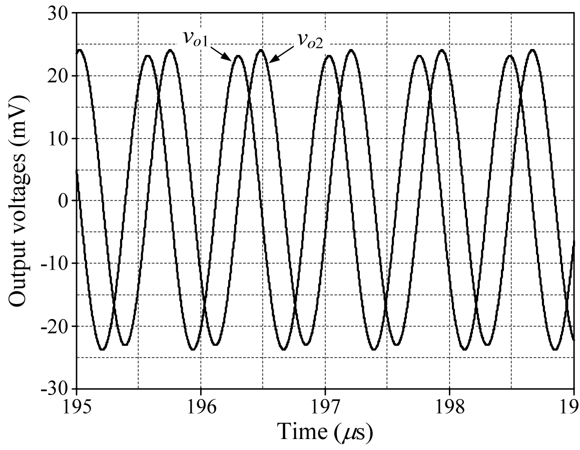


Fig.5. Simulated output waveforms for v_{o1} and v_{o2} of the proposed oscillator circuit in Fig.3(a).

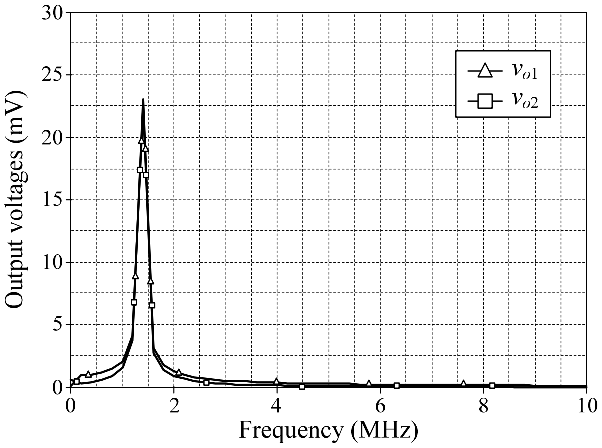


Fig.6. Simulated frequency spectrums for v_{o1} and v_{o2} of the proposed oscillator circuit in Fig.3(a).

Furthermore, the variations of the oscillation frequency f_o as a function of the bias currents I_B compared with the predicted theory are illustrated in Fig.7. The result is obtained by setting $I_B = I_{B1} = I_{B2}$ ($g_m = g_{m1} = g_{m2}$) and $C_1 = C_2$. As can be observed, the difference between the theory and the simulated plots especially in high bias current value region is mainly attributed to the deviation of the value of g_m that differs from the calculation ones.

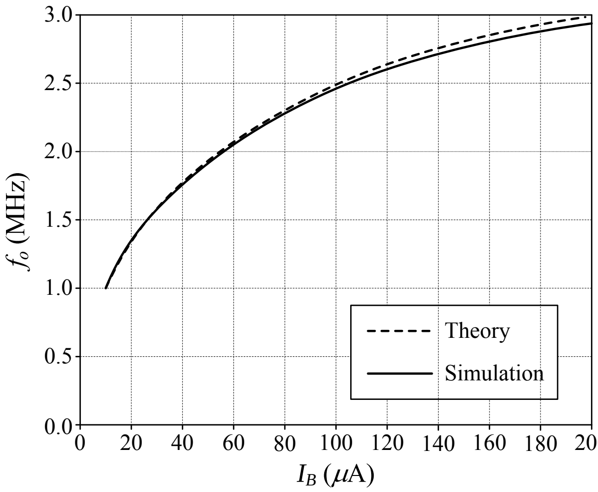


Fig.7. Variations of the oscillation frequency (f_o) with the controlled bias currents I_B.

Conclusions

This paper describes a volatge-mode sinusoidal quadrature oscillator employing two VDIBAs, one electronic resistor and two grounded capacitors, suitable for MOSFET-C realization. The proposed oscillator circuit provides simultaneously two quadrature sinusoidal output waveforms of 90^o phase shift, and can be used as a single-element-controlled variable frequency sinusoidal oscillator. PSPICE simulation results by TSMC 0.25-μm CMOS process parameters are provided to validate the theoretical analysis.

Acknowledgements

This work was supported by Faculty of Engineering, Rajamangala University of Technology Isan, Khon Kaen Campus. The support in part by Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL) is also gratefully acknowledged.

***Authors**: Dr. Orapin CHANNUMSIN, Faculty of Engineering, Rajamangala University of Technology Isan, Khon Kaen Campus, Khon Kaen 40000, Thailand, E-mail: pinmut@hotmail.com;*

Assoc. Prof. Dr. Worapong TANGSRIRAT, Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Ladkrabang, Bangkok 10520, Thailand,
E-mail : worapong.ta@kmitl.ac.th

The correspondence address is: Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Ladkrabang, Bangkok 10520, Thailand.
e-mail: worapong.ta@kmitl.ac.th

REFERENCES

[1] N. Minhaj, Current conveyor-based voltage-mode two-phase and four-phase quadrature oscillator, *Int. J. Electron*., 94 (2007), No.6-8, 663-669.

[2] S. Maheshwariang, J. Mohan, D. S. Chauhan, High input impedance voltage-mode universal filter and quadrature oscillator, *J. Circuits Syst. Comput*., 19 (2010), No.7, 1597-1607.

[3] W. Tangsrirat, S. Pisitchalermpong, CDBA-based quadrature sinusoidal oscillator, *Frequenz*, 61 (2007), No.3-4, 102-104.

[4] W. Tangsrirat, T. Pukkalanun, W. Surakampontorn, CDBA-based universal biquad filter and quadrature oscillator, *Active Passive Electron. Comp*., vol.2008, Article ID 24717, 6 pages, doi : 10.1155/2008/247171, 2008.

[5] W. Tangsrirat, D. Prasertsom, T. Piyatat, W. Surakampontorn, Single-resistance-controlled quadrature oscillator using current differencing buffered amplifiers, *Int. J. Electron*., 95 (2008), No.11, 1119-1126.

[6] F. Khateb, W. Jaikla, D. Kubanek, N. Khatib, Electronically tunable voltage-output quadrature oscillator based on high performance CCCDBA, *Analog Integr. Circ. Sig. Process*., 74 (2013), 499-505.

[7] N. Herencsar, K. Vrba, J. Koton, A. Lahiri, Realisations of single-resistance-controlled quadrature oscillator using a generalized current follower transconductance amplifier and a unity-gain voltage-follower, *Int. J. Electron*., 97 (2010), No.8, 897-906.

[8] D. Biolek, R. Senani, V. Biolkova, Z. Kolka, Active elements for analog signal processing: classification, review, and new proposals, *Radioengineering*, 17 (2008), 15-32.

[9] R. Sotner, J. Jerabek, N. Herencsar, Voltage differencing buffered/inverted amplifiers and their applications for signal generation, *Radioengineering*, 22 (2013), No.2, 490-504.

[10] N. Herencsar, S. Minaei, J. Koton, E. Yuce, K. Vrba, New resistorless and electronically tunable realization of dual-output VM all-pass filter using VDIBA, *Analog Integr. Circ. Signal Process.*, 74 (2013), No.1, 141-154.

[11] N. Herencsar,O. Cicekoglu, R. Sotner, J. Koton, K. Vrba, New resistorless tunable voltage-mode universal filter using single VDIBA, *Analog Integr. Circ. Signal Process.*, 76 (20130, 251-260.

[12] K. L. Pushkar, D. R. Bhaskar, D. Prasad, Voltage-mode new universal biquad filter configuration using a single VDIBA, *Circuits Syst. Signal Process*., 33 (2014), No.1, 275-285.

[13] I. S. Han and S. B. Park, Voltage-controlled linear resistor by two MOS transistors and its application to active RC filter MOS integration, *Proceedings of the IEEE*, 72 (1984), No.11, 1655-1657.