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doi:10.15199/48.2017.03.63

Single-ended to differential converters based on operational amplifiers: Performance analysis and design tips

***Abstract**. The paper presents a detailed analysis of the properties of selected single-ended to differential converters based on voltage-feedback operational amplifiers. The key issues discussed in the work are: the identification of the equivalent circuit model, definition of the model parameters, effect of resistor tolerances and operational amplifier's parameters on circuit accuracy, frequency response analysis, conclusions regarding the possibility of adjustment. The obtained results allow for a simple selection of converters with respect to their DC and AC performance.*

***Streszczenie.** Artykuł prezentuje analizę działania wybranych układów symetryzatorów napięcia zrealizowanych w oparciu o napięciowe wzmacniacze operacyjne. W pracy poruszono szereg zagadnień, takich jak identyfikacja modelu układu i jego parametrów, wpływ tolerancji rezystorów i parametrów wzmacniaczy operacyjnych na dokładność przetwarzania, analiza częstotliwościowa, możliwość strojenia. Uzyskane wyniki pozwalają na wybór najkorzystniejszego rozwiązania symetryzatora przy uwzględnieniu jego parametrów stało- i zmiennoprądowych. (**Symetryzatory napięcia zrealizowane na wzmacniaczach operacyjnych: Analiza działania i wskazówki projektowe**).*

Keywords: single-ended to differential converter, operational amplifier, signal conditioning, analog-to-digital converters.
Słowa kluczowe: symetryzator napięcia, wzmacniacz operacyjny, kondycjonowanie sygnałów, przetworniki analogowo-cyfrowe.

Introduction

Differential signalling has been used with great success in many areas of electronics, such as data transmission (e.g. RS-422, RS-485 standard), professional audio devices, standard twisted-pair analog telephone communication and measurement systems. Of all the potential benefits, the ability to reject common-mode noise and interference is its greatest asset. Two other advantages of the technique are reduced even-order harmonics and increased dynamic range [1, 2, 3].

Most modern high-resolution, high-accuracy ADCs have differential inputs. Even though this type of ADC accepts single-ended input signals, optimum performance is achieved when the input signal is differential [4]. There are a few strategies for driving these converters from single-ended sources [4, 5]. The first method is based on transformer coupling. This approach has several disadvantages. Transformers block the DC signal component, and they are expensive and large. Moreover, very often an additional buffer must be used to convert the low impedance of the transformer to the form that is required by the other stages of a circuit. Due to the scope of the paper, this approach is not analysed here.

In addition to the mentioned applications, single-ended to differential converters can also be used to test instrumentation amplifiers. To test and measure the DC and AC performance of instrumental amplifiers, the converter can work as a precise voltage source, that produce the voltage with a predefined differential and common-mode voltage component.

Nowadays, discrete operational amplifiers are essential signal conditioning elements in data acquisition systems. For this reason, very often single-ended to differential converters are built using discrete, voltage-feedback operational amplifiers. These amplifiers provide a simple way to perform many important functions including signal level conversion, amplitude scaling, buffering, reference voltage adjustment and filtering. Additional advantages arise from their low cost, small size and weight, and wide bandwidth from DC up to hundreds of MHz [6].

Single-ended to differential converters can also be built using integrated fully differential amplifiers (FDA) [7, 8]. These amplifiers are similar in a nodal architecture to standard voltage-feedback operational amplifiers, except for the fact that the fully differential amplifiers have differential outputs. The output common-mode voltage can be controlled independent of the differential voltage by applying a voltage to the input pin, usually called a V_{ocm}. This property allows single-ended to differential converters to be easily built. Typically, integrated FDAs are designed and optimised for driving high-speed ADCs. These devices provide high bandwidth (up to 2 GHz), low noise and distortions and a very high dynamic range. Their disadvantages are a worse DC performance and high cost (compared with the solutions based on voltage-feedback operational amplifiers).

This article is intended to complement the previous work of the authors [9] by considering a new structure of a converter and by addressing new topics, such as the influence of the amplifier parameters on circuit accuracy.

The main aim of this paper is to give an overview of the circuit solutions of single-ended to differential converters based on voltage-feedback operational amplifiers. In order to derive practically useful results, various properties, including the effect of resistor tolerances on circuit accuracy and the influence of operational amplifier parameters on DC and AC performance were studied.

Basic model

A functional diagram of the ideal single-ended to differential converter is shown in Fig. 1.

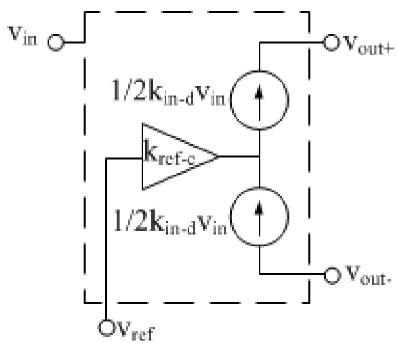

Fig. 1. A functional diagram of a single-ended to differential converter.

The circuit has two inputs, v_{in} and v_{ref}, and two outputs, v_{out+} and v_{out-}. A single-ended signal source drives the v_{in} input. The v_{ref} input allows the output common-mode voltage to be set to the required value (e.g. to match the input range of the ADC).

Voltage definitions

Common-mode voltage refers to the average value of two node voltages with respect to the ground reference. Thus, the output common-mode voltage is defined as

$$v_{out,cm} = \frac{v_{out+} + v_{out-}}{2} \quad (1)$$

Differential voltage is defined as the difference between the two node voltages. The output differential-mode voltage is given by the equation

$$v_{out,dm} = v_{out+} - v_{out-} \quad (2)$$

where v_{out+} and v_{out-} refer to the voltages at the output nodes (with respect to a ground reference).

Gains definitions

The ideal single-ended to differential converter is characterised by two gains, which are defined as follows

$$k_{in-d} = \frac{v_{out,dm}}{v_{in}} \qquad k_{ref-c} = \frac{v_{out,cm}}{v_{ref}} \quad (3)$$

As a result of the asymmetry of the signal paths, the input signal can generate a common- mode component and the reference signal can generate a differential output component. These effects can be characterised by two additional gains:

$$k_{in-c} = \frac{v_{out,cm}}{v_{in}} \qquad k_{ref-d} = \frac{v_{out,dm}}{v_{ref}} \quad (4)$$

Basic relationships

According to Fig. 1, the output voltages, v_{out+} and v_{out-}, are given by equations

$$v_{out+} = k_{ref-c} v_{ref} + \tfrac{1}{2} k_{in-d} v_{in} \quad (5)$$

$$v_{out-} = k_{ref-c} v_{ref} - \tfrac{1}{2} k_{in-d} v_{in} \quad (6)$$

Since

$$v_{out,dm} = v_{out+} - v_{out-} = k_{in-d} v_{in} \quad (7)$$

$$v_{out,cm} = \frac{v_{out+} + v_{out-}}{2} = k_{ref-c} v_{ref} \quad (8)$$

The voltage gain k_{in-d} relates the differential-mode output signal and the single-ended input signal. Usually it is a design parameter that can be adjusted by selecting the proper values of the resistors. The voltage gain k_{ref-c} relates $v_{out,cm}$ and v_{ref} , and, in most cases, is equal to 1.

Circuit description

Assuming that the circuit is linear, we can describe a single-ended to differential converter by using the following matrix representation [10, 11]:

$$\begin{bmatrix} v_{out,dm} \\ v_{out,cm} \end{bmatrix} = \begin{bmatrix} k_{in-d} & k_{ref-d} \\ k_{in-c} & k_{ref-c} \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ v_{ref} \end{bmatrix} \quad (9)$$

In the case of an ideal circuit, the values of k_{ref-d} and k_{in-c} are equal to zero, which leads to (7) and (8). However, due to many factors including the tolerance of the resistors as well as the DC and AC imperfections of operational amplifiers, the values of the voltage gains k_{ref-d} and k_{in-c} differ from zero. Based on the voltage gains given by (3) and (4), it is possible to define additional parameters that describe the quality of the converter.

The OBE (Output Balance Error) parameter is defined as the ratio of the output common-mode voltage produced by a ground referenced single-ended input signal to the output differential-mode voltage produced by the same input signal [12, 13]

$$OBE = \frac{\Delta v_{out,cm}}{\Delta v_{out,dm}} \quad (10)$$

In a logarithmic scale, OBE is expressed as

$$OBE = 20\log\left(\frac{\Delta v_{out,cm}}{\Delta v_{out,dm}}\right) \quad [dB] \quad (11)$$

The OBE is a very important quality metric for a single-ended to differential converter. The value depends on two components – amplitude balance and phase balance. The first one is a measure of how closely the two outputs are matched in the amplitude (in an ideal case they are exactly matched). The output phase balance is the measure of how close the phase difference between the two outputs, v_{out+} and v_{out-}, is to 180°. Thus, the presence of an imbalance in the output amplitude or phase produces an undesirable common-mode component at the output. By simple manipulations, the (10) can be rewritten as

$$OBE = \frac{k_{in-c}}{k_{in-d}} \quad (12)$$

The second parameter, CME (Common-Mode Error), is defined as the ratio of the output differential-mode voltage produced by the v_{ref} signal to the same output voltage but produced by the v_{in} signal [9]. In terms of voltage gains, the CME can be expressed as

$$CME = \frac{k_{ref-d}}{k_{in-d}} \quad (13)$$

Analysed circuits

Fig. 2 shows four implementations of the single-ended to differential converters built with voltage-feedback operational amplifiers. The presented circuits can be found in [4, 5, 6, 9, 14, 15, 16].

DC analysis

In this section, the DC gain error, which results from the mismatch of resistors and the finite value of the CMRR parameter, is studied.

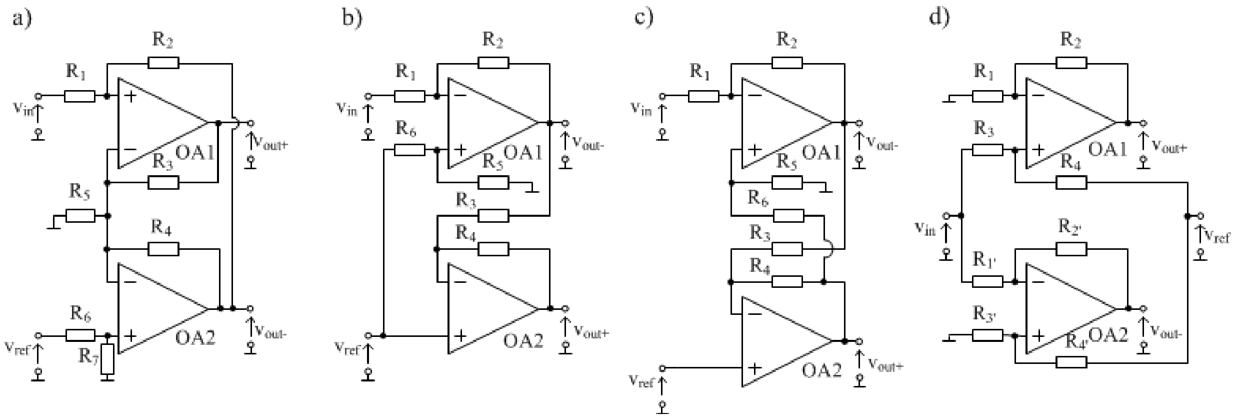

Fig. 2. Op-amp based implementations of single-ended to differential converters

The impact of mismatched resistors

Let us consider the single-ended to differential converter shown in Fig. 2a. Assuming ideal voltage-feedback operational amplifiers, the equations for voltage gains are as follows:

(14)
$$k_{in-d} = \frac{R_2}{R_1}\left(\frac{R_4}{R_3}+1\right)$$
$$k_{ref-c} = \frac{1}{2}\frac{R_7}{R_6+R_7}\left[2+\frac{R_3}{R_5}+\frac{R_2}{R_1}\left(1-\frac{R_3}{R_4}\right)\right]$$
$$k_{ref-d} = \frac{R_7}{R_6+R_7}\left[\frac{R_3}{R_5}-\frac{R_2}{R_1}\left(1+\frac{R_3}{R_4}\right)\right]$$
$$k_{in-c} = \frac{1}{2}\frac{R_2}{R_1}\left(\frac{R_3}{R_4}-1\right)$$

In order to fulfil the requirements that $k_{ref-d} = k_{in-c} = 0$, and $k_{ref-c} = 1$ (common choice) resistors should be selected so that

(15)
$$R_1 = R_7 = \frac{2}{k_d}R\,,\quad R_5 = \frac{1}{k_d}R,\quad R_2 = R_3 = R_4 = R_6 = R$$

where:
k_d – the assumed value of k_{in-d} gain (design parameter).

In practice, due to the mismatch of resistors, the real value of the individual gains differs from the nominal ones. By performing the worst-case analysis, we are able to determine the maximum and minimum values of the gains:

(16a)
$$k_{in-d-\max} = k_d\cdot\frac{1+\delta}{1-2\delta+\delta^2}\,,$$
$$k_{in-d-\min} = k_d\cdot\frac{1-\delta}{1+2\delta+\delta^2}\,;$$
$$k_{ref-c-\max} = \frac{1+\frac{k_d}{2}+\delta k_{d'}+\delta^2(\frac{k_d}{2}-1)}{1+\frac{k_d}{2}-\delta k_d+\delta^2(\frac{k_d}{2}-1)}\,,$$
$$k_{ref-c-\min} = \frac{1+\frac{k_d}{2}-\delta k_d+\delta^2(\frac{k_d}{2}-1)}{1+\frac{k_d}{2}+\delta k_d+\delta^2(\frac{k_d}{2}-1)}\,;$$

(16b)
$$k_{ref-d-\max} = \frac{4k_d\delta}{1+\frac{k_d}{2}-\delta k_d+\delta^2\left(\frac{k_d}{2}-1\right)},$$
$$k_{ref-d-\min} = \frac{-4k_d\delta}{1+\frac{k_d}{2}-\delta k_d+\delta^2\left(\frac{k_d}{2}-1\right)};$$
$$k_{in-c-\max} = \frac{k_d}{2}\cdot\frac{\delta(1+\delta)}{1-2\delta+\delta^2}\,,$$
$$k_{in-c-\min} = -\frac{k_d}{2}\cdot\frac{\delta}{1-\delta}\,;$$

where δ is the resistor tolerance specified by the resistor manufacturer or the resistor matching accuracy obtained during circuit trimming.

The derived equations allow the accurate values of gains variations to be calculated. Based on (16a) and (16b), we can also derive the bounds for the relative error of the gains k_{in-d} and k_{ref-c}. After neglecting the less significant terms, we obtain a simplified, compact form of the relationship between the gains and resistor tolerance.

(17)
$$\delta_{k_{in-d}} = \pm 3\delta$$
$$\delta_{k_{ref-c}} = \pm\frac{4\delta k_d}{k_d+2}$$

In the same way we can estimate the range for gain k_{ref-d} and k_{in-c},

(18)
$$k_{ref-d} = \pm\frac{8k_d}{k_d+2}\delta$$
$$k_{in-c} = \pm\frac{k_d}{2}\delta$$

and the bounds for the OBE and CME parameters

(19)
$$OBE = \pm\frac{\delta}{2}$$

(20)
$$CME = \pm\frac{8\delta}{k_d+2}$$

The obtained results, in a simple way, allow the DC accuracy of the single-ended to differential converter to be estimated, which is important from the practical point of view.

Adjustment

A useful design trick is to trim the resistors (e.g. by adding an adjustable resistor in a series or in parallel) so that the resulting gain is equal (or near) to the assumed value. The advantage of the circuit shown in Fig. 1a is that there is the possibility to adjust the individual voltage gains without an interaction. It is evident from (14) that the voltage gain k_{in-c} can be set to zero (or near zero) by trimming the value of R_3 (or R_4). Then, we are able to set the desired value of k_{in-d} by trimming R_2 (or R_1). Having R_1, R_2, R_3, R_4 fixed, the value of R_5 can be found to fulfil the requirement that k_{ref-d} = 0. In the last step, we trim the resistor R_6 (or R_7) to obtain the assumed value of the voltage gain k_{ref-c} (usually k_{ref-c} = 1).

Gain error due to CMRR

The operational amplifier common-mode rejection ratio (CMRR) is the next factor that influences the final value of the defined voltage gains. Assuming that the resistors are matched and modelling the CMRR parameter as in [17], we obtain the modified gain values:

(21) $$k'_{in-d} \approx 0 \cdot \frac{1}{CMRR_1} + 0 \cdot \frac{1}{CMRR_2} + k_d = k_d$$

(22) $$k'_{ref-c} \approx k_{ref-c} + 0 \cdot \frac{1}{CMRR_1} + \frac{1}{CMRR_2} = 1 + \frac{1}{CMRR_2}$$

(23) $$k'_{ref-d} \approx \frac{-2}{CMRR_1} + 0 \cdot \frac{1}{CMRR_2} = \frac{-2}{CMRR_1}$$

(24) $$k'_{in-c} \approx 0 \cdot \frac{1}{CMRR_1} + 0 \cdot \frac{1}{CMRR_2} = 0$$

where $CMRR_1$ and $CMRR_2$ are, respectively, the value of the CMRR of the OA1 and OA2 operational amplifiers (see Fig 2a). The voltage gains k_{in-c} and k_{in-d} are not influenced by the CMRR parameter.

The same analysis has also been done for the circuits shown in Fig. 2b-d. The following table summarises the parameters and properties of the analysed single-ended to differential converters.

Table 1. Comparison of DC parameters

	Fig. 2a	Fig. 2b	Fig. 2c	Fig. 2d
gain	(14)	$k_{in-d} = \frac{R_2}{R_1}\left(\frac{R_4}{R_3}+1\right)$ $k_{ref-c} = \frac{1}{2}\left[\frac{R_5\left(1+\frac{R_2}{R_1}\right)\left(1-\frac{R_4}{R_3}\right)}{R_5+R_6}+1+\frac{R_4}{R_3}\right]$ $k_{ref-d} = \left(1+\frac{R_4}{R_3}\right)\left[1-\left(1+\frac{R_2}{R_1}\right)\frac{R_5}{R_5+R_6}\right]$ $k_{in-c} = \frac{1}{2}\frac{R_2}{R_1}\left(\frac{R_4}{R_3}-1\right)$	$k_{in-d} = \frac{\frac{R_2}{R_1}\left(\frac{R_4}{R_3}+1\right)}{1+\frac{R_4}{R_3}\left(1+\frac{R_2}{R_1}\right)\frac{R_5}{R_5+R_6}}$ $k_{ref-c} = \frac{1}{2}\left[1+\frac{\frac{R_4}{R_3}+\left(1+\frac{R_2}{R_1}\right)\frac{R_5}{R_5+R_6}}{1+\frac{R_4}{R_3}\left(1+\frac{R_2}{R_1}\right)\frac{R_5}{R_5+R_6}}\right]$ $k_{ref-d} = \frac{\left(\frac{R_4}{R_3}+1\right)\left[1-\left(1+\frac{R_2}{R_1}\right)\frac{R_5}{R_5+R_6}\right]}{1+\frac{R_4}{R_3}\left(1+\frac{R_2}{R_1}\right)\frac{R_5}{R_5+R_6}}$ $k_{in-c} = \frac{1}{2}\cdot\frac{\frac{R_2}{R_1}\left(\frac{R_4}{R_3}-1\right)}{1+\frac{R_4}{R_3}\left(1+\frac{R_2}{R_1}\right)\frac{R_5}{R_5+R_6}}$	$k_{in-d} = \frac{R_4}{R_3+R_4}\left(1+\frac{R_2}{R_1}\right)+\frac{R_{2'}}{R_{1'}}$ $k_{ref-c} = \frac{1}{2}\left[\frac{R_3\left(1+\frac{R_2}{R_1}\right)}{R_3+R_4}+\frac{R_{3'}\left(1+\frac{R_{2'}}{R_{1'}}\right)}{R_{3'}+R_{4'}}\right]$ $k_{ref-d} = \frac{R_3\left(1+\frac{R_2}{R_1}\right)}{R_3+R_4}-\frac{R_{3'}\left(1+\frac{R_{2'}}{R_{1'}}\right)}{R_{3'}+R_{4'}}$ $k_{in-c} = \frac{1}{2}\left[\frac{R_4}{R_3+R_4}\left(1+\frac{R_2}{R_1}\right)-\frac{R_{2'}}{R_{1'}}\right]$
condition	(15)	$R_1 = R_5 = \frac{2}{k_d}R$ $R_2 = R_3 = R_4 = R_6 = R$	$R_1 = R_5 = \frac{1}{k_d}R$ $R_2 = R_3 = R_4 = R_6 = R$	$R_1 = R_3 = R_{1'} = R_{3'} = \frac{2}{k_d}R$ $R_2 = R_4 = R_{2'} = R_{4'} = R$
Gain (CMRR)	(21)-(24)	$k'_{ref-d} \approx \frac{-2}{CMRR_1}+\frac{2}{CMRR_2}$ $k'_{ref-c} \approx k_{ref-c}+\frac{1}{CMRR_2}$ $k'_{in-d} = k_d$ $k'_{in-c} = 0$	$k'_{ref-d} \approx \frac{-1}{CMRR_1}$ $k'_{ref-c} \approx k_{ref-c}+\frac{1}{CMRR_2}$ $k'_{in-d} = k_d - \frac{0.5k_d}{CMRR_1}$ $k'_{in-c} = 0$	$k'_{ref-d} \approx \frac{1}{CMRR_1}-\frac{1}{CMRR_2}$ $k'_{ref-c} \approx k_{ref-c}+\frac{0.5}{CMRR_1}+\frac{0.5}{CMRR_2}$ $k'_{in-d} = k_d + \frac{0.5k_d}{CMRR_1}$ $k'_{in-c} = \frac{0.25k_d}{CMRR_1}$
$\delta_{k_{in-d}}$	(17)	$\delta_{k_{in-d}} = \pm 3\delta$ $\delta_{k_{in-d}} = 0$ (from CMRR)	$\delta_{k_{in-d}} = \pm 2\delta$ $\delta_{k_{in-d}} = -\frac{0.5}{CMRR_1}$ (from CMRR)	$\delta_{k_{in-d}} = \pm 2\delta$ $\delta_{k_{in-d}} = \frac{0.5}{CMRR_1}$ (from CMRR)
$\delta_{k_{ref-c}}$	(17)	$\delta_{k_{ref-c}} = \pm\frac{4k_d\delta^2}{k_d+2}$ $\delta_{k_{ref-c}} = \frac{1}{k_{ref-c}CMRR_2}$ (from CMRR)	$\delta_{k_{ref-c}} = \pm\frac{2k_d\delta^2}{k_d+1}$ $\delta_{k_{ref-c}} = \frac{1}{k_{ref-c}CMRR_2}$ (from CMRR)	$\delta_{k_{ref-c}} = \pm\frac{4k_d\delta}{k_d+2}$ $\delta_{k_{ref-c}} = \frac{1}{k_{ref-c}}\left(\frac{0.5}{CMRR_1}+\frac{0.5}{CMRR_2}\right)$ (from CMRR)

k_{in-c}	(18)	$k_{in-c} = \pm(k_d/2)\delta$ $k_{in-c} = 0$ (from CMRR)	$k_{in-c} = \pm(k_d/2)\delta$ $k_{in-c} = 0$ (from CMRR)	$k_{in-c} = \pm k_d \delta$ $k_{in-c} = \frac{0.25 k_d}{CMRR_1}$ (from CMRR)
k_{ref-d}	(18)	$k_{ref-d} = \pm \frac{8 k_d \delta}{k_d + 2}$ $k_{ref-d} = \frac{-2}{CMRR_1} + \frac{2}{CMRR_2}$ (from CMRR)	$k_{ref-d} = \pm \frac{4 k_d \delta}{k_d + 1}$ $k_{ref-d} = \frac{-1}{CMRR_1}$ (from CMRR)	$k_{ref-d} = \pm \frac{2 k_d (k_d + 2)\delta}{k_d + 1 + 0.5 k_d^2}$ $k_{ref-d} = \frac{1}{CMRR_1} - \frac{1}{CMRR_2}$ (from CMRR)
OBE	(19)	$OBE = \pm(\delta/2)$ $OBE = 0$ (from CMRR)	$OBE = \pm(\delta/2)$ $OBE = 0$ (from CMRR)	$OBE = \pm\delta$ $OBE = \frac{0.25}{CMRR_1}$ (from CMRR)
CME	(20)	$CME = \pm \frac{8\delta}{k_d + 2}$ $CME = \frac{1}{k_d}\left(\frac{-2}{CMRR_1} + \frac{2}{CMRR_2}\right)$ (from CMRR)	$CME = \pm \frac{4\delta}{k_d + 1}$ $CME = -\frac{1}{k_d CMRR_1}$ (from CMRR)	$CME = \pm \frac{8\delta}{k_d + 2}$ $CME = \frac{1}{k_d}\left(\frac{1}{CMRR_1} - \frac{1}{CMRR_2}\right)$ (from CMRR)
adjust-able	Y	Y	N	N

AC analysis

The AC parameters of a single-ended to differential converter are important factors that characterise its quality and usability in specific applications. The four gains described by (8) should remain constant in the full span of the frequencies in which a circuit works. However, particular gains depend on the frequency as a result of parasitic capacitances, inductances and also the limited bandwidth of the components used.

Frequency dependence of gains

The dominant factor, which influences the transfer functions of converters, is the limited gain-bandwidth product of the operational amplifiers. A simplified (single-pole) open-loop transfer function of a voltage-feedback operational amplifier can be expressed as:

(25) $$A(s) = \frac{A_0}{1 + s/\omega_P}$$

where:
A_0 – DC open loop gain,
ω_P – dominant pole frequency.

The DC gain A_0 in real circuits is much greater than the close-loop gains, so the dependency (25) can be simplified to the following form:

(26) $$A(s) = \frac{A_0 \omega_P}{s} = \frac{\omega_T}{s}$$

where:
ω_T – gain-bandwidth product of the amplifier, i.e. the frequency for which the open loop gain decreases to 1.

The circuit presented in Fig. 2a was analysed using the simplified model of the operational amplifier given by (26). Assuming that both operational amplifiers have the same ω_T and the resistors are adjusted to obtain the DC gains $k_{in-d} = k_d$, $k_{in-c} = 0$, $k_{ref-d} = 0$, $k_{ref-c} = 1$, the transfer functions of the converter given in Fig. 2a are presented in Table 2.

The characteristic parameters used in the Table 2 are given by:

(27) $$\omega_X = \frac{\sqrt{2}}{2 + k_d} \cdot \omega_T$$

(28) $$Q = \frac{\sqrt{2}}{2}$$

Table 2. Transfer functions of a single-ended to differential converter for limited bandwidth operational amplifiers

Input \ Output	$v_{out,dm}$	$v_{out,cm}$
v_{in}	$k_{in-d}(s) = k_d \cdot \frac{1 + \frac{s}{2Q\omega_X}}{1 + \frac{s}{Q\omega_X} + \frac{s^2}{\omega_X^2}}$	$k_{in-c}(s) = k_d \cdot \frac{\frac{s}{4Q\omega_X}}{1 + \frac{s}{Q\omega_X} + \frac{s^2}{\omega_X^2}}$
v_{ref}	$k_{ref-d}(s) = -\frac{\frac{s}{Q\omega_X}}{1 + \frac{s}{Q\omega_X} + \frac{s^2}{\omega_X^2}}$	$k_{ref-c} = \frac{1 + \frac{s}{2Q\omega_X}}{1 + \frac{s}{Q\omega_X} + \frac{s^2}{\omega_X^2}}$

One can notice that the $k_{in-d}(s)$ transfer function corresponds to low-pass filtering with the DC gain equal to k_d and a corner frequency depending on k_d. The $k_{in-c}(s)$ corresponds to band pass filtering. Its quality factor Q is independent of the gain k_d. The OBE calculated according to (12) reaches its maximum value of ¼ at the characteristic frequency ω_X. The transfer function from the reference input to the common-mode output $k_{ref-c}(s)$ represents low-pass filtering with a DC gain equal to 1 and a corner frequency near ω_X. The transfer function from the reference input to the differential output $k_{ref\text{-}d}(s)$ represents band-pass filtering with a fixed quality factor Q and a maximum gain equal to 1 for the characteristic frequency ω_X which is dependent on the gain k_d and the gain-bandwidth product of the amplifiers. The maximum value of the $k_{ref\text{-}d}$ gain is independent of the assumed gain k_d. It is not possible to reduce this gain, for example by adding compensating capacitors. Such a big value of $k_{ref\text{-}d}$ can be a serious problem especially in the circuits where the reference signal noise should not affect the differential output signal – mostly in the adjustment devices that are used to supply differential voltages with an AC common-mode component. The frequency characteristics that were obtained as the simulation results in SPICE are presented in Fig. 3.

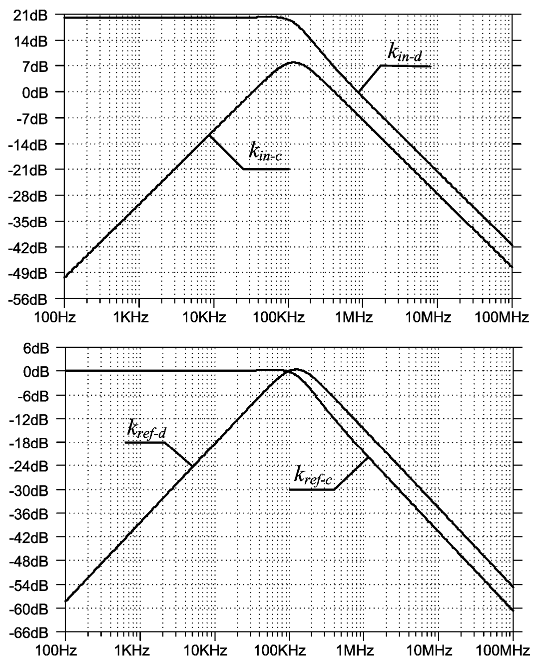

Fig. 3. Frequency response of the converter (simulation results)

The circuit was simulated for the assumed gain k_d = 10 and gain-bandwidth product of the amplifiers ω_T = $2\pi\cdot 1$ MHz.

The gains values, corner frequencies and quality factors obtained in simulation correspond to values calculated according to the equations given in Table 2.

Fig. 4 presents the step response of the analysed converter. The differential gain k_d was set to 1. At 10 µs the step change of the reference voltage was applied, and after 20 µs the step change of the input signal was applied. The step levels of the input signal and reference signal were set to 1 V. The waveforms in the figure are shifted up and down for clarity.

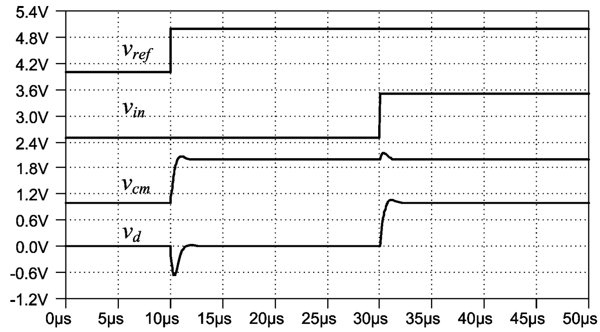

Fig. 4 Step response of the converter – differential-mode and common-mode

One can see a glitch that appears in the differential output signal as a result of the step change of the reference voltage. Its level is about 0.6 V, which can be unacceptable in specific applications. The only way to avoid it is to add a low-pass filter between the reference source and the reference input of the circuit. This can be done in circuits where the bandwidth of the $k_{ref\text{-}c}$ transfer function is not critical.

Comparison of the AC performance of the analysed single-ended to differential converters

In order to compare the parameters of analysed converters, SPICE simulations were performed. The resistors values in each circuit were selected for the assumed gain k_d = 10. The gain-bandwidth product of the amplifiers was set to ω_T = $2\pi\cdot 1$ MHz. The features obtained from the simulations are presented in Table 3 (where f_C denotes the corner frequency).

Table 3. Comparison of the AC parameters of the analysed single-ended to differential converters

	Circuit 1 – Fig. 2a	Circuit 2 – Fig. 2b	Circuit 3 – Fig. 2c	Circuit 4 – Fig. 2d
$k_{in\text{-}d}$	LPF, f_C = 0.6 MHz	LPF, f_C = 0.42 MHz	LPF, f_C = 0.9 MHz	LPF, f_C = 0.67 MHz
$k_{in\text{-}c}$	BPF, K_{MAX} = -12 dB f_C = 0.47 MHz	BPF, K_{MAX} = -17 dB f_C = 0.56 MHz	BPF, K_{MAX} = -12 dB f_C = 0.7 MHz	LPF K_{MAX} = -190 dB f_C = 0.67 MHz
$k_{ref\text{-}d}$	BPF, K_{MAX} = 0 dB f_C = 0.47 MHz	No compensation BPF, K_{MAX} = -11 dB f_C = 0.58 MHz With compensation [9] K_{MAX} = -57 dB f_C = 0.47 MHz	BPF, K_{MAX} = 0 dB f_C = 0.7 MHz	0 (assuming identical operational amplifiers and identical resistors)
$k_{ref\text{-}c}$	LPF, f_C = 0.6 MHz	LPF, f_C = 0.9 MHz	LPF, f_C = 0.9 MHz	LPF, f_C = 0.67 MHz
Step response	Oscillatory	Aperiodical	Oscillatory	Aperiodical
Glitch in v_d step response	0.6 V	0.13 V	0.6 V	0 V

Conclusions

Knowledge about the DC and AC parameters of single-ended to differential converters is essential in order to maximise their functionality. This paper attempts to be a practical guide to designing and developing this type of circuits. The main results, which are presented in the form of tables, allow for a quick and easy comparison between all of solutions. In order to select the proper single-ended to differential converter, the designer has to consider the different features of a circuit – application requirements, bandwidth, resistor tolerances and CMRR values. The relationships and hints presented in this paper should help designers to select the best structure and to evaluate the errors that can appear in a circuit.

The performed analyses were validated with SPICE simulations using an assumed, idealised model of the operational amplifier. The obtained results show the precise agreement between the analytical model and the simulations. The simulations were then repeated with the real operational amplifier. The single ended to differential converters were also simulated with models of LT1007 (equivalent to the popular OP27) [18]. The frequency domain characteristics were analogous to those obtained for a single pole model of an op-amp. The response of each circuit to the step change of the reference voltage contained larger glitches, which was the result of considering higher order poles.

The main conclusions that were drawn from the study are as follows. A phase imbalance (phase deviation from the nominal 180° phase shift of the differential outputs) causes a small frequency-dependent common-mode component which appears at the outputs. The OBE parameter, defined by (12), is a measure of this non-ideality. It is worth noting that the phase imbalance, which was measured by the OBE, was only caused by a ground referenced single-ended input signal (we assume v_{ref} = 0). Thus, the OBE parameter is essential for applications such as ADC driving and differential line data transmission. At DC, the phase balance is limited by matching the resistors and the CMRR of the operational amplifiers. According to Table 1, the minimum value of the OBE is provided by circuits 2a, 2b, 2c. However, the AC transfer function $k_{ref\text{-}c}(j\omega)$ for these circuits corresponds to the band-pass filtering. This means that the OBE degrades at higher frequencies. The circuit presented in Fig. 2d is much better balanced. Its $k_{ref\text{-}c}(j\omega)$ transfer function is nearly constant from DC to the corner frequency of the circuit. For the simulated circuit, its gain was as low as –190 dB.

On the other hand, there are circuits that are used to test the differential amplifiers, strain gauge amplifiers and medical ECG amplifiers. In such applications one of the most important parameters is the CME error, which characterises the undesired differential component that is produced by the reference signal. Comparing the parameters of the analysed circuits, we can point out that the circuit presented in Fig. 2b, seems to be the best choice for this purpose because of the lowest number of resistors that have to be matched and the possibility to adjust the individual voltage gains without an interaction. Further advantages are the compensation of the CMRR influence to the CME and the possibility of the CME compensation in AC by means of an additional capacitor [9].

Acknowledgements

This work was supported by the Ministry of Science and Higher Education funding for statutory activities.

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