

# Broadband power electronics controlled voltage source with output stage based on GaN transistors

**Abstract.** The work presents the power electronics controlled voltage source (V CVS) with a modified sigma-delta modulator (SDM) in the control section. The modulator includes an analog comparator with dynamic hysteresis instead of a latched comparator, being typically used in single-bit SDMs. Thank to this feature a resolution of the SDM output signal is, theoretically, unlimited. Due to very high frequency of the SDM output bit stream in the power stage of V CVS the GaN transistors are used. Planned field of application of the converter is an Automated Test Equipment (ATE). In the work the converter's operation basics and selected results of its simulation model studies are presented.

**Streszczenie.** W pracy zaprezentowano energoelektroniczne sterowane źródło napięcia ze zmodyfikowanym modulatorem sigma-delta w bloku sterowania. Modulator zawiera komparator z dynamiczną pętlą histerezy zamiast, typowo stosowanego, komparatora „zatraskowego”. Dzięki temu rozdzielczość sygnału wyjściowego modulatora jest, teoretycznie, nieskończona. Z powodu znacznej wartości częstotliwości strumienia bitowego na wyjściu modulatora, w bloku wykonawczym użyto tranzystorów GaN. Planowanym polem zastosowań źródła napięcia jest sprzęt do testowania urządzeń elektrycznych dużej mocy. W pracy przedstawiono zasadę działania źródła oraz przedstawiono wybrane wyniki badań jego modelu symulacyjnego. (Szerokopasmowe energoelektroniczne sterowane źródło napięcia ze stopniem mocy bazującym na tranzystorach GaN).

**Keywords:** converter topology, GaN transistor, pulse modulation, reference voltage generator.

**Słowa kluczowe:** struktura przekształtnika, tranzystor GaN, modulacja impulsowa, generator napięcia wzorcowego.

## Introduction

A non-linearity of loads, limited frequency response of power electronics converters, and wide-band nature of signal sampling and pulse width modulation processes are reasons of inaccurate mapping a converter's output voltage in an input signal. To meet this requirement both advanced solutions of converters in hardware and in control algorithms are necessary. One of them is a sigma-delta modulator. The sigma-delta modulators are widely used in the A/D converters [1,2], Class-D Amplifiers [3,4], and equipment for power electronics systems [5]. In the work the modified sigma-delta modulator with dynamic hysteresis comparator (DHCS DM) is used to direct control of the output stage of a power electronics controlled voltage source (V CVS).

The basic premise of the proposed DHCS DM conception is obtainment of precise mapping of the converter output voltage in the input (reference) signal. Besides, the structure of control system is simple, i.e. mostly analogu one (no “purely” digital components are used in the DHCS DM), and can be easily implemented in power electronics equipment, where high quality of the output quantity (i.e. voltage) is necessary. Due to high frequency of the DHCS DM output bit stream in the inverter the gallium-nitride (GaN) transistors are used. As result, the value of distortions of the inverter output voltage are lower, compared to a typical, i.e. digital PWM based, solutions [6,7]. This benefit is not paid significantly by increase in the system complexity.

The paper presents the first stage of work on the layout of this type of converter. The planned final effect of the work is design of the laboratory prototype of a medium power Reference Voltage Generator (RVG). The main expected application area of the RVG is ATE (Automated Test Equipment) – for testing energy meters and special purpose electrical machines (motors and transformers).

The following text is divided into three sections. The first one deals with the structure and the rule or work of the SDM based voltage source. The second one shows the simulation model researches for the V CVS. In the last part conclusions are presented.

## Basics of converter's operation

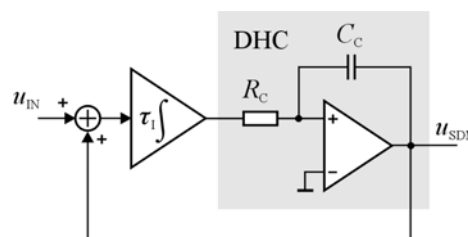
The DHCS DM principles of operation was dedicated the work [7]. Therefore, only a brief detail of the DHCS DM is

given here for reader's convenience. From a point of view of a kind of modulation a typical SDM output signal is a pulse-duration modulated (PDM). A duration of a single bit is equal to a period of sampling clock:  $T_S = \frac{1}{f_s}$ . This one

determines a time resolution, thereby a pass-band, of a SDM. If a SDM is a part of ADC architecture, achieving even high value of a sampling clock is not a technical and technological problem nowadays [1,2]. This situation rapidly changes if modulator is used in a structure of power electronics converter. The reasons for this are simply dynamic parameters of actual power semiconductor devices. As result, a THD and other parameters of amplifier are often unsatisfactory. A solution to this problem can be use pulse-width instead of pulse-duration modulation strategy in a converter.

The proposed modulator is similar to a typical single-bit SDM however, no latched comparator is used in their structure. Instead, a comparator with dynamic hysteresis (DHC) is included. The DHC is the sub-circuit shown in the shaded area in Fig.1.

a)



b)

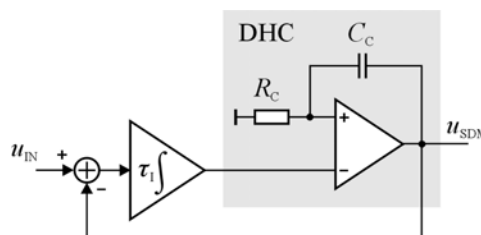


Fig.1. Diagram of SDM with dynamic hysteresis comparator (DHC) in (a) “non-inverting” and (b) “inverting” version

The particular feature of the proposed SDM solution is that, it does not use a sampling signal. Instead, it generates the PWM similar signal with the “carrier” frequency, which value depends on the time constant of the comparator  $\tau_C$ , where  $\tau_C = R_C C_C$ . A “carrier” frequency value varies with the SDM input signal magnitude. Thanks to the structure of SDM is mostly analog (the SDM is continuous-time circuit) duration of its output signal can be, theoretically, arbitrarily small. Thus, the time resolution of this one tends to infinity. The sigma-delta modulators are very difficult to analyze in the time domain because of its apparent randomness of the single-bit data output – the system is both non-linear and time variant. Usually, more or less simplified models of SDM in a frequency domain are in use, e.g. [1,2,9]. These models are often used for a system stability analysis.

By means of heuristic methods following equation has been formulated [7]. This one specifies the value of the PWM “carrier” frequency of SDM output signal (however, the equation is valid for small values of the modulation index only)

$$(1) \quad f_C = \frac{1}{5\tau_C}.$$

The modulation index ( $m$ ) is determined similarly like in case of typical PWM

$$(2) \quad m = \frac{|u_{IN}|}{|u_{SDM}|}.$$

If  $\tau_1$  (Fig. 1) in relation to  $\tau_C$  is too small the system stability can be an issue [2,7]. For obtaining of this the following equation has to be met

$$(3) \quad \tau_1 > 2\tau_C.$$

By fulfilling (3) the integrator is also prevented from entering its output in a signal clipping state [7].

In the following figures the spectrum of DHCSM output signal, for different values  $m$ , is shown. For actual mathematical model parameters ( $\tau_1$ ,  $\tau_C$ ) the switching frequency is approximately equal to 1 MHz.

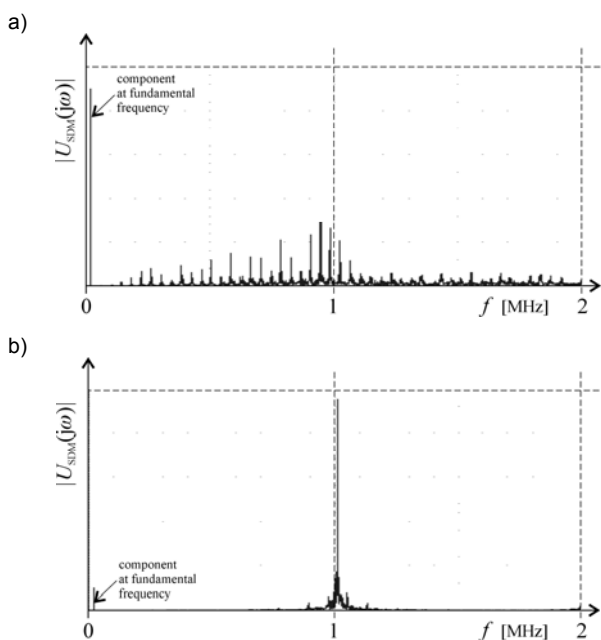


Fig.2. Spectrum of SDM output signal if (a)  $m = 0.9$ , (b)  $m = 0.1$

The frequency of the DHCSM switching pattern is a spread spectrum in nature however, while amplitude of the input signal decreases, this spectrum focuses more and more on the value given by (1). The spread-spectrum techniques are often applied to distribute the emissions over a wider range of frequency [10].

In Fig. 3 the general block scheme of the proposed converter is presented. This one has a semi-differential topology, i.e. an input signal ( $u_{IN}$ ) is referred to a common system ground while an output signal ( $u_L$ ) is a differential one.

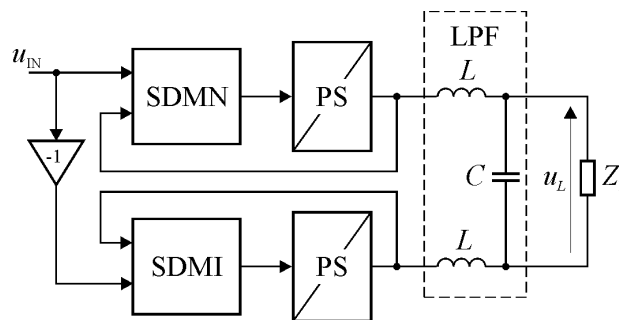


Fig.3. Block scheme of VCVS

The amplifier consists of following elements: two SDMs (in both “non-inverting” and “inverting” version, what is necessary for minimizing “carrier” frequency components in output differential signal), two separate power stages (PS – about half-bridge topology), and common LC low-pass filter (LPF) at the PSs outputs. The filter is necessary for minimizing the “carrier” component in the output signal.

Because an output of VCVS is a differential one (2) takes now the new form as follows

$$(4) \quad m = \frac{|2u_{IN}|}{|u_L|}.$$

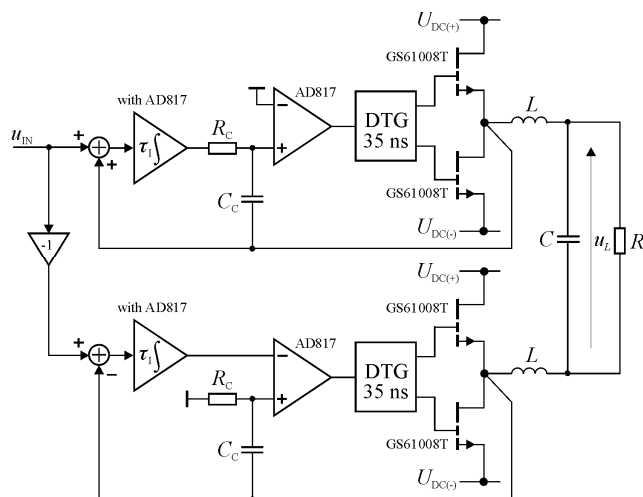


Fig.4. Block diagram of VCVS simulation model

### Simulation model studies

For checking theoretical assumptions the simulation model of VCVS with use of the ORCAD/PSpice tool was studied. Following features of the model were evaluated: THD and slew rate of an output voltage as well as large signal pass band.

The diagram of the model is shown in Fig. 4. The most valid for the model functionality devices were AD817 – an ultra fast operational amplifier (Analog Devices Inc.) – being

used in the integrator and the comparator of SDM and GS61008T – the 100 V/ 90 A gallium nitride E-HEMT [11] (GaN Systems) – being used in the power stage of the simulation model. In the VCVS model ready to use models of GaN E-HEMTs, provided by GaN Systems, were used.

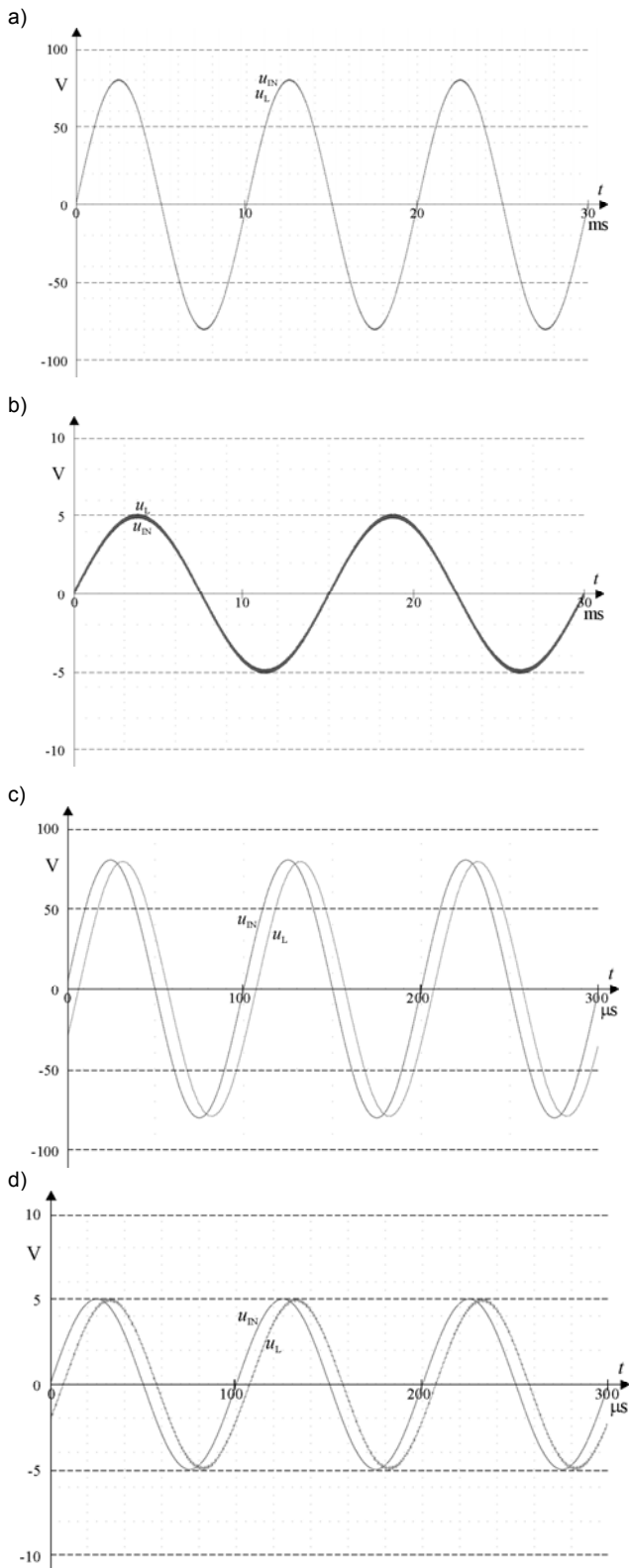


Fig.5. Waveforms in the simulation model while the input signal is a sinusoidal one and a)  $f_{IN}=100\text{ Hz}$ ,  $m=0.8$ , b)  $f_{IN}=100\text{ Hz}$ ,  $m=0.05$ , c)  $f_{IN}=10\text{ kHz}$ ,  $m=0.8$ , and d)  $f_{IN}=10\text{ kHz}$ ,  $m=0.05$

The basic model's parameters were as follows:  $\tau_I=200\text{ ns}$ ,  $\tau_C=500\text{ ns}$ , dead-time for the half-bridge in the power stage – 35 ns (the dead-time was generated by the DTG block),  $L=10\text{ }\mu\text{H}$ ,  $C=1\text{ }\mu\text{F}$ , and nominal magnitude of the output current:  $i_{L,n}=20\text{ A}$ . The voltages at inverter's DC rails:  $U_{DC}=\pm 50\text{ V}$ .

In Fig.5 exemplary waveforms in the simulation model are shown. Primarily they differ in shape, magnitude, and fundamental frequency of the input signal.

It can be observed that, while input signal's frequency is below of 1 kHz, a phase delay of the output signal, in the relation to  $u_{IN}$ , is negligible (Fig. 5a, 5b). However, for higher frequencies it becomes visible (Fig. 5c, 5d).

In the following figure  $THD$  of  $u_L$  vs. modulation index is shown. This one is also related to two different fundamental frequencies of  $u_{IN}$  i.e. 100 Hz and 10 kHz.

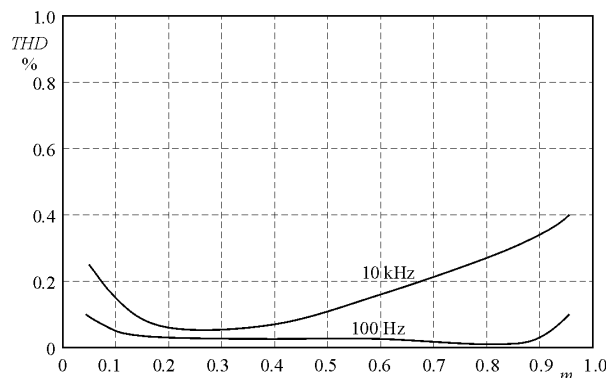


Fig.6. Curve of  $THD$  of output signal vs. modulation index while signal frequency is equal to 100 Hz or 10 kHz

While value of  $f_{IN}$  not exceeds 1 kHz in all analyzed range of modulation index the  $THD$  value was below of 0.1 %. However, while this frequency is equal to a few kHz (up to 10 kHz) value of  $THD$  grows up to 0.5 %.

In Fig. 7 response of simulation model to the rectangular input signal is presented. It allows evaluate a pass-band of the VCVS simulation model.

A slew rate ( $SR$ ) of the output signal is defined as follows [1]

$$(5) \quad SR = \frac{\Delta u_L}{\Delta t}$$

For actual model's parameters  $SR$  was equal to 7 V/ $\mu$ s (Fig. 7b).

To determine an approximate large-signal bandwidth ( $BW$ ) of the model the following formula was used [1]

$$(6) \quad BW = \frac{SR}{2\pi A_L}$$

where  $A_L$  is the output signal's magnitude.

Assuming  $A_L=100\text{ V}$  (i.e.  $m=1.0$ ) the bandwidth of the VCVS is equal to 11 kHz. This one can be extended through increasing of LC output filter's pass-band however, magnitude of "carrier" frequency components in the VCVS output signal will grow also.

Thus, the proposed VCVS, based on the DHCSM, is characterized by much wider the pass-band compared to typical converter's solutions [6,8].

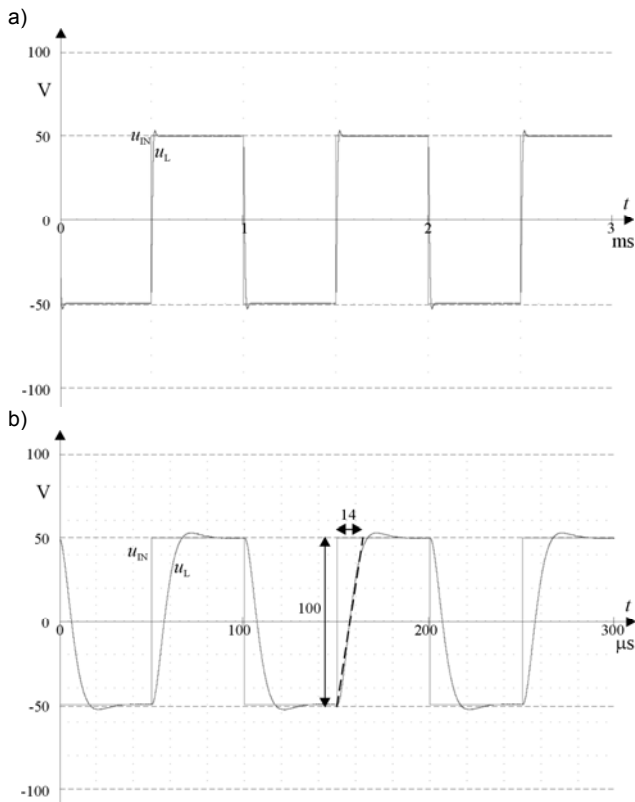


Fig.7. Waveforms in the simulation model while the input signal is a rectangular one and  $m=0.5$ : a)  $f_{IN}=1$  kHz, b)  $f_{IN}=10$  kHz

## Conclusions

The power electronics controlled voltage source based on the sigma-delta modulator with dynamic hysteresis loop and the output stage with the GaN transistors is characterized by wide the pass-band, compared to typical converter's solutions. As result, the output voltage waveform is precisely mapped in the input signal. Thanks to operation of the converter at very high switching frequency also components of pulse modulation are minimized. The structure of control section is simple, mostly analogue one, and can be easily implemented in power electronics equipment, where high quality of the output voltage (current) is necessary. These benefits are not significantly paid by increase in the system complexity and the system cost.

The presented solution of the converter can find application in many power electronics equipment like reference voltage generators, serial active power filters, and converters for RES.

**Author:** Michał Gwóźdź, PhD. DSc. Eng., Poznan University of Technology, Institute of Electrical Engineering and Electronics, Piotrowo 3A Street, 60965 Poznań, POLAND, E-mail: Michal.Gwozdz@put.poznan.pl.

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