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Radosław NALEPA[1], Marcin ZYGMANOWSKI[2], Jarosław MICHALAK[2]

Wroclaw University of Science and Technology (1), Silesian University of Technology (2)

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Dual-Active-Bridge converter inductance DC-bias current compensation under low and high load conditions

Abstract*. Operation of the Dual-Active-Bridge converter in steady state and dynamic conditions are presented in this paper basing on a simulation model taking into account the bridge inductance DC-bias current driven by the volt-second unbalance within PWM cycles. In the paper the bridge operation within the output power range from <1% to the 100% is presented under: a) basic output voltage closed loop control, b) output voltage with proposed DC-bias current compensation control strategies. At this stage of research power losses generated inside of the converter have not been taken into account.*

Streszczenie. *W artykule prezentuje się pracę przekształtnika typu DAB zarówno w stanie ustalonym jak i stanach dynamicznych bazując na modelu symulacyjnym w którym uwzględniono możliwość występowania składowej stałej prądu dławika spowodowanej niezerową wartością średniej bieżącej jego napięcia. W artykule analizuje się pracę w zakresie mocy równych od <1% do 100% mocy znamionowej gdy przekształtnik pracuje z a) podstawowym sterowaniem ze sprzężeniem od napięcia wyjściowego, b) sterowaniem napięcia wyjściowego z uwzględnieniem zaproponowanych metod kompensacji składowej stałej prądu. W pokazanej analizie nie uwzględniono strat mocy generowanych w przekształtniku.* ***Kompensacja składowej stałej prądu indukcyjności konwertera z podwójnym mostkiem aktywnym w warunkach niskiego i wysokiego obciążenia.***

Keywords: dual active bridge, DC-bias current, feed-forward control.
Słowa kluczowe: podwójny mostek H, składowa stała prądu, sterowanie feed-forward.

Introduction

Advanced power distribution grids are often considered as smart grids [1]. Generally speaking, such grids rely on various measurements, information exchange by communication means and advanced control actions in order to enable (bidirectional) electric energy flow between energy sources (including renewables and energy storage) and the end user. In addition, the electric energy can be in form of AC and/or DC - this for cost reduction and efficiency reasons [1],[2]. All that together creates challenging system environment in terms of ensuring its safe and stable operation.

Such a system creates opportunities for technologies developments which will facilitate its operation. One of such technology area is energy transformation between two different DC voltage levels within a DC-grid. The solution could come with development of a so called Solid State Transformer, SST [3]. The SST concept, Fig.1, is already in use for same time and with certain assumptions could be considered as a mature technology for low voltage applications. It relies on the Dual Active Bridge, DAB, DC-DC converter topology [4], Fig. 2.

Nevertheless the SST, basing on the DAB, related to medium-to-low DC voltage conversion, Fig. 1, e.g. 10 kV to 380V and power of 1 MW, still calls for attention. Especially in area of its control at all functional levels. The functional levels can be defined as following: 1st) individual DAB converter as a SST Module, SSTM; 2nd) group of DAB converters creating single SST; 3rd) group of SSTs acting inside of a smart grid.

In this paper, as the first step towards complete SST, authors concentrate on control of the 1st functional level, namely single DAB converter depicted in Fig. 2. Appropriate control solution must ensure, inter alia, a) steady-state operation of the DAB under light load (below 1% of the rated low voltage output power, $P_{\mathrm{DAB,LV}}^{\mathrm{rtd}}$) and full load (100% of $P_{\mathrm{DAB,LV}}^{\mathrm{rtd}}$); b) minimization of undesired DAB inductance DC-bias current (the same as the DAB transformer current), $i_{\mathrm{L,MV}}^{\mathrm{dc}} = i_{\mathrm{T,MV}}^{\mathrm{dc}}$ during transients, and in short-term steady-state operation [5],[6], with low overall circuit resistance. For simplicity reasons, the resistance is to be understood here as a combination of the power MOSFET module switches on-state resistance, $R_{\mathrm{DS,on}}$ and parasitic resistance of inductance, esr_{L}.

Control aspects of remaining SST functional levels (2nd and 3rd) will be subjects to further discussions and analysis in different publications. In this paper the DC-bias transformer current compensation method is proposed. Effect of low parasitic resistance in the current conducting paths is considered briefly too.

The SST general specification and the DAB basic parameters

As a compromise between grid equipment complexity and grid conduction power losses driven by high current, the medium DC-voltage of SST from Fig. 1, is assumed to be equal to $V_{\mathrm{SST,MV}}^{\mathrm{rtd}}$ = 10 kV with ±10% tolerance. This, with assumed SST total rated power of $P_{\mathrm{SST}}^{\mathrm{rtd}}$ = 1 MW (ideal lossless conversion), gives the medium DC-voltage side rated current equal to $I_{\mathrm{SST,MV}}^{\mathrm{rtd}}$ = 100 A. In such a case it can be assumed that a single 10 kV DC distribution grid line can easily handle up to 15 of such SST devices. As result, the DC-grid line total current will be at level near to $I_{\mathrm{grid,MV}}^{\mathrm{dc}}$ = 1.6 kA. Such assumption leads to relatively low cable cost within a 16 MW DC distribution grid.

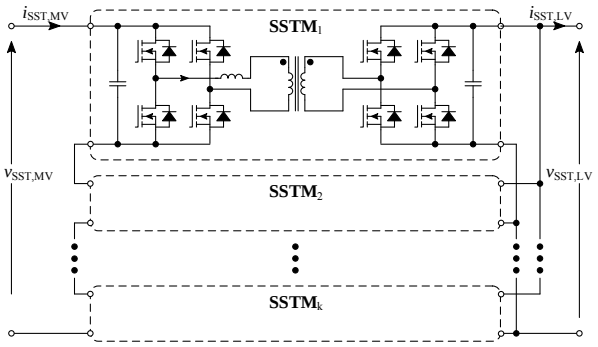

Fig.1. Solid state transformer, SST, general concept. Built of input-serial, output-parallel connected SST Modules, SSTM

Rated voltage at the low DC-voltage side is assumed as $V^{\mathrm{rtd}}_{\mathrm{SST,LV}}$ = 380 V. It stands for $I^{\mathrm{rtd}}_{\mathrm{SST,LV}}$ = 2.6 kA output current. This relatively high current can be handled by properly designed SST output power stage. Nevertheless in most of cases the current will be divided immediately after the SST terminals into smaller currents flowing to the end users.

Basing on such SST general specification, further assumptions for its DAB sub-circuits, SSTM, see Fig. 1, can be made. Assuming that there will be 14 of SSTM in stack, $SSTM_{\mathrm{k}}$ where $k \in \{1, 2,..,14\}$, connected as shown in Fig. 1, the input and output electrical parameters can be specified as in Table 1. The SSTM rated and minimum output powers are $P^{\mathrm{rtd}}_{\mathrm{SSTM,LV}}$ = 71.4 kW and $P^{\mathrm{min}}_{\mathrm{SSTM,LV}}$ < 0.714 kW respectively. Their rated voltages are $V^{\mathrm{rtd}}_{\mathrm{SSTM,MV}}$ = 714 V and $V^{\mathrm{rtd}}_{\mathrm{SSTM,LV}}$ = 380 V. The DAB transformer turns ratio is assumed as $n = V^{\mathrm{rtd}}_{\mathrm{SSTM,MV}}/V^{\mathrm{rtd}}_{\mathrm{SSTM,LV}}$.

In order to calculate the DAB inductance, L, the converter efficiency, η_{DAB}, is assumed to be not less than 85 % and at this stage without specific load range defined. The inductance is responsible for the SSTM power transfer.

Formula for calculation of the transferred power depends, inter alia, on the modulation scheme used to control the DAB. In this case the Phase Shift Modulation, PSM, is used. In consequence, (1) is used for purpose of the initial inductance value calculation,[7].

$$P_{SSTM} = \frac{V_{SSTM,MV} V_{SSTM,LV} n \varphi_{SSTM,LV} \left(\pi - \left|\varphi_{SSTM,LV}\right|\right)}{2\pi^2 f_s L} \quad (1)$$

where: P_{SSTM} – SSTM power transfer [W] assuming lossless conversion; $V_{\mathrm{SSTM,MV}}$, $V_{\mathrm{SSTM,LV}}$ – medium and low voltages respectively [V]; n – the transformer turns ratio; $\varphi_{SSTM,LV}$ – low voltage side phase shift angle [rad]; L – total DAB inductance; f_s = 16kHz is the switching frequency [Hz];.

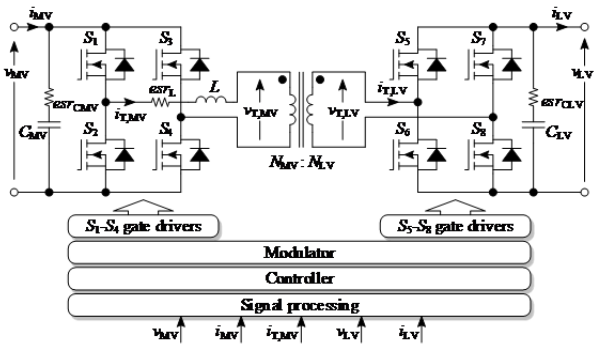

Fig.2. The DAB converter general overview

The PSM control scheme assumes variation of the phase shift, φ, between the gate drive signals of the medium DC-voltage side switches, S_{MV}, and the low DC-voltage side switches, S_{LV}. In considered case phase of the S_{LV} gate drive signals is changed, $\varphi_{\mathrm{SSTM,LV}}$. The changes are driven by control scheme No.I shown in Fig. 5. Of course with the switching pole dead time included. The medium DC-voltage side phase shift is assumed to be $\varphi_{SSTM,MV}$ = 0 rad. The $\varphi_{\mathrm{SSTM,LV}}$ varies between -π/2 and +π/2 rad. Power transfer direction, in this bidirectional circuit, depends on the $\varphi_{SSTM,LV}$ sign. Duty cycle for PSM control is fixed to $D_{\mathrm{MV}} = D_{\mathrm{LV}}$ = 0.5 for both the S_{MV} and the S_{LV}. While $S_1(S_5)$ and $S_4(S_8)$ are ON, the $S_2(S_6)$ and $S_3(S_7)$ are OFF and vice versa. In this paper, for simplicity reasons, the power transfer direction is from MV to LV side.

The initial inductance calculation results can be seen in Fig. 3. They indicate that L = 46μH should fulfil DAB power transfer requirements even at minimum voltage, $V^{\mathrm{min}}_{\mathrm{SSTM,MV}}$ = 642 V (-10% DC-grid tolerance), at regulated $V^{\mathrm{rtd}}_{\mathrm{SSTM,LV}}$ = 380 V, Fig. 3 dotted line - this with 15% DAB losses taken into account. Finally, L = 38 μH was selected basing on simulations with the given electrical parameters and with a modified control schemes discussed later in this paper. Inductance of the simulation model is located in one place - on MV side of an ideal transformer with turns ratio n = 2.

The MV DC-grid, for simplicity reasons, was assumed as a strong DC source. The converter input capacitance was set to relatively large value of C_{MV} = 100 mF with esr_{CMV} = 1mΩ. The output capacitance was set to C_{LV} = 3.03 mF with its esr_{CLV} = 4.39 mΩ, this in order to keep the output voltage ripple below 1%.

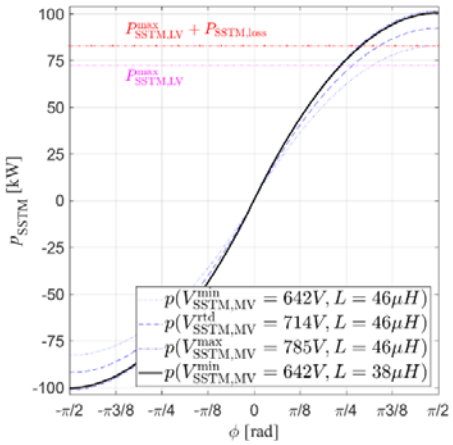

Fig.3. The DAB converter power transfer characteristics for phase shift modulation, PSM, according to (1) as functions of $\varphi_{SSTM,LV}$. Plots drawn for $V_{\mathrm{SSTM,LV}}$ = 380 V, $V_{\mathrm{SSTM,MV}}$ and L given in the plot legend. The inductance L = 38 μH was used in circuit considered in this paper

DAB control scheme No. I – basic control

The PSM is considered as the basic control scheme of the DAB. As already described, it simply relays on the $\varphi_{\mathrm{SSTM,LV}}$ variation in order to control transfer of electric power from one side of the converter to the other, and this according to (1) or Fig. 3. In a simple control scenario, assuming constant $v_{\mathrm{SSTM,MV}}$, the $v_{\mathrm{SSTM,LV}}$ is to be controlled. Such control can be realised according to simplified block diagram shown in Fig. 5, with scheme No. I. In this case the $v_{\mathrm{SSTM,LV}}$ is controlled by means of standard closed loop control with output limited PI compensator setting required $\varphi_{\mathrm{SSTM,LV}}$. The reference voltage is set to $V^{\mathrm{ref}}_{\mathrm{SSTM,LV}}$ = 380 V. The PI compensator gains were tuned manually for satisfactory simulation results. Such control scheme was applied to the earlier specified DAB and it was modelled in Matlab-Simulink environment.

Simulation results demonstrate presence of significant DC-bias transformer current, $i_{\mathrm{T,MV}}^{\mathrm{dc}}$ (equal to inductance DC-bias current $i_{\mathrm{L,MV}}^{\mathrm{dc}}$), in the measured transformer current, $i_{\mathrm{T,MV}}^{\mathrm{m}}$, especially during transients, see Fig. 7 to Fig. 9. The $i_{\mathrm{T,MV}}^{\mathrm{dc}}$, denoted as $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$, was calculated as average value of $i_{\mathrm{T,MV}}^{m}$ over each switching period - basing on 62 samples of the $i_{\mathrm{T,MV}}^{\mathrm{m}}$. The biggest $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$, near 254 A, appears at the beginning of the start-up. Similar situation was observed during the start-up phase of a down scaled laboratory circuit used as a quick qualitative validation of the simulation model built, see Fig. 4.

The DC-bias current in Fig. 4 settles to near 0-level after few switching cycles. This compensation effect is strongly supported by significant IGBT $R_{\mathrm{CE,on}}$ = 80 mΩ and esr_{L} ≈ 50 mΩ. The resistance effect in such circuit was considered in the simulation model used.

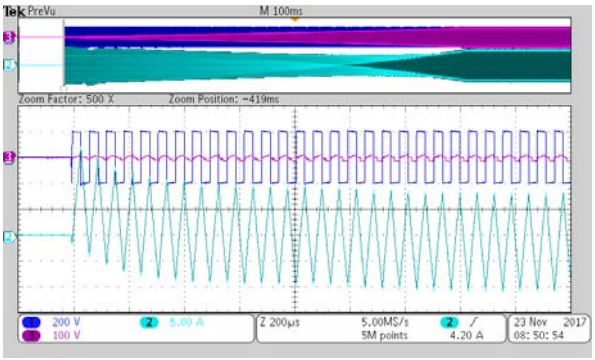

Fig.4. Laboratory measurements of a DAB, zoom of start-up: Ch1 – $v_{DAB,input}$, Ch2 - $i_{T,input}$, Ch3 - $v_{DAB,output}$. The circuit parameters: $V_{\mathrm{DAB,input}}^{\mathrm{rtd}}$ = 200 V, $V_{\mathrm{DAB,output}}^{\mathrm{rtd}}$ = 100 V, f_{s} = 16 kHz, L = 400 µH, $P_{\mathrm{DAB,input}}^{\mathrm{rtd}}$ = 1 kW

Results with $R_{\mathrm{DS,on}}$ = 55 mΩ and esr_{L} = 10 mΩ can be seen in Fig. 7. They are to be compared with Fig. 8, when $R_{\mathrm{DS,on}}$ = 5.5 mΩ as per CAS325M12HM2 component data sheet, for T_{J} = 125 □C and V_{GS} =20 V. It can be seen that initial $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$ during start-up, are similar (238 A in Fig. 7 and 254 A in Fig. 8) although declining faster in Fig. 7. Later on advantage of bigger $R_{\mathrm{DS,on}}$ is clear (4.6 A at 0.003s; 63 A at 0.015s; -47 A at 0.02s in Fig. 7 vs. 19 A at 0.003s; 93 A at 0.015s; -54 A at 0.02s in Fig. 8 respectively). Such results strongly encourage to reduce the $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$ of DAB in case of $R_{\mathrm{DS,on}}$ in range of few mΩ. At this stage effect of the esr_{L} is not considered for simplicity reasons but generally speaking the lower overall circuit parasitic resistance the more pronounced DC-bias current is.

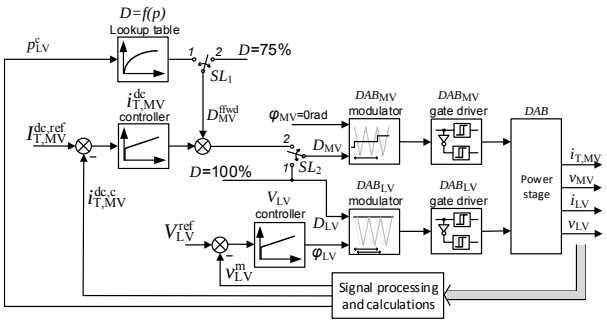

Fig.5. General overview of the DAB (SSTM) control schemes used: No. I - selector SL_2 in position 1; No. II - SL_2 in position 2 and SL_1 in position 2; No. III - SL_2 in position 2 and SL_1 in position 1

Results shown in Fig. 8 will be used as a base line for further simulation analysis and control solutions evaluation.

During start-up the measured converter output voltage, $v_{\mathrm{LV}}^{\mathrm{m}}$, follows reference ramp profile, $V_{\mathrm{LV}}^{\mathrm{ref}}$, (from 0 V to 380 V in 0.01s) and later $V_{\mathrm{LV}}^{\mathrm{ref}}$ = 380 V. The DAB runs from 0s to 0.015s under load of $p_{\mathrm{LV}}^{\mathrm{min}}$ = 0.357 kW (0.5% of $p_{\mathrm{LV}}^{\mathrm{rtd}}$) which stands for steady-state average current $\bar{I}_{\mathrm{LV}}$ = 0.99 A. At time of 0.015s $p_{\mathrm{LV}}^{\mathrm{rtd}}$ =71.4 kW ($\bar{I}_{\mathrm{LV}}$ = 188 A) is switched ON for 5ms. After that the load is equal again to $p_{\mathrm{LV}}^{\mathrm{min}}$ = 0.357 kW till the end of analysis at 25ms. The same profile is used in Fig. 9 and Fig. 10.

The PSM control scheme No. I in Fig. 5 ensures stable operation of DAB converter in load power range from minimum to rated. Nevertheless, the measured transformer current $i_{\mathrm{T,MV}}^{\mathrm{m}}$ contains undesired DC-bias component even in short-term steady-state conditions.

DAB control scheme No. II – simple DC-bias current reduction

In order to reduce the $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$ additional control loop was added to the basic control scheme No. I from Fig. 5. This created control scheme No. II, see Fig. 5. Additional PI compensator with a feed-forward path was added. The feed-forward constant value was set to 75% of the maximum duty cycle D_{MV} ($D_{\mathrm{MV}}^{\mathrm{ffwd}}$ = 0.5 * 0.75 = 0.375). The 75% and the PI compensator gains were selected manually basing on satisfactory simulation results – this as an initial approach.

The results can be seen in Fig. 9. The initial $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$ is now equal to 130 A which is 124 A less than in Fig. 8. The $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$ maximum absolute value after reaching $V_{\mathrm{LV}}^{\mathrm{ref}}$ = 380 V is equal to 15.4 A at 0.0103s. Although the transient DC-bias currents are significantly reduced, the short-term steady-state DC-bias current are still too large (about -9 A in average). Therefore further control solution improvements are needed.

DAB control scheme No. III – advanced DC-bias current reduction

As improvement of the control scenario No. II, the constant feed-forward value was replaced by a variable value dependent on the calculated output power level, p_{LV}^{c}, see scenario No. III in Fig. 5. It has been implemented as a look-up table with profile shown in Fig. 6. The profile was manually set for satisfactory performance, this as an initial setup for purpose of this publication. In future there will be optimized tuning guidelines.

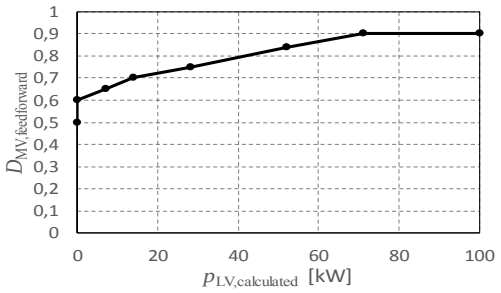

Fig.6. Profile of the look-up table used in control scheme No. III

The nonlinear feed-forward path introduced significant reduction in the $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$, see Fig. 10. It's initial value is well under control now. Up to t = 0.01s the DC current is within pk-pk range of -2 A to 1.4 A. After t = 0.01s the DC current is within pk-pk range of -16A to 11A. The remaining $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$ spikes are related to fast changes of the transformer current in response to the output voltage control actions. The spikes can by further reduced on expense of the control dynamics.

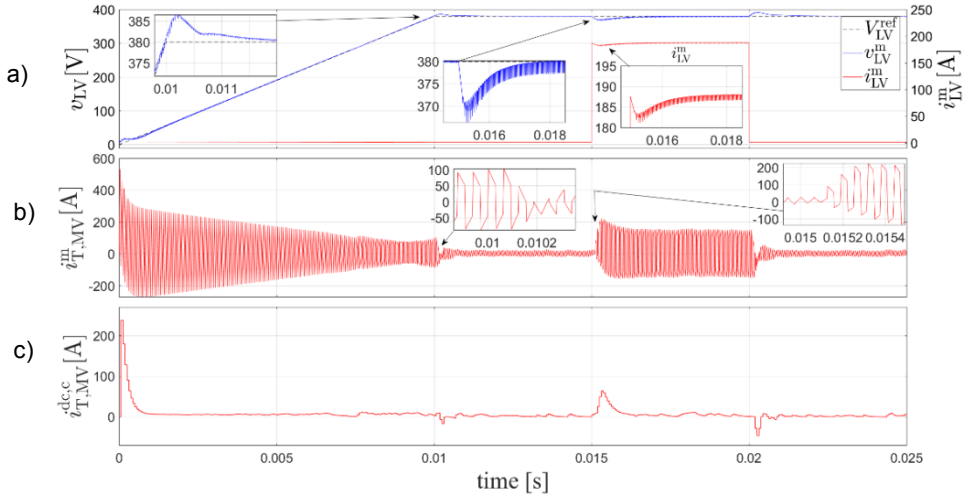

Fig.7. Selected SSTM voltages and currents under control scheme No. I, MOSFET $R_{\mathrm{DS,on}}$ = 55 mΩ and $R_{\mathrm{D,on}}$ = 8 mΩ, selector SL_2 from Fig. 5 in position 1 (only v_{LV} control), $V_{\mathrm{LV}}^{\mathrm{ref}}$ = 380 V, v_{MV} = 714 V, low voltage side load power cycle from $p_{\mathrm{LV}}^{\mathrm{min}}$ = 0.36 kW (0.5%) to $p_{\mathrm{LV}}^{\mathrm{max}}$ = 71.4 kW (100%) and to $p_{\mathrm{LV}}^{\mathrm{min}}$ at 0.015 s..0.02 s: a) output voltage reference $V_{\mathrm{LV}}^{\mathrm{ref}}$, measured output voltage $v_{\mathrm{LV}}^{\mathrm{m}}$, measured output current $i_{\mathrm{LV}}^{\mathrm{m}}$, b) measured transformer MV-side current $i_{\mathrm{T,MV}}^{\mathrm{m}}$, c) calculated DC-bias transformer current $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$ flowing through the L = 38 μH

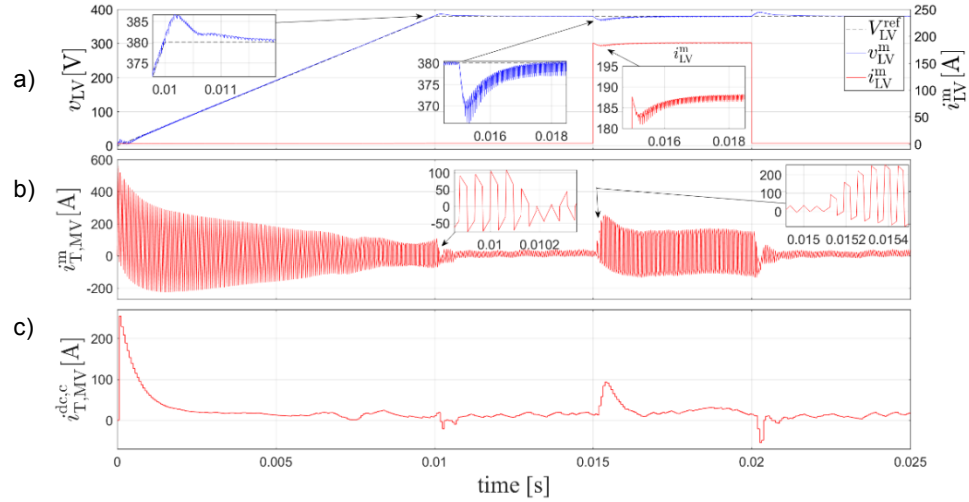

Fig.8. Selected SSTM voltages and currents under control scheme No. I, MOSFET $R_{\mathrm{DS,on}}$ = 5.5 mΩ and $R_{\mathrm{D,on}}$ = 8 mΩ, selector SL_2 from Fig. 5 in position 1 (only v_{LV} control), $V_{\mathrm{LV}}^{\mathrm{ref}}$ = 380 V, v_{MV} = 714 V, low voltage side load power cycle from $p_{\mathrm{LV}}^{\mathrm{min}}$ = 0.36 kW (0.5%) to $p_{\mathrm{LV}}^{\mathrm{max}}$ = 71.4 kW (100%) and to $p_{\mathrm{LV}}^{\mathrm{min}}$ at 0.015 s..0.02 s: a) output voltage reference $V_{\mathrm{LV}}^{\mathrm{ref}}$, measured output voltage $v_{\mathrm{LV}}^{\mathrm{m}}$, measured output current $i_{\mathrm{LV}}^{\mathrm{m}}$, b) measured transformer MV-side current $i_{\mathrm{T,MV}}^{\mathrm{m}}$, c) calculated DC-bias transformer current $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$ flowing through the L = 38 μH

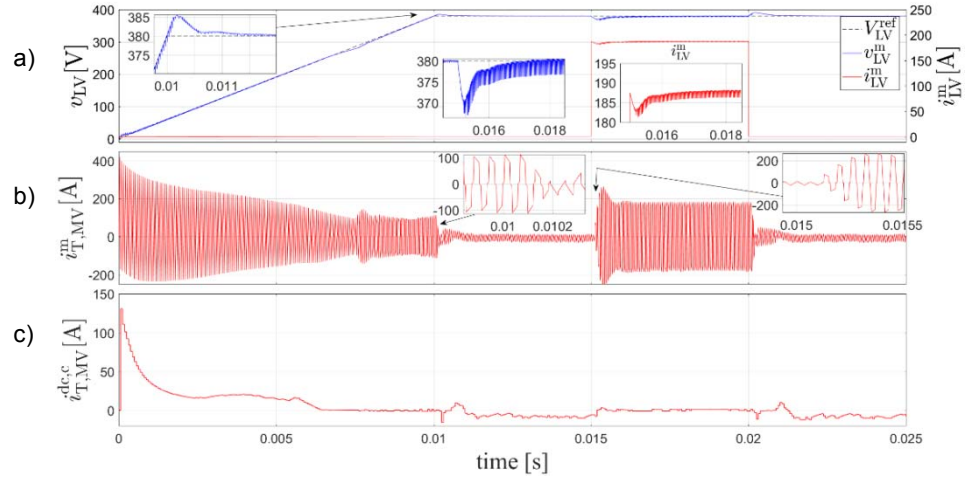

Fig.9. Selected SSTM voltages and currents under control scheme No. II, MOSFET $R_{\mathrm{DS,on}}$ = 5.5 mΩ and $R_{\mathrm{D,on}}$ = 8 mΩ, selector SL_2 from Fig. 5 in position 2 and SL_1 in position 2 (v_{LV} control and $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$ compensation with a PI compensator and feed-forward fixed duty cycle D_{MV} = 75%), $V_{\mathrm{LV}}^{\mathrm{ref}}$ = 380 V, v_{MV} = 714 V, low voltage side load power cycle from $p_{\mathrm{LV}}^{\mathrm{min}}$ = 0.36 kW (0.5%) to $p_{\mathrm{LV}}^{\mathrm{max}}$ = 71.4 kW (100%) and to $p_{\mathrm{LV}}^{\mathrm{min}}$ at 0.015 s..0.02 s: a) output voltage reference $V_{\mathrm{LV}}^{\mathrm{ref}}$, measured output voltage $v_{\mathrm{LV}}^{\mathrm{m}}$, measured output current $i_{\mathrm{LV}}^{\mathrm{m}}$, b) measured transformer MV-side current $i_{\mathrm{T,MV}}^{\mathrm{m}}$, c) calculated DC-bias transformer current $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$ flowing through the L = 38 μH

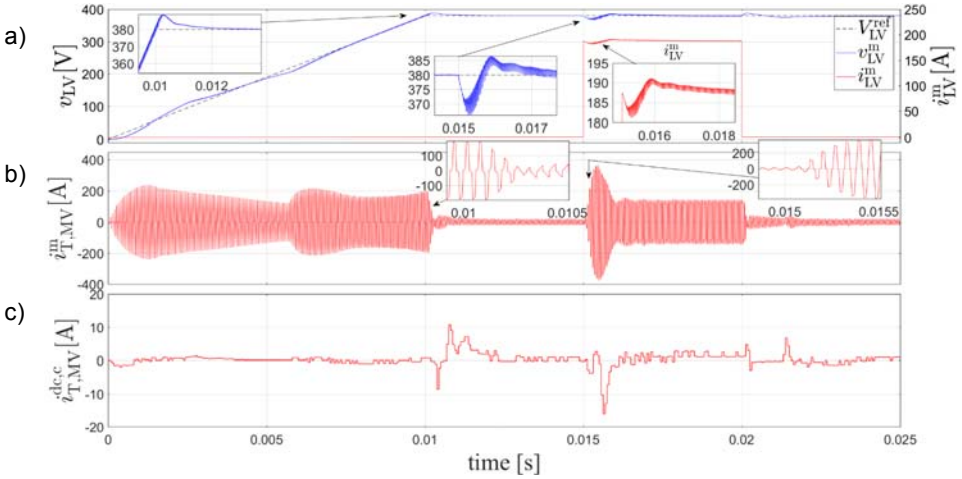

Fig.10. Selected SSTM voltages and currents under control scheme No. III, MOSFET $R_{\mathrm{DS,on}}$ = 5.5 mΩ and $R_{\mathrm{D,on}}$ = 8 mΩ, selector SL_2 from Fig. 5 in position 2 and SL_1 in position 1 (v_{LV} control and $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$ compensation with a PI compensator and nonlinear feed-forward function D_{MV} = f($p_{\mathrm{LV}}^{\mathrm{c}}$), $V_{\mathrm{LV}}^{\mathrm{ref}}$ = 380 V, v_{MV} = 714 V, low voltage side load power cycle from $p_{\mathrm{LV}}^{\mathrm{min}}$ = 0.36 kW (0.5%) to $p_{\mathrm{LV}}^{\mathrm{max}}$ = 71.4 kW (100%) and to $p_{\mathrm{LV}}^{\mathrm{min}}$ at 0.015 s..0.02 s: a) output voltage reference $V_{\mathrm{LV}}^{\mathrm{ref}}$, measured output voltage $v_{\mathrm{LV}}^{\mathrm{m}}$, measured output current $i_{\mathrm{LV}}^{\mathrm{m}}$, b) measured transformer MV-side current $i_{\mathrm{T,MV}}^{\mathrm{m}}$, c) calculated DC-bias transformer current $i_{\mathrm{T,MV}}^{\mathrm{dc,c}}$ flowing through the L = 38 μH

Table 1. Parameters of the DAB as SSTM

Parameter Name	Value
Input rated voltage, $V_{\mathrm{SSTM,MV}}^{\mathrm{rtd}}$	714 V
Output rated voltage, $V_{\mathrm{SSTM,LV}}^{\mathrm{rtd}}$	380 V
Input voltage tolerance, $V_{\mathrm{SSTM,MV}}^{\mathrm{tol}}$	±10 %
Output rated power, $P_{\mathrm{SSTM,LV}}^{\mathrm{rtd}}$	71.4 kW
Output minimum power, $P_{\mathrm{SSTM,LV}}^{\mathrm{min}}$	0.714 kW
Converter inductance, L	38 μH
Input capacitance, C_{MV}	100 mF
Output capacitance, C_{LV}	3.03 mF
Transformer turns ratio, n	2
Switching frequency, f_{s}	16 kHz
Assumed min efficiency, η_{SSTM}	85 %
Gate drive dead time, T_{dt}	0.5 μs

Conclusions

Control solutions for reduction of DC-bias current in Dual Active Bridge DC-DC converter have been proposed and analysed in this paper. Effect of low resistance in the current conducting path has been considered too.

Presented solutions have been derived basing on detailed simulation model.

A PI compensator combined with a nonlinear feed-forward path basing on a look-up table is recommended as a solution. Further analysis of the proposed solution will be carried on a prototype circuit which is under development.

***Authors**: dr inż. Radosław Nalepa, Politechnika Wrocławska, Wydział Elektryczny, Katedra Energoelektryki, Wybrzeże Wyspiańskiego 27, 50-370 Wrocław, E-mail: radoslaw.nalepa@pwr.edu.pl; dr inż. Marcin Zygmanowski, Politechnika Śląska, KENER, ul. B. Krzywoustego 2, 44-100, E-mail: marcin.zygmanowski@polsl.pl ; dr inż. Jarosław Michalak, Politechnika Śląska, KENER, ul. B. Krzywoustego 2, 44-100, E-mail: jaroslaw.miochalak@pol.sl.*

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