

Voltage-Mode First-Order Allpass Filter with Grounded Capacitor and Electronic Controllability

Abstract. A design and analysis of a voltage-mode first order allpass filter using the voltage differencing current conveyor (VDCC) is proposed in this paper. The synthesis of the proposed allpass filter is based on the connection of the voltage-mode lossy integrator and voltage-mode subtraction with single VDCC, single grounded capacitor and two resistors. The proposed filter is simple structure and grounded capacitor is attractive for integrated circuit implementation. The proposed circuit doesn't use the active building block with multiple output current output terminal which is easy the design by using commercially available IC. The phase response of the proposed first order allpass filter is electronically tuned via the DC bias current of VDCC. The proposed filter doesn't require the matching condition for simultaneously adjusting two parameters to control the phase response. The simulation results of the proposed filter are based upon the TSMC 0.18 μm CMOS process and $\pm 0.9\text{V}$ supply voltages.

Streszczenie. Przedstawiono projekt i analizę filtru pierwszego rzędu wykorzystującego układ VDCC, uziemioną pojemność i dwa rezystory. Odpowiedź fazowa jest łatwa do strojenia za pośrednictwem prądu. **Filtr napięciowy pierwszego rzędu z uziemionym kondensatorem i elektronicznym strojeniem**

Keywords: VDCC; Allpass filter; Electronic controllability.

Słowa kluczowe: układ VDCC (voltage differencing current conveyor), filtr pierwszego rzędu.

Introduction

The first-order allpass filter or well-known as phase shifter circuit is utilized to delay the sinusoidal output phase from the sinusoidal input phase with equal magnitude of the output signal for all operational frequency. For the first order allpass system, the phase of output waveform can be shifted from -180° to 0° or from 0° to 180° . It is also called as the phase shifter circuit. This filter is important in many analog signal processing systems for examples communication system, measurement and instrument system, biomedical system etc. [1]

There has been continuous increase in the design of electronic circuit using the active building block [2-8]. The well-known active building blocks are OPAMP, OTA and CCII. These active elements offer the flexibility and convenience to design the circuit by using minimum component count. The voltage differencing current conveyor (VDCC) [9] is interesting active element. It is electronically controllable active building block, where its transconductance gain (g_m) can be adjusted via DC bias current.

The VDCC based circuits have been introduced in the open literature. These circuits include sinusoidal waveform generator [10-13], capacitance multiplier [14], second order multifunction filter [15-18], inductance simulator [9, 19-20], ladder filter [21] and first order filter [22-23]. The first-order voltage-mode filter using z-copy controlled gain voltage differencing current conveyor (ZC-CGVDDCC) is presented in [22]. The circuit comprises single ZC-CGVDDCC and single grounded capacitor. The phase variation is electronically adjusted. However, this first-order filter requires the active building block with multiple output current terminals. Also, the internal construction of ZC-CGVDDCC looks complicated. Various first-order allpass filters using z-copy voltage differencing current conveyor (ZC-VDCC) are proposed in [23]. These circuits contain current-mode, mixed-mode and voltage-mode first order allpass filters. The proposed filters in Fig. 2, 3, 4, 5 and 7, require single ZC-VDCC and single capacitor. Figure 6 comprises of a ZC-VDCC, a capacitor and grounded resistor. Figure 8 consists of one ZC-VDCC, one capacitor and one inverting voltage buffer. Figure 9 requires one ZC-VDCC, one capacitor and two resistors. The phase response is electronically controlled. However, these first-order filters require ZC-VDCC with multiple output current

terminals. Some circuits (Figs. 6-8) use floating capacitor. Also, the filters in Figs. 2, 3, 4, 7 and 9, need matching condition during adjusting the phase response (simultaneously adjusting two parameters for controlling the phase response).

This contribution presents the circuit topology of simple voltage-mode first-order allpass filter employing VDCC as active element. The proposed filter uses one grounded capacitor, two resistors and one VDCC. The angle phase of the voltage output signal can be electronically adjusted via bias current. The proposed first-order allpass filter is verified with Pspice simulation with 0.18 μm TSMC CMOS process parameters to confirm the theory. The given results agree well with theoretical expect.

Theory and Principle

Basic Concept of VDCC

Voltage differencing current conveyor (VDCC) is the active building block used in this design. The principle of VDCC is firstly proposed by Biolek, et al. [8]. Later, the CMOS internal construction of VDCC and its application are proposed by Kacar, et al. [9]. This active device is composed of a transconductance amplifier (OTA) and second generation current conveyor (CCII). The p and n circuit symbol of VDCC is illustrated in Fig. 1(a). The x terminal is the low impedance output voltage port. The z and w terminals are the high impedance input voltage port. In this design, it is required only single w terminal. The DC bias current I_B is employed to adjust the transconductance (g_m) of VDCC. The electrical behaviour for each terminal of VDCC is characterised by

$$(1) \quad \begin{pmatrix} i_n \\ i_p \\ i_z \\ v_x \\ i_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} v_p \\ v_n \\ v_z \\ i_x \end{pmatrix}$$

The implementation of CMOS VDCC is shown in Fig. 1(b). With this structure, the transconductance is given as

$$(2) \quad g_m = \sqrt{\mu_n C_{ox} (W/L) I_B}.$$

where μ is the effective channel mobility. C_{ox} is the gate oxide capacitance per unit area. W is the channel width and L is the channel length [18].

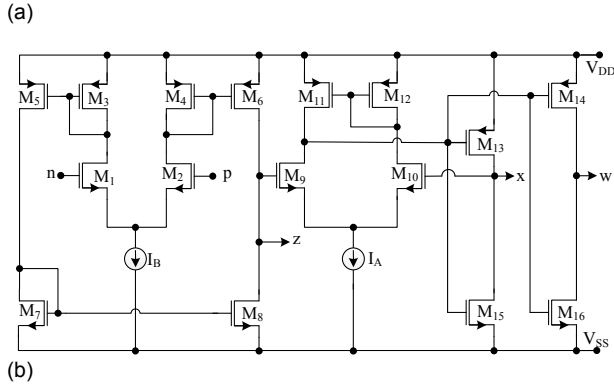
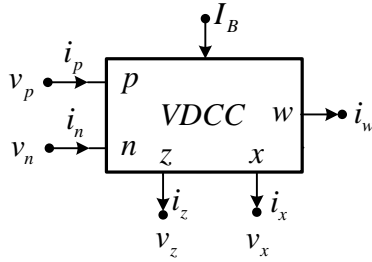


Fig. 1. VDCC (a) Symbol (b) CMOS internal construction

Proposed Voltage-Mode Filter

A simplified schematic of the proposed voltage-mode first order allpass filter with single VDCC, one grounded capacitor and two resistors is shown in Fig. 2. The synthesis of the proposed filter is based on the connection of the voltage-mode lossy integrator and voltage-mode subtraction. Performing a routine analysis and using Eq. (1), the voltage transfer function of the circuit in Fig. 2 is express as

$$(3) \quad H(s) = \frac{v_{out}}{v_{in}} = \frac{R_2}{R_1} \left(\frac{g_m}{sC + g_m} \right) - \frac{R_2}{R_1} + 1.$$

According to Eq. (3), if $R_2 = 2R_1$, the voltage transfer function of the proposed circuit has the following form

$$(4) \quad H(s) = \frac{v_{out}}{v_{in}} = \frac{g_m - sC}{g_m + sC}.$$

As seen in Eq. (4), the proposed circuit is the first-order system. If $s = j\omega$, the magnitude of the voltage gain is found as

$$(5) \quad H(\omega) = \left| \frac{v_{out}}{v_{in}} \right| = 1.$$

The phase variation is given as

$$(6) \quad \theta(\omega) = -2 \tan^{-1} \left(\frac{\omega C}{g_m} \right).$$

Substituting the transconductance as appeared in Eq. (2) into Eq. (6), the phase variation of the proposed circuit is given by

$$(7) \quad \theta(\omega) = -2 \tan^{-1} \left(\frac{\omega C}{\sqrt{\mu_n C_{ox} (W/L) I_B}} \right).$$

It is evident that the phase variation is electronically adjusted with constant amplitude. The electronic controllability of the proposed circuit is convenient for controlling by microcontroller or microcomputer which is the requirement for modern circuit systems [24-25]. Also during the tuning of the phase variation, the matching donation of the bias current is not required.

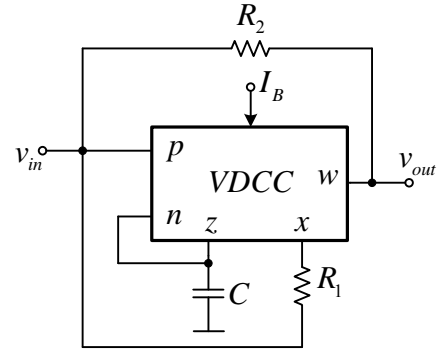


Fig. 2. Proposed filter

Non-Ideal Analysis

Taking the influent of various non-ideal port-transfer ratios of VDCC into account, the relationship of the port voltages and currents of VDCC can be rewritten as:

$$(8) \quad \begin{pmatrix} i_n \\ i_p \\ i_z \\ v_x \\ i_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \alpha \end{pmatrix} \begin{pmatrix} v_p \\ v_n \\ v_z \\ i_x \end{pmatrix}.$$

where $\beta (\beta = 1 - \varepsilon_v)$ represents the voltage gain error from x to z terminal, $\alpha (\alpha = 1 - \varepsilon_c)$ represents the current gain error from x to w terminal. ε_v is the voltage tracking error and ε_c is the current tracking error where $\varepsilon_v \ll 1$ and $\varepsilon_c \ll 1$. Taking these voltage and current gain errors into account, the voltage transfer function of Fig. 2 becomes

$$(9) \quad H(s) = \frac{v_{out}}{v_{in}} = \beta \alpha \frac{R_2}{R_1} \left(\frac{g_m}{sC + g_m} \right) - \alpha \frac{R_2}{R_1} + 1.$$

According to Eq. (3), if $R_2 = 2R_1$, the voltage transfer function of the proposed circuit has the following form

$$(10) \quad H(s) = \frac{v_{out}}{v_{in}} = \frac{2\alpha g_m (\beta - 1) + g_m - sC (2\alpha - 1)}{g_m + sC}.$$

Subsequently, if $s = j\omega$, the magnitude of the voltage gain is found as

$$(11) \quad H(\omega) = \left| \frac{v_{out}}{v_{in}} \right| = \sqrt{\frac{[2\alpha g_m (\beta - 1) + g_m]^2}{C^2 (2\alpha - 1)^2} + \omega^2}}{\left(\frac{g_m}{C} \right)^2 + \omega^2}}.$$

The phase variation is given as

$$(12) \quad \theta(\omega) = -\tan^{-1} \left[\frac{\omega C(2\alpha - 1)}{2\alpha g_m(\beta - 1) + g_m} \right] - \tan^{-1} \left(\frac{\omega C}{g_m} \right).$$

The voltage and current gain errors affect both the voltage gain and phase variation.

Simulation Results

The proposed circuit in Fig. 2 based on the CMOS VDCC instruction in Fig 1(b) is designed and simulated using LEVEL 7 Pspice parameters from TSMC 0.18 μ m [26]. The width (W) and length (L) of the PMOS and NMOS transistor are listed in table 1. The bulk terminal of all NMOS transistors is connected to V_{SS} while the bulk terminal of all PMOS transistors is connected to V_{DD} . The voltage power supplies and DC bias current are set to $V_{DD} = -V_{SS} = 0.9$ V, $I_A = 100$ μ A, and $I_B = 24.5$ μ A. With these conditions, the simulated properties of VDCC are as follows: $g_m = 207$ μ A/V, $\beta = 0.999$ and $\alpha = 0.994$. The circuit is designed to have the 90° phase difference of input and output signal at 1 MHz frequency, with $I_B = 24.5$ μ A, $C = 33$ pF, $R_1 = 5$ k Ω and $R_2 = 10$ k Ω . With these values of active and passive elements, the simulated power consumption is 0.492 mW. The variation of magnitude and phase with respect to frequency is shown in Fig. 3. The simulated magnitude and phase at 1MHz frequency are - 87.58°, 0.203dB, respectively. Besides, the phase response can be tuned electronically by bias current as shown in Fig. 4. In this result, the bias current, I_B is changed to 10 μ A, 20 μ A and 40 μ A. The phase angle at 1MHz frequency is located at - 114.09°, - 93.64° and - 75.82°, respectively.

Table 1. W/L of the MOSFET in the VDCC [8]

Transistor	W (μ m)	L (μ m)
M1-M4	3.6	1.8
M5-M6	7.2	1.8
M7-M8	2.4	1.8
M9-M10	3.06	0.72
M11-M12	9	0.72
M13-M14	14.4	0.72
M15-M16	0.72	0.72

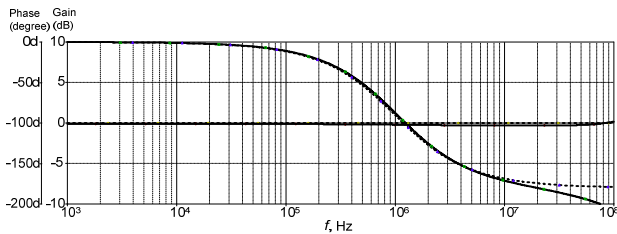


Fig.3. Simulated magnitude and phase response of the proposed filter.

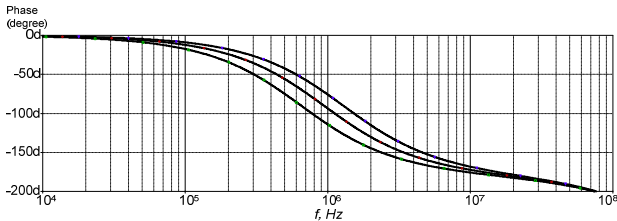


Fig.4. Varying phase response by changing the bias current.

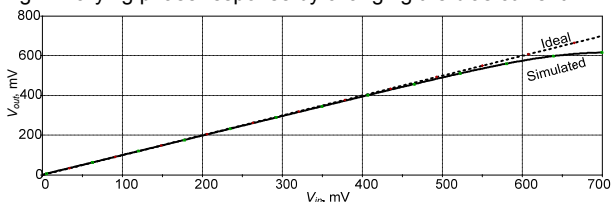


Fig.5. Linearity of the proposed filter against input voltage

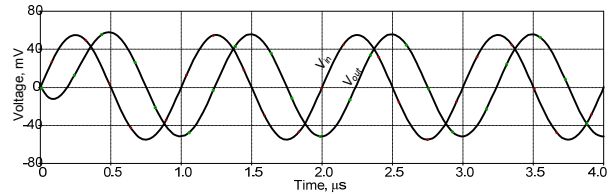


Fig.6. Output and Input waveforms at 1MHz frequency

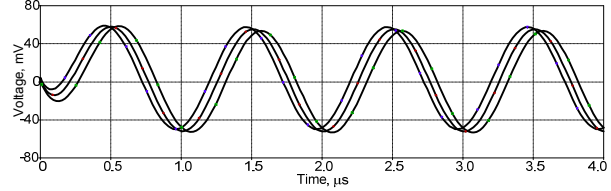


Fig.7. Output waveform for different I_B values

The DC transfer characteristic of the proposed first allpass filter is shown in Fig. 5. It is indicated that the proposed filter works well when apply the magnitude of input voltage below 550mV. The simulated time domain response in Fig. 6 is the input and output waveform where the sinusoidal voltage signal with 55mV_p, f=1MHz, is applied as input. Also, the output waveform for different I_B values is illustrated in Fig. 7. THD analysis of the proposed filter given in Fig. 8 is performed at 1 MHz for various sinusoidal peak input voltages.

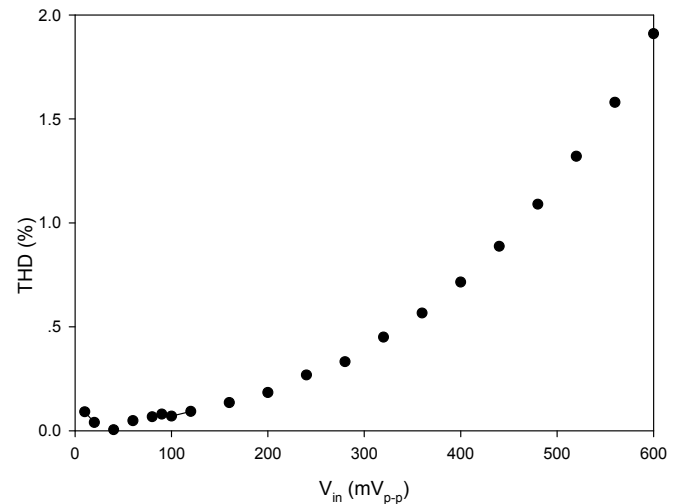


Fig.8. THD against peak value of the applied sinusoidal signal at 1 MHz frequency.

Conclusions

The proposed first order voltage-mode allpass filter based on VDCC is implemented using 0.18 μ m TSMC CMOS process. The circuit realization employs one VDCC, one grounded capacitor and two resistors. The proposed filter offers a variable phase response through the electronically tunable bias current of VDCC. The proposed filter is simulated by Pspice program. The proposed filter consumes a power of 0.492mW from ± 0.9 V power supply.

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