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Analogue part of multichannel highly productive analog-digital system on converters and switches of current

***Abstract**. A method for structurally-functional organization of an analog part of a highly productive ADC is proposed. In this method the primary transformation and commutation of signals in channels is performed over currents. The possibility of implementing the required analog units for primary conversion channels of input electrical signals from sensors is analyzed. Analytical relations connecting the values of input and output electrical quantities are obtained.*

Streszczenie.** Zaproponowano metodę strukturalno-funkcjonalnej organizacji części analogowej wysoko wydajnego ADC. W tej metodzie pierwotna transformacja i komutacja sygnałów w kanałach odbywa się nad prądami. Analizowana jest możliwość implementacji wymaganych jednostek analogowych dla pierwotnych kanałów konwersji wejściowych sygnałów elektrycznych z czujników. Uzyskane zostają zależności analityczne łączące wartości wejściowych i wyjściowych wielkości elektrycznych. **(Analogowa część wielokanałowego, wysoce wydajnego systemu analogowo-cyfrowego na konwerterach i przełącznikach prądu).

Keywords: analog-digital systems, primary conversion channels, voltage-to-current converters, current-to-current converters.
Słowa kluczowe: systemy analogowo-cyfrowe, pierwotne kanały konwersji, konwertery napięcia do prądu, konwertery prądu do prądu.

Introduction

Analog-to-digital systems (ADS) are used to solve a wide class of problems in the measurement, signal recording and processing technique. Depending on the application area, they are subject to various requirements for accuracy, speed and productivity. For example, in measuring systems, a high absolute accuracy of the analog-to-digital conversion is sometimes required, and in the registration systems, a low linearity error is sufficient. Similarly, the primary analog signal in many sensors is converted to digital output signal using electronic circuits for signal processing and conditioning, incorporated into the sensor (i.e. the temperature and humidity sensors [1]) Regarding the same requirements for speed, they are determined by the spectra of the input analog signals and the possibility of their reproduction with minimal losses. In a number of cases, it is advisable to use such a complex characteristic as productivity. The basic unit of these systems is an analog-to-digital converter (ADC). Currently, there are basically three types of ADCs [2]: sigma-delta, pipelined and successive approximation. It should be noted that the first have high resolution, but their speed is relatively small [3, 4]. The highest speed is characterized by pipelined converters, but they have a sufficiently high power consumption and circuit complexity. Successive approximation ADCs have a significant productivity range and it can be further increased by introducing, for example, a weight redundancy [5, 6].

Relevance

Quantitatively, the performance of the ADC can be estimated by analogy with digital computing devices [7], as the product of the display range (the length of the bit grid) by the frequency of the operations performed. For the ADC (part of the ADS), this will correspondingly be the product of the resolution of the analog-to-digital conversion (the number of conversion quanta) to the maximum frequency of execution of the conversions. It is known that the performance of successive approximation ADCs with weight redundancy [3,4] is higher than traditional binary ones, since they can have a significantly shorter conversion time and therefore a higher conversion frequency. However, this is a separate topic of research and we will not consider it in the article.

As for the whole ADS, an additional reserve for increasing the speed (and performance, respectively) is the analog part of the system, which is a part of the so-called sampler [8]. In fact, these are the primary converters of the input signal in conjunction with the switch. Their parameters such as accuracy and switching frequency also are instrumental in increased performance. In connection with this, it is important to select the basic signal carrier in the analog part.

It is known that [9,10] current converters have certain advantages in comparison with converters built on voltage amplifiers. There are two aspects here. First, most of the parasitic parameters of integrated circuits are capacities, as a result of which it is expedient to carry out the amplification operations precisely over currents, and not voltages. In this case, it is possible to avoid the appearance of large voltage drops on the capacitances and to increase the speed. The second: reduction of voltage drops on the electrodes of bipolar transistors (especially collector-emitter transitions) of the converter circuits will help to reduce the linearity errors of the conversion characteristics. Finally, current switches, in particular, that build on diode switches are simpler and faster.

At the same time, it should be noted that the issue of constructing an analog part of the ADS on current converters is quite rare in scientific and technical literature, so the topic of the article devoted to the construction of an analog part of multichannel and high-performance ADS on converters and current switches is relevant.

The purpose of the research is to increase the performance of multichannel ADCs by implementing the analog part on high-linear amplifiers and converters, in which the signal carrier is a current, with the additional possibility of its high-speed commutation.

Objectives of the research

1. Consider the proposed method of structural and functional organization of the analog part of a high-performance ADC, in which primary transformations and commutations in channels are performed over currents.
2. Analyze the feasibility of implementing analog units for primary conversion channels of input electrical signals from sensors on voltage-to-current (VCC), current-to-current

(CCC) converters with subsequent switching of currents at their outputs.

3. Obtain analytical relationships that bind the values of input and output electrical quantities for the VCC and CCC, as well as analog units of the system successive approximation analog-digital converter.

Solution of tasks

Depending on the functions that the ADS should perform, it can contain a different number of channels for the primary transformation of sensor signals, and specific requirements for accuracy, speed, and other characteristics are formulated to the channels themselves. The fulfillment of these requirements largely depends on the capabilities of the analog part. For example, to improve accuracy and speed, it is advisable to implement the conversion, amplification and switching of electrical signals presented in the form of currents.

In this case, we can formulate a method for determining the structure-functional organization of the analog part of a multi-channel high-performance ADS as follows:

determine the feasibility and technical possibilities of obtaining from the signal sensor (SS) (which usually works with non-electrical quantities) an electrical signal in the form of voltage or current;

if such signal is a voltage, then it is necessary to solve the problem of it further high-precision conversion into a current and use for this a voltage-current converter (VCC);

estimate the output resistance of the SS, as well as the range of its output signal change, then determine what function the sensor mainly performs, namely the voltage or current generator;

if it is a voltage generator, then it is necessary to introduce the VCC into the circuit; if it is a current generator, it is advisable to connect its output directly to the CCC with the desired transfer factor;

provide the possibility of commutating the output current of the VCC with the help of high-speed switch elements and supplying a difference current to the input of the successive approximation ADC with accelerated conversion;

A generalized block diagram of a multichannel high-performance ADS is shown in Fig. 1. It contains the actual analog part, together with the successive approximation ADC, which is self-correcting (SADC), a memory device (MD), a digital computing device (DCD) and a control unit (CU) that provides the functioning of the system as a whole.

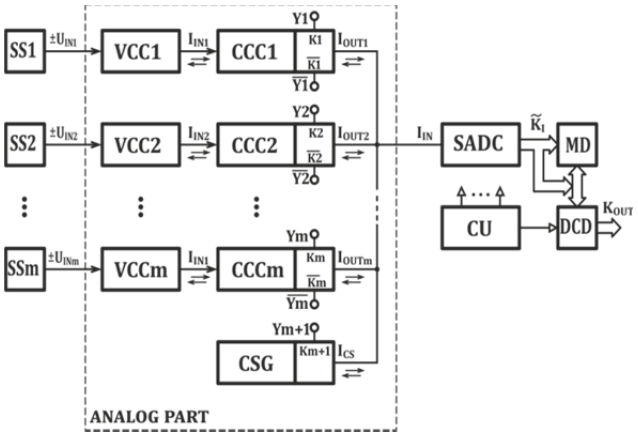

Fig. 1. Structural diagram of multichannel ADS

In its turn, the analog part of the system consists of m CCC, and if necessary of m VCC, which are connected to m signal sensors and a calibration signal generator (CSG). Each CCC contains 2m switch elements providing switching of the output amplified currents I_{OUT1}, I_{OUT2}, …, I_{OUTm}, I_{CS} and their serial connection to the input of the SADC. The SADC is a successive approximation analog-to-digital converter with a weight redundancy [3, 4, 12], which has an increased speed and the ability to self-correct the bits weights of the DAC included in it. The encoding results in the form of K_I codes are stored in a memory device (MD). The digital computing device processes the received information according to the specified program. In the self-correcting mode, the I_{CS} current from the CSG by the K_{m+1} switch is connected to the input of the SADC [13, 14, 15].

The functional diagrams of the primary conversion channels are shown in Fig. 2. If the SS acts as a voltage generator, it is advisable to use a channel with a VCC, the circuit of which is shown in Fig. 2a. It contains a voltage buffer (VB), a current-to-current converter (CCC) with an output signal commutator on the diode switches. In this case, the input voltage $\pm U_{IN}$ is converted to the current I_{IN}, which from the VB output through the resistor R^*_{SC} goes to the CCC input. Further, this current is amplified and split into two components I'_{OUT} and I''_{OUT}, which are commutated by the switch elements that are controlled by the digital signals with opposite phases Y and $\overline{Y}$. Thus, an output current:

$$I_{OUT} = I'_{OUT} - I''_{OUT}, \quad (1)$$

which is applied to the input of the DAC. The result of the analog-to-digital conversion is formed as a code $\tilde{K}_I$.

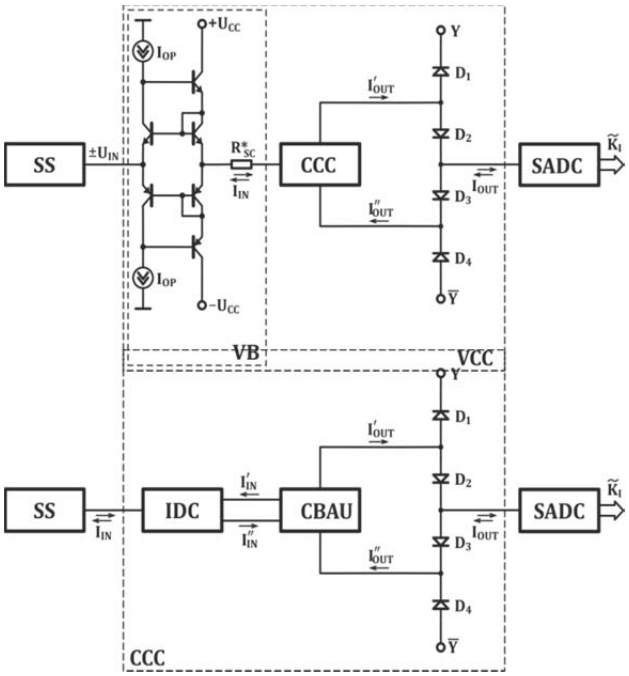

Fig. 2. Structurally-functional organization of ADS conversion channels for different types of input signal generators (SS): voltage and current

In the event that the source of the input signal is a current generator, it is necessary to apply the circuit shown in Fig. 2b. It contains a CCC consisting of an input push-pull cascade (IPPC), current balancing and amplification unit (CBAU), and an output currents switch. In this case, I_{IN} splits into two components I'_{IN} and I''_{IN}, which are amplified by CBAU to the required level I'_{OUT} and I''_{OUT}, switched and in the form of I_{OUT} are applied to the input of the SADC.

Let us consider in more detail the basic analog units of the ADS. The functional scheme of the CCC with current switches is shown in Fig. 3a.

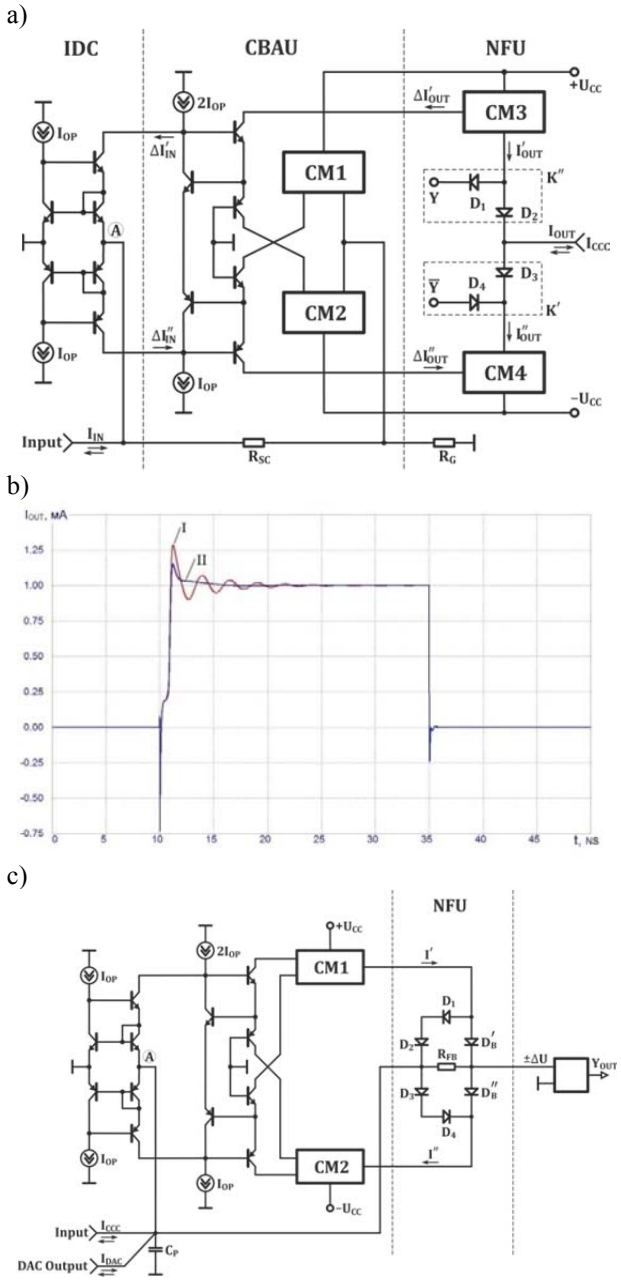

Fig. 3. Analog units of ADS: a) functional circuit of the CCC with a current switch; b) the transient characteristics of the CCC with the current switch I – K_{TI} = 2, II – K_{TI} = 20; c) a preamplifier (current-voltage converter) for VC of ADC

It contains a input differential cascade (IDC) with a low input resistance, whose value for a small-signal zone is approximately equal to the resistance of the emitter junction of transistors

$$r_{IN} = r_E + \frac{r_B}{1+\beta} = \frac{\varphi_T}{I_{OP}} + \frac{r_B}{1+\beta}, \quad (2)$$

where: r_E is the emitter resistance, I_{OP} is the operating current, φ_T is the thermal potential, r_B is the base resistance, and β is the current amplification factor of the base. It should be noted that r_B and β depend on the type of transistors, and r_E on the value of I_{OP} and the temperature of the crystal. In the case of using NUHFARRY integral transistors [10] and setting I_{OP} = 1mA, r_E ≈ 26-27 Ohm at normal temperature. The coefficients K_I' and K_I'' of the small-signal increments $\Delta I_{IN}'$ and $\Delta I_{IN}''$ are equal [12]:

$$K'_I = K''_I = \frac{\beta' \cdot \beta'}{\beta' \cdot \beta'}, \quad (3)$$

where β' and β'' are the low-signal current transfer coefficients for the n-p-n and p-n-p transistors, respectively. To generate output currents with the desired directions, the current mirrors CM1-CM4 are applied in the circuit. The current gain of the CCC in case of the presence of deep feedback is

$$K_{TI} = \frac{R_{SC} + R_G}{R_G}, \quad (4)$$

where R_{SC} and R_G are the resistors of the negative feedback loop. Thus, the K_{TI} value is determined by the ratio of R_{SC} and R_G. Dynamic properties of CCC should be investigated by computer simulation. The graphs of the transient characteristics for different values of the K_{TI} and for the connection of the I_{OUT} to the low-resistance load R_L = 100 Ohm are shown in Fig. 3b.

Analysis of the results shows that the speed of the CCC is quite high. The rate of increase (at the level of 0.9) is not less than 500 V/μs.

An important role in improving the productivity of the ADS acts the construction of a preamplifier for the voltage comparator (VC) of the SADC. This is due to the presence at its input of parasitic capacitance C_P, the value of which depends on the number of channels. To reduce its negative influence on the input of the VC, it is necessary to use a high-speed current-voltage converter with a low input resistance. Such requirements are met by the scheme shown in Fig. 3c. The circuit contains a two-stage balanced direct current amplifier with paraphase outputs and a nonlinear feedback unit (NFU). The NFU is realized in the form of a current bridge built on diodes D_1-D_4 (a separate block is shown in Fig. 4a, a variant of the block with a current bridge built on six diodes D_1-D_6 is shown in Fig. 4b). In this case, the bias diodes D_B' and D_B'' determine the operating points of the arms of the bridge in such a way that for | I' | > | I" | the diodes D_1 and D_2 are opened, and D_3 and D_4 are closed, if | I' | < | I" |. In the low-signal zone, when | I' | ≈ | I" ||, the resistances of these diodes are sufficiently large and the value of the voltage increase at the input of the VC is:

$$\Delta U = \left(I_{CC} - I_{DAC}\right) \cdot R_{FB}, \quad (5)$$

where I_{DAC} is the output current of the code-to-current converter (DAC), R_{FB} is the feedback resistance.

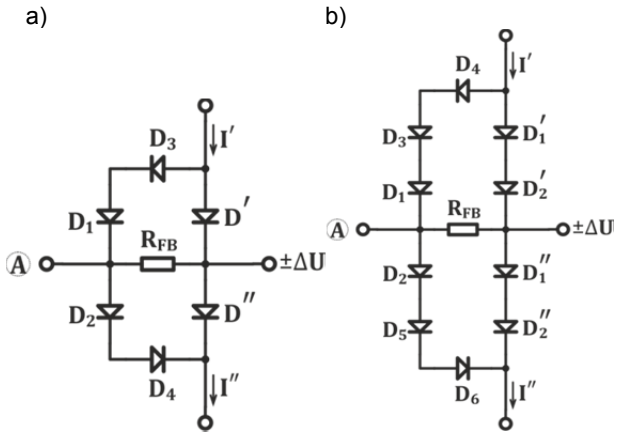

Fig. 4. Unit of nonlinear feedback: a) schematic diagram with two D_B; b) a schematic diagram with four D_B

The goal of NFU is to limit the voltage gain $\pm \Delta U$ at the input of the VC, when the input difference current $\Delta I = I_{CCC} - I_{DAC}$ at the beginning of the balancing process in the SADC is significantly larger (by degrees of magnitude) than at the end. At the same time, at the lower coding cycles, the ΔI level is small and ΔU can be increased for normal operation of the VC only by adjusting R_{FB}. In this case, the parasitic capacities of the NFU diodes tighten the transient processes at the output of the circuit. The paired serial connection of the diodes D_1, D_2 and D_3, D_4 (Fig. 4a) halves the total capacitance in the nonlinear feedback loop and improves the situation somewhat, and the use of six D_1-D_6 diodes (Fig. 4b) allows to reduce the capacity threefold.

Let's estimate the dependence $\Delta U = f(\Delta I)$, where $\Delta I = I' - I''$. Note that for $\Delta I = 0$ the diode bridge is balanced and $U_{D1} = U_{D2} = U_{D3} = U_{D4} \approx (U'_{DB} + U''_{DB}) / 4$. If $| I_{CCC} | \neq 0$, then the bridge is unbalanced and in the case of $| I' | > | I'' |$

(6) $$\Delta U = \Delta U_{D1} + U_{D2} = 2\varphi_T \cdot l \cdot n \frac{\Delta I}{I_D},$$

Where: I_D is the current through D_1 and D_2 at $\Delta I = 0$. In the case of a change ΔI in direction, we have:

(7) $$\Delta U = -2 \cdot \varphi_T \cdot l \cdot n \frac{\Delta I}{I_D},$$

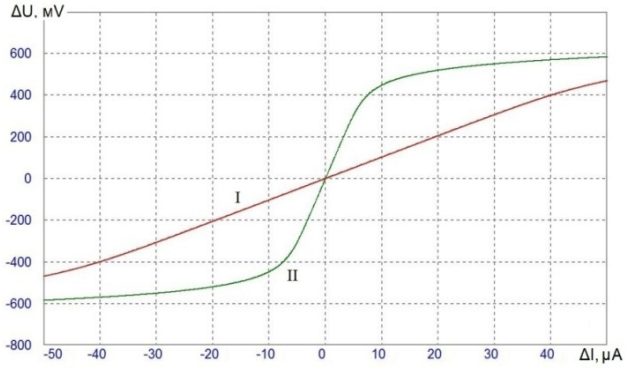

Fig. 5. Static characteristics $\Delta U = f(\Delta I)$, $I - R_{FB}$ = 10 kOhm, II – R_{FB} = 100 kOhm

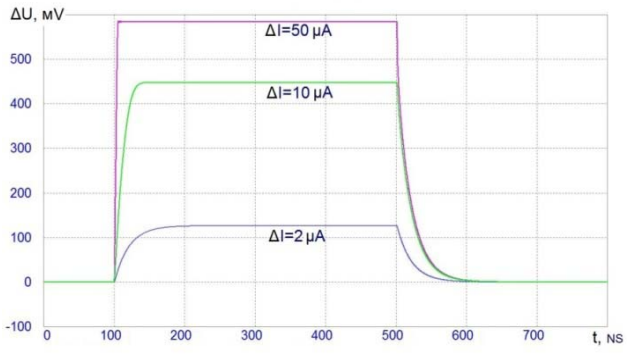

Fig. 6.Dynamic characteristics $\Delta U = f(t)$, for different ΔI.

Graphs of the dependences $\Delta U = f(\Delta I)$ and $\Delta U = f(t)$ (for a given ΔI) obtained by computer simulation using the Microcap 11 integrated package are shown in Fig. 5 and Fig.6. In this case, the analysis of the static characteristic (Fig. 5) shows that for small ΔI level of ΔU completely depends on the value of R_{FB}. At the same time, if ΔI increases, the growth of ΔU slows down significantly, and the maximum value for curve I does not exceed $\Delta U_{MAX} \leq 0.6$V, for curve II it is even smaller - $\Delta U_{MAX} \leq 0.45$V. This avoids overloading the VC and keeps its speed. The dynamic characteristics (Fig. 6), in particular, the settling time of ΔU also depend significantly on ΔI. At small ΔI (0.1 μA), the transient process is prolonged, for large ΔI (10 μA) the transient process is accelerated.

Let's analyze the productivity gain for the considered ADS. Note that it largely depends on the speed of the applied ADC. Thus, the conversion time, depending on the level of the weight redundancy, can be 5 ÷ 10 times less than for the classical binary ADC with the same resolution. Thus, the frequency of sampling increases by 5 ÷ 10 times. This indicator can still increase if the redundancy is increased, but this requires additional equipment and it is advisable to make the final decision after solving the optimization problem. Within the framework of the above, the element base of the analog part of the ADC, in particular, of the primary conversion channels must be selected in such a way that the speed of the secondary conversion, which is potentially set by the system ADC, is not reduced.

Conclusions

1. The proposed method for determining the structural and functional organization of the analog part of high-performance ADS, in which the current is used as a signal carrier in order to improve the speed of linear units, is considered.
2. The static and dynamic characteristics of the considered current-to-current converters, voltage-current and current-voltage converters are analyzed. The schemes of commutation of the currents at the output of the CCC are considered, which in aggregate form the system switch of the ADS, the speed of which slightly depends on parasitic capacitances.
3. Analytical relations are obtained that connect the values of the input and output electrical quantities of the VCC, CCC and CVC. The adequacy of the mathematical relations obtained for the case of use integral bipolar transistors has been proved by computer modeling.

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