Krzysztof Cyprian NOWASZEWSKI, Andrzej SIKORSKI

Bialystok University of Technology

doi:10.15199/48.2019.08.34

Application of GaN HEMT as a bidirectional switch in matrix converter

***Abstract**. This paper presents a study of the GaN HEMT as a bidirectional switch. The considerations were conducted for the purpose of application of bidirectional switch in a matrix converter. Semi-soft 4-step commutation method was analysed and laboratory tested on the 2-phase to 1-phase converter to verify all the possible commutation processes which occur in a matrix converter. The problem of wrong sign of current detection and output current interruption has also been raised.*

***Streszczenie.** Artykuł przedstawia badania GaN HEMT jako łącznika dwukierunkowego. Rozważania były prowadzone w celu zastosowania łącznika dwukierunkowego w przekształtniku matrycowym. Metoda 4-krokowej półmiękkiej komutacji została przeanalizowana i przebadana laboratoryjnie na przekształtniku 2-fazowym na 1-fazowy, który odwzorowuje wszystkie procesy komutacyjne w przekształtniku matrycowym. Został również poruszony problem błędnej detekcji znaku prądu wyjściowego oraz jego przerwania. (**Zastosowanie GaN HEMT jako łącznika dwukierunkowego w przekształtniku matrycowym**)*

Keywords: matrix converter, bidirectional switch, GaN, semisoft commutation
Słowa kluczowe: przekształtnik matrycowy, łącznik dwukierunkowy, GaN, półmiękka komutacja

Introduction

In power electronics, bidirectional (four-quadrant) switches (BDS) are a necessary part of all matrix converters which allow to convert AC voltage directly (without a DC link) to AC voltage with controllable amplitude and frequency. BDS are capable to conduct current in both directions and block voltage of both polarities. There are several configurations of BDS but the most commonly used is antiparallel connection of two RB-IGBT and its main advantage is that the current is passing only through one semiconductor [1]. Nowadays, GaN BDS begin to appear as a single package device with dual gate and are used in matrix converters (MC), e.g. [2, 3], but they are still not available on the market. GaN HEMT could be a competition for RB-IGBT due their lower switching and conduction losses, their high frequency operation which could increase the power density of MCs [3]. GaN HEMT connected in series has not yet been tested as a BDS which was the main reason to conduct the research.

I. Four-step semisoft current commutation method

A. Analysis

The 4-step semisoft current commutation method for BDS was firstly proposed in [4]. It is called semisoft, because half of the commutation process is soft switching and half is hard switching [1]. There are many other modifications of that method, e.g. 3-step, 2-step. [5] which are the modification of the 4-step method. To analyse all the commutation processes in a 3-phase MC it is enough to consider only a 2-phase to 1-phase (2f/1f) converter with a DC voltage source and RL load (Fig.1). RC snubbers added to each GaN HEMT significantly reduce the voltage ripple [6], (it is worth mentioning that in [2] for GaN BDS an RCD snubber with 4 diodes, resistor and capacitor is proposed, which could be compared in future work).

Control strategy of the 4-step current commutation method is shown in Table 1. For example, if we want to switch from conducting T_{Aa} to open T_{Ba} BDS and the current of the RL load is greater than zero, the switching order from column $T_{Aa} \rightarrow T_{Ba}$ with $I_a > 0$ should be selected. A "1100" = "$T_{Aa1}T_{Aa2}T_{Ba1}T_{Ba2}$" state means that T_{Aa1} and T_{Aa2} transistors are closed ("1"), T_{Ba1} and T_{Ba2} are opened ("0"). In the first step the transistor T_{Aa2} should be turned off, in the second T_{Ba1} turned on, in the third T_{Aa1} is turned off and in the fourth T_{Ba2} is turned on. For switching under different conditions a correct column should be selected and the switching process is analogous to that described above. For this same sign of current, the sequence of switching process is exactly the same.

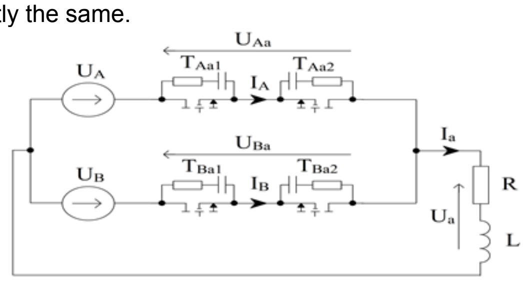

Fig.1. Scheme of 2-phase to 1-phase converter with 2 BDS GaN HEMT connected in series with a common source and RL load

Table 1. Four-step semisoft current commutation for 2f/1f converter

Direction of switching order	Step	$T_{Aa} \rightarrow T_{Ba}$ (Sequence 12)		$T_{Aa} \leftarrow T_{Ba}$ (Sequence 21)	
		$I_a > 0$	$I_a < 0$	$I_a > 0$	$I_a < 0$
↓	Initial	1100	1100	0011	0011
	1st	1000	0100	0010	0001
	2nd	1010	0101	1010	0101
	3rd	0010	0001	1000	0100
	4th	0011	0011	1100	1100

B. Simulation studies

Firstly, in order to verify the presented commutation method in a 2f/1f converter simulation studies with the use of an LTspice simulator and the manufacturer (Gan Systems Inc.) spice model of GS66506T transistor which include thermal behaviour and parasitic inductance of leads (around 0.2nH). Also, to reflect a more realistic scenario parasitic inductance of the PCB layers Ls = 40nH has been added at the source and drain terminal, because the GaN HEMT switches current with very high *di/dt* (even 10^9) which is the reason of overvoltage. To simulate the turn-on process of BDS in all its four quadrant current-voltage characteristic two variants of U_A and U_B need to be considered.

The work of BDS in the I and II quadrant could be obtained e.g. when U_A = 40V and U_B = 0V and switching between T_{Aa} and T_{Ba} with duty 0,5 (switching between sequence 12 and 21 with positive current sign). When U_A = 0V and U_B = -40V BDS will work in the other quadrants III and IV (switching between sequence 12 and 21 with negative current sign).

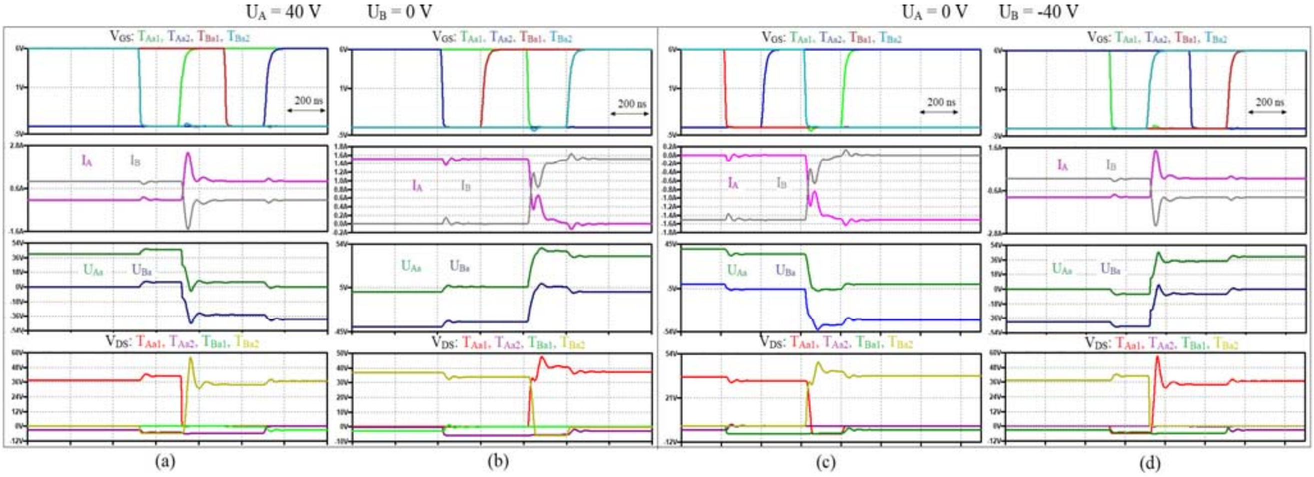

Fig.2. Simulation results of BDS in all four-quadrant characteristic I-V with 4-step semisoft current commutation: (a) T_{Aa} turning on in I quadrant, (b) T_{Ba} turning on in II quadrant, (c) T_{Aa} turning on in IV quadrant, (d) T_{Ba} turning on in III quadrant. I_A, I_B, U_{Aa}, U_{Ba} are in accordance with the scheme from the Fig.1. and V_{GS}, V_{DS}: T_{Aa1}, T_{Aa2}, T_{Ba1}, T_{Ba2} refers adequate to the gate to source voltage and drain to source of each HEMT.

Simulation results of that situations have been presented in Fig.2. Other simulation conditions are: switching frequency f_s *= 5 kHz,* load *R = 16 Ω, L = 3,51 mH*, snubber R_s *= 50 Ω* C_s *= 1 nF*, gate voltage turned on $V_{GS(on)}$ *= 6 V* and turned off $V_{GS(off)}$ *= -4 V*. Dead time between each step of commutation is equal to 200 ns. Results show that commutation process is proper. The peak of current during commutation which can be seen in Fig.2a is related to the overcharging capacitance of transistors and their snubbers. At drain to source voltages it can be observed that firstly the T_{Aa1} transistor is turned on so the capacitance has been discharged. Then, only when the current of the switched branch drops to zero (all the load current has been transferred to the other branch) the T_{Ba2} capacitance is charging (T_{Ba2} changes the state from reverse conducting to blocking mode) and this charging causes the peak of current. Moreover, the charging current closes at both sources so it could be said that this creates a short-circuit by the capacitance of T_{Ba2} and its snubber. The same process could be seen in Fig.2d (III quadrant), but when BDS switches in the II and IV quadrant (Fig.2b,c) the current peak does not occur. In that case, the signs of discharging and charging currents of capacitance are the same as the sign of the output current and the process could happen in the same time as the exchange of the load current (not after the exchange like before). The surge of the V_{DS} voltage is significant during that overcharging process. To reduce that voltage spike, the parasitic inductance had to be reduced and at higher drain to source voltages this is less visible due to lower GaN HEMT capacitances. High dropout voltage at BDS during commutation is caused by turning off the GaN HEMT using -4 V. If the GaN HEMT conducts in reverse when it is turning off the voltage drop on it is equal to:

(1) $$\Delta U = R_{DS} I_{DS} + |V_{GS(off)}| + V_{GS(th)}$$

where: R_{DS} – drain to source resistance, I_{DS} – drain to source current, $V_{GS(th)}$ – gate to source voltage threshold.
In that case the $\Delta U = 0{,}067\Omega \cdot 1A + |-4V| + 1{,}5V \approx 5{,}5\ V$. GaN HEMT can conduct in reverse mode only when drain to source voltage V_{DS} is lower than $|V_{GS(off)}| + V_{GS(th)}$ and the transistor is turned off.

C. Experimental results

To verify this commutation process experimentally two BDS GaN HEMT (Fig.3.) have been designed, built and tested.

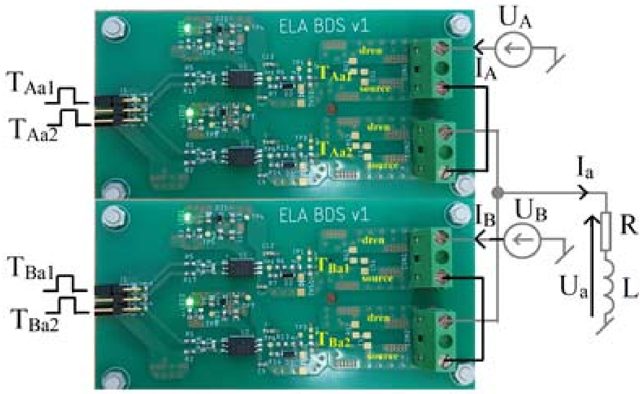

Fig.3. Experimental model of 2-phase to 1-phase converter with 2 BDS GaN HEMT connected in series with common source and RL load

One BDS consists of two GS66506T [7] connected in series with a common source controlled by the STM32F407ZE microcontroller. The gate circuit was designed basing on the evaluation board GS66508T-EVBDB2 [8] and an application note [9]. Drain and source of every HEMTs terminal were led out to make the entry check of the switches easier and to allow the modification of the configuration in the future. This, however, increased parasitic inductance. The parameters of the tested model and the switching strategy are the same as those presented in section I A.

Results of the experiment are presented in Fig.4. and they confirm earlier considerations and are very similar to the simulation results. A significant difference could be seen in the V_{GS} waveforms where there occurs ringing and undervoltage (which is controlled by +/- 6,5 V TVS). The reason of the oscillation could not be directly indicated because to observe the V_{GS} probes with long loops have been used, which could insert additional noise.

After that verification of the commutation method the 2f/1f converter was supplied by 2 phases from the grid by an autotransformer to lower the voltage amplitude. Converter switching between T_{Aa} and T_{Bb} with constant frequency fs = 50 kHz and duty 0,5 generate a sinusoidal current at the output. In cases presented above there was no need to measure the current because it had constant sign. Now, switching between 2 phases required an output current measurement so a current sensor to detect that sign has been introduced. The result of that experiment could be seen in Fig.5. The converter was protected against power failure or improper current sign detection by a clamp circuit connected to the load to intercept the energy from the inductor. A clamp circuit (CC) (commonly used in MC) has been presented in Fig.6 and consists of a one phase full-bridge rectifier, a 2 μF capacitor, and a 10 kΩ resistor. The CC had to be built using fast switching diodes to be able to catch the voltage surge in time. The resistance of the load has been changed to 8 Ω, the amplitude of each phase is equal to 30 V and the rest of the parameters are the same as in point I.B.

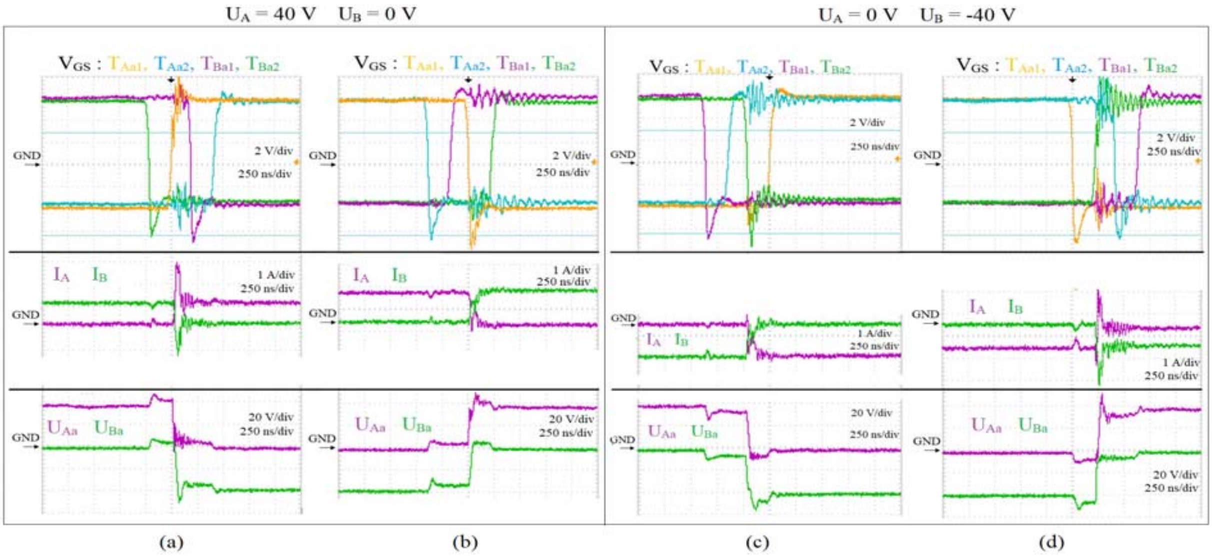

Fig.4. Experimental results of BDS in all four-quadrant characteristic I-V with a 4-step semisoft current commutation: (a) T_{Aa} turning on in I quadrant, (b) T_{Ba} turning on in II quadrant, (c) T_{Aa} turning on in IV quadrant, (d) T_{Ba} turning on in III quadrant. I_A, I_B, U_{Aa}, U_{Ba} are in accordance with the scheme from Fig.1. and V_{GS}: T_{Aa1}, T_{Aa2}, T_{Ba1}, T_{Ba2} refer respectively to the gate to source voltage of each HEMT.

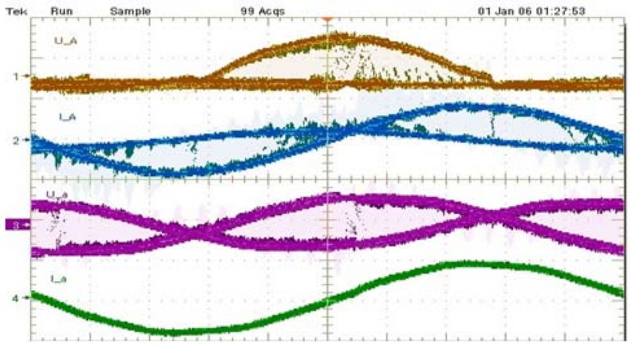

Fig.5. Waveforms $U_{DS}(T_{Aa1})$ (CH1), I_A (CH2), U_a (CH3), I_a (CH4) of the two-phase to one-phase converter with constant switching between two phases.

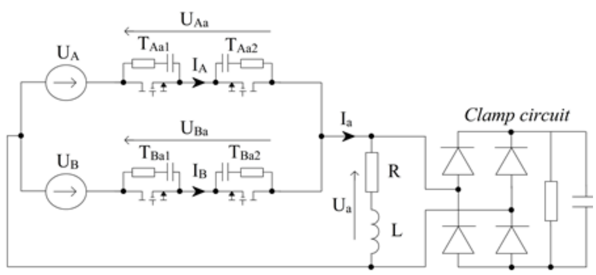

Fig.6. 2f/1f converter with clamp circuit protection.

Fig.5. shows the waveforms of drain to source voltage of T_{Aa1} $U_{DS(TAa1)}$ which is only positive because that HEMT blocks only positive voltage when it is turned off. The envelope of the phase A current I_A is the same as of the sinusoidal output current I_a because the output current is a sum of currents I_A and I_B. The output voltage U_a looks like a surface between two phases because one time at the output there is the voltage of phase A and another time the voltage of phase B. The current or voltage ripples are less visible due to the resolution but they occur like in the earlier tests. That experiment confirms the adequateness of the used commutation method and the possibility of application GaN HEMTs in the construction of BDS.

D. Sign of current detection problem

As it was mentioned in the previous point, the 2f/1f converter has been protected by a CC in case the flow of current I_a through the inductor is interrupted. This could cause a voltage surge which would damage the transistor. The same problem could occur at the input of the converter, so the commonly used CC consists of two full-bridge rectifiers connected to the same capacitor.

Another kind of protection could be the varistors added at the input and output of the converter between each phase and the ground. Together with varistors suppressor diodes have also been inserted between the drain and the gate of each HEMT [1].

To show the effects of improper current sign detection a simulation study has been conducted and the results are presented in Fig.7. Only one case has been considered with U_A = 0 V, U_B = -40 V, and the switching strategy and other circuit parameters remaining the same as in point I.C. Fig.7a presents simulation results of wrong current detection (current I_a was lower than zero, but the algorithm chose the sequence 21 with I_a greater than zero). The voltage U_{Aa} and U_{Bb} reached around -500 V because the current flows through the capacitance of the HEMTs and their snubbers. For the same case of improper current sign detection a simulation with a CC added to the load has been done, as it could be seen in Fig.7.b. Even if the the commutation was wrong the current I_a was not interrupted because when the output voltage U_a rose over the voltage of the CC the current I_a could flow by the capacitor in the CC.

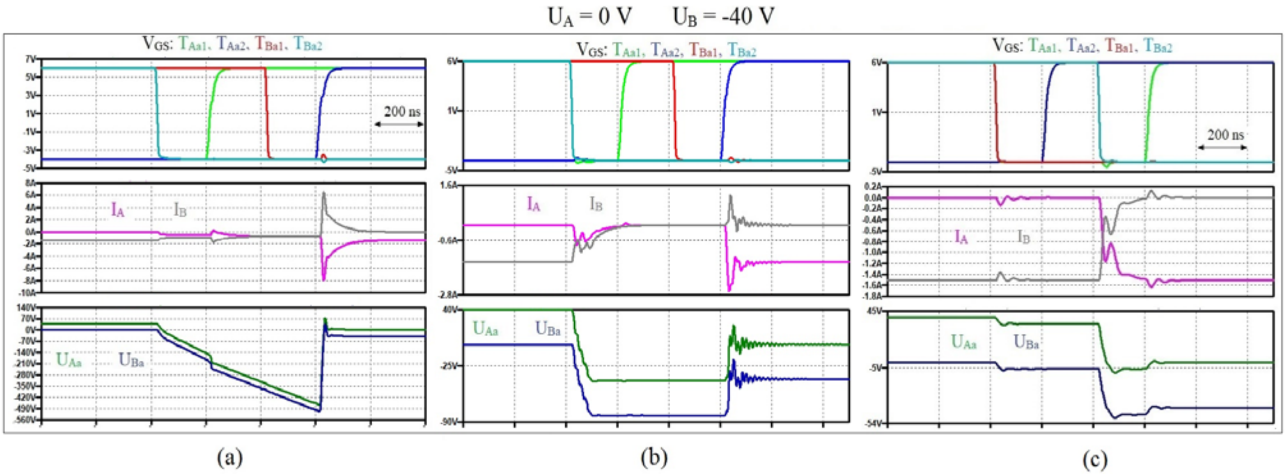

Fig.7. Simulation results of BDS during: (a) wrong current sign detection without clamp circuit, (b) wrong current sign detection with clamp circuit, (c) proper current sign detection (I_A, I_B, U_{Aa}, U_{Ba} are in accordance with the scheme from the Fig.1. and V_{GS}: T_{Aa1}, T_{Aa2}, T_{Ba1}, T_{Ba2} refers adequate to the gate to source voltage of each HEMT)

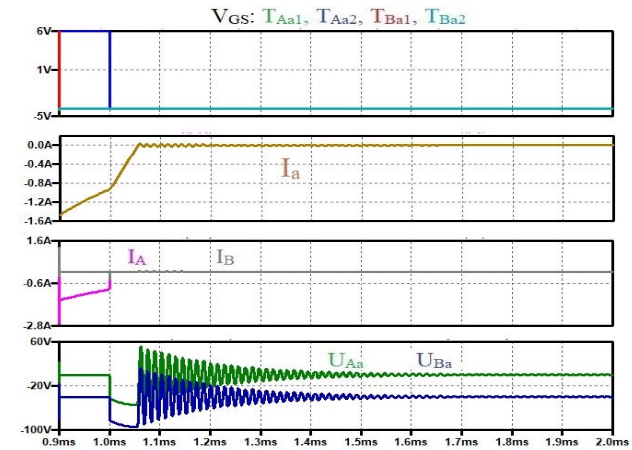

Fig.8. Simulation results of BDS during unexpected turn off of all HEMTs (I_a,I_A, I_B, U_{Aa}, U_{Ba} are in accordance with the scheme from the Fig.1. and V_{GS}: T_{Aa1}, T_{Aa2}, T_{Ba1}, T_{Ba2} refers adequate to the gate to source voltage of each HEMT)

The voltage of the U_{Ba} switch reached only -80 V when in proper commutation (Fig7.c) it reached only -50 V. The capacitance of the CC should be chosen depending on the energy that could be stored in the inductance of the load.

Finally, Fig.8 shows an example of CC protection when all transistors are suddenly turned off and the energy is transferred to the CC. After turning the transistors off the interrupted current of the load I_a was captured by the clamped circuit. When I_a approached zero amperes the oscillation of the current and the output voltage occurred, but the maximum value of the voltage during that state achieved -100V and could still be better limited using proper values of R and C of the CC.

II. Conclusions

Simulation and experimental studies has been conducted on a 2f/1f converter with BDS built from two GaN HEMT connected in series with a common source. The 4-step current semisoft commutation method was verified in detail and confirmed. The current peak occurs during switching BDS in the I and III quadrant of the I-V characteristics and it is caused by the overcharging of the capacitance of BDS and their snubbers. The application of a tested BDS in the matrix converter is possible. The current sign detection problem was mentioned and a commonly used CC protection to limit that problem was verified.

The work was supported by research projects MB/WE/2/2018 and S/WE/1/2018.

***Authors**:*
mgr inż. Krzysztof Cyprian Nowaszewski, Bialystok University of Technology, Department of Power Electronics and Electric Drives, Wiejska 45 D Street, 15-351 Białystok, E-mail: k.nowaszewski@doktoranci.pb.edu.pl;
prof. dr hab. inż. Andrzej Sikorski, Bialystok University of Technology, Department of Power Electronics and Electric Drives, Wiejska 45 D Street, 15-351 Białystok, E-mail: a.sikorski@pb.edu.pl;

REFERENCES

[1] Szcześniak P., Three-Phase AC–AC Power Converters Based on Matrix Converter Topology: Matrix-Reactance Frequency Converters Concept, *Springer*, 2013, nr 5, 125-128
[2] Hirota T., Inomata K., Yoshimi D. and Higuchi M., Nine Switches Matrix Converter Using Bi-directional GaN Device, *International Power Electronics Conference* (2018), 3952-3957
[3] Umeda H., Yamada Y., Asanuma K., Kusama F., Kinoshita Y., Ueno H., Ishida H., Hatsuda T. and Ueda T., High power 3-phase to 3-phase matrix converter using dual-gate GaN bidirectional switches, *IEEE Applied Power Electronics Conference and Exposition* (March 2018), 894-897
[4] Burany, N., Safe control of four-quadrant switches, *Conference Record of the IEEE Industry Applications Society Annual Meeting* (1989), 1190-1194
[5] Tammaruckwattana S., Yue C., Ikeda Y., and Ohyama K., Comparison of switching losses of matrix converters for commutation methods, *IEEE European Conference on Power Electronics and Applications*, 16th (2014), 133-137
[6] Zdanowski M., Rąbkowski J., Operation modes of the GaN HEMT in high-frequency half-bridge converter, *Progress in Applied Electrical Engineering, PAEE*., (2016), 468 – 474
[7] Datasheet of GS66506T from *GaN Systems webpage www.gansystems.com,* 2018
[8] "GS665xxT-EVBDB2-UserGuide-rev-2018.09.05" from *GaN Systems webpage www.gansystems.com,* 2018
[9] GN001 Application Guide Design with GaN Enhancement Mode HEMT from *GaN Systems webpage www.gansystems.com,* 2018