

Identification of Digital Relay Protection Measuring Part Elements using Time of its Tripping

Abstract. The main problem preventing the use of digital relay protection mathematical models for real devices setting up is the confidentiality of the information about its internal configuration. This mainly concerns the input circuits (measuring part) of the protection, the components of which introduce the most significant errors. In this case, an arbitrary choice of the configuration may lead to incorrect results. The identification of the internal structure by standard methods, in particular by a real interpolation method, cannot be carried out in practice, due to the need to have input and output signals. In this regard, the purpose of the research was to develop a method of identification according to the time for formation of tripping signal. Identical signals were transmitted to real device and mathematical model of protection. The starting point of the time reference was the moment when the input signal reached a threshold; the final point was the time of tripping command appearance, unlike similar studies, where the time was determined by the closure of the output relay contacts. The research was carried out for 144 different combinations of the measuring part elements: auxiliary converters, analog filters, digital finite impulse response filters. As a result, the combination in which the smallest deviation from the tripping time of the real device was observed in all studied modes was selected as the most 'optimal'. Performing such comparisons is the main way to make the model closer to real protection.

Streszczenie. Analizowano cyfrowe zabezpieczenie przekaźnikowe i jego model matematyczny przy założeniu, że nie jest znana jego struktura wewnętrzna. Zaproponowano metodę identyfikacji bazującą na pomiarze czasu między przekroczeniem przez sygnał wejściowy wartości progowej a wyłączeniem. **Identyfikacja części pomiarowej cyfrowego zabezpieczenia przekaźnikowego na podstawie analizy czasu wyłączenia**

Keywords: relay protection, identification, setting up, mathematical simulation.

Słowa kluczowe: cyfrowe zabezpieczenie przekaźnikowe, czas wyłączenia.

Introduction

According to It is known that mathematical modeling is the only generally available way to obtain information on the entire range of processes in a particular equipment, including relay protection (RP) and automation, and electric power systems (EPS) as a whole. With the advent and development of various simulation tools, many issues, the solution of which was previously difficult, become relevant. One of them is the development of new methods and means for RP devices setting up that take into account the current state and prospects of the EPS development, in particular the integration of renewable energy sources, FACTS and HVDC devices. The conclusion about this need is formulated by the authors on the basis of the analysis of the existing guidelines for the RP thresholds calculation [1]. It has been determined that modern methods for RP setting are largely based on the guidelines of previous decades, and accordingly have the same disadvantages. The main of these shortcomings is the accounting of processes in specific RPs and primary transducers and the errors introduced by them via approximate generalized coefficients.

A satisfactory solution to the indicated issue is impossible without a detailed analysis of the operation of differently designed RP devices in specific operating modes and studying the processes of currents and voltages changes in protected elements, measuring current and voltage transformers, and RP themselves. The information obtained as a result of this will allow to form the parameters for RP settings which will be adequate to the actual operating conditions.

Speaking about the RP simulation, or rather the most modern digital relay protection (DRP), two main approaches should be distinguished:

1. Modeling of DRP logic [2-4]. In this approach, only the computational and logical part (CLP) of the DRP is simulated, such as digital signal processing (filtering, conversion to vector), the RP operation algorithm and basic restraint algorithms. At the same time, taking into account the factor of trade secrets, RP models are often based on theoretical descriptions in open sources.

2. Modeling of the input circuits and DRP logic [5-7]. The elements of the measuring part (MP) and converting part (CP) are partially or completely taken into account: measuring transformers, auxiliary transducers and analog filters; switches, analog-to-digital converters (ADC). There are many variations of such DRP mathematical models, since the accurate configuration of MP and CP elements (except for measuring transformers) is also a trade secret.

Due to the confidentiality of the internal design of the DRP, in practice it is impossible to determine the configuration of MP, CP and CLP. It is obvious, however, that incorrect selection of elements can lead to false results. In this regard, the identification of the internal elements of the DRP is necessary for the further use of the mathematical model, especially for their setting up. The methods used to identify mathematical models, in particular, the real interpolation method [8], imply the presence of known signals at the input and output. As for the input signal, they are always known. The main problem is with the output signal. At the output of a real DRP terminal, it is possible to control only the operation of the output relays and binary signals that are not informative in terms of identifying the DRP configuration via this approach.

The authors are implementing a project aimed at development of a methodology for RP setting up in modern EPS, the basis of which is the use of combination of the Hybrid Real-Time Power System Simulator (HRTSim) [9] and RP detailed mathematical models that reproduce as a whole all the key and known elements of MP, CP and CLP [10]. It is obvious that the highest errors in the conversion of the primary signal are in the MP, so the main task is to determine the configuration of MP itself. Based on the above, it is necessary to develop an approach that will identify the MP configuration based on the input signal and the time for formation of RP tripping command.

Materials and methods

Before proceeding with the description of the developed method for identification of MP elements, it should be noted that the DRP model is implemented as a specialized hybrid processor "Figure 1a" [11], which was used to research protection and its settings. Specialized hybrid processor

(SHP) structure for DRP simulation presented in "Figure 1b".

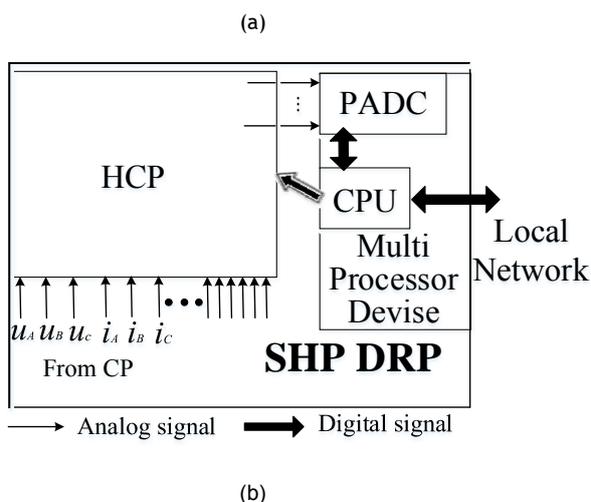


Fig.1. a) The external view of specialized hybrid processor for DRP simulation; b) Structural scheme SHP DRP

In accordance with the SHP DRP structure, for solving a system of differential equations that form a mathematical model of MP DRP, by the method of implicit integration in an analogue way a hybrid coprocessor (HCP) is being developed. The processor of analog-to-digital conversion (PADC) provides real-time reading of the values of operating parameters, their functional processing (i.e., digitization), data transfer to the central processing unit (CPU) and real-time implementation of functional controls, for example, setting the coefficients of differential equations. In addition, the PADC implements an algorithm for the DRP functioning. It should also be explained that the PADC naturally implements the CP DRP function. The PADC operational parameters are read from the EES model continuously every 200 μ s.

Microprocessor unit (MPU) CPU designed to provide the following functional properties and capabilities of the SHP:

1. Organization of network information interactions with the HRDSim Server.
2. Reading parameters from the PADC and transmitting them to the HRDSim Server.
3. Implementation of algorithms for various local scenarios designed for automatic control of SVC parameters: 1) equivalent circuit parameters MP generating transfer function (TF) coefficients and their differential equations; 2) settings for the algorithm and additional functions of digital relay protection (DRP); 3) magnetizing curve $B=f(H)$.
4. Time synchronization of both its own and peripheral processors. Time is synchronized by broadcast packets

from the HRTSim server, which contain the number of pulses (duration 50 μ s) from the beginning of its operation. All processors simultaneously receive this data, so they adjust their frequency and adjust to the frequency of the Server.

5. Reception of parameter values from the HRDSim Server and their installation in the SHP equipment: DAC SHP state control; transmission to peripheral processors, for example, to the PADC for RP setting settings and the magnetization curve $B=f(H)$.

Variables from ERS, for example, currents i_A, i_B, i_C or voltages u_A, u_B, u_C , are introduced into the circuit for solving the MP equations from specialized processors (SP) HRDSim, implementing mathematical models of EPS equipment.

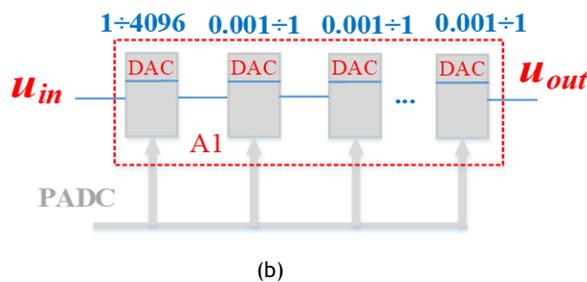
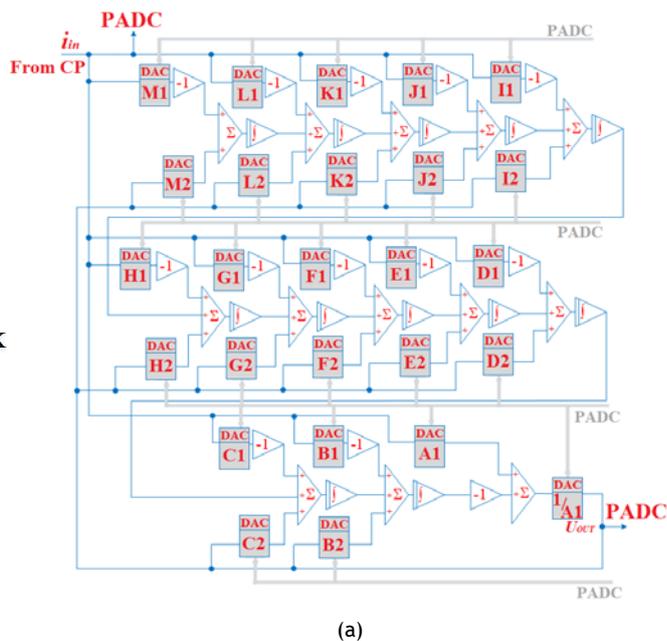


Fig.2. a) fragment of the functional diagram of the HCP for phase A of one TF in the composition of the HSP DRP, used to solve the aggregate universal mathematical model of the MP; b) range extension scheme for setting TF coefficients

A fragment of the functional diagram of the HSP for one MP as part of the HSP DRP is shown in Figure 2a. The mathematical model of the MP is calculated by the method of implicit integration by the analog method. The MP output signal U_{out} goes to the PADC, where it is digitized and goes to the program block for the implementation of the protection functioning algorithm. TF coefficients ($A_1, A_2, B_1, B_2, C_1, C_2, D_1, D_2, E_1, E_2, F_1, F_2, G_1, G_2, H_1, H_2, I_1, I_2, J_1, J_2, K_1, K_2, L_1, L_2, M_1, M_2$) determined by the RLC parameters of the MP equivalent circuit. Each coefficient is set by the user through specialized software on a client computer, from where it is transmitted to the Server and through the CPU to the PADC. In PACP, coefficients dependent on the magnetization resistance of a current

measuring transformer (CMT) Z_{μ} , recounted. Resistance Z_{μ} is selected every 100 μ s (this is the time for calculating and issuing the parameters spent by the PADC). Accounting for the magnetic properties of CMT core steel, including hysteresis, implemented in the PADC in accordance with the Preisach theory [12].

It should be noted that the difference between the TF coefficients, which are the main mathematical descriptions of RP, can be significant. The bit depth of even the most modern DACs does not allow you to set such a coefficient, therefore, to solve this problem, each DAC in the circuit in Figure 2a refers to more than one converter, and the chain is connected in series Figure 2b. In this case, the first DAC sets the coefficient value reduced to the range $1 \div 4096$ (212 this is the maximum value that can be set in a 12-bit DAC). The rest form the degree to which the coefficient needs to be reduced. Using the same 12-bit DACs can be reduced by $10 \div 1000$ times. If you do not need to reduce more, then the DAC sets 1. In each chain, apart from the main one, ten DACs are installed, which allows covering the difference by 1030 times. As a result, it is possible to form a coefficient in the range $1 \cdot 10 \cdot 30 \div 4096$.

To carry out testing operation, the SHP DRP was connected to RETOM-51. RETOM-51 [13] this is a Russian-made device for testing a relay protection device.

The DRP MP configuration was identified via comparison of the time for formation of tripping command (PUP (pick-up) command in Figure 7) of the real RP device and the mathematical model in several test modes. In this case, the input signals of the mathematical model were saved in the COMTRADE format. After that, via RETOM-51, they were transmitted to the RP terminal. The time for PUP command was determined according to the diagrams recorded using specialized software of the DRP terminal. The monitoring of contact closure of the DRP output relays and, in accordance with this, the pick-up time via RETOM-51 program timer, as, for example, in similar studies [14], was not used, since in this case the delays of the DRP output elements (digital-to-analog converters (DAC), analog signals amplifiers and output relays, with the help of which control signals are generated) are taken into account. To solve the issue of defining protection settings, these elements are not needed and, accordingly, their influence during identification should be excluded, what has been achieved through the applied approach.

Obviously, the intrinsic time of terminal operation own is mainly determined by auxiliary converters, analog frequency filters, ADC, microprocessor (operations of digital filtering and vector conversion). When determining the 'optimal' implementation of DRP, combinations of different elements were used in the comprehensive model: an active auxiliary current transformer (ACT), a passive ACT "Figure 3a", 1÷6 order Butterworth low-pass filters (LPF) "Figure 3b", 1÷6 order Chebyshev LPF, 1÷6 order digital finite impulse response (FIR) filters [15]. A total of 144 combinations were studied. Two types of LPF were used – Butterworth and Chebyshev – since they are most often used in DRP simulation [5-7]. Implementation of the required LPF and ICT model via a universal model was carried out by varying the values (10^{-10} or 10^{10} Ohms) of resistances (R_{TEMP1}) in the circuits. To generate a PUP signal, it is necessary to fulfill the conditions for operation of any protection. As the test subject, the simplest instantaneous overcurrent protection without time delay was selected. The specific type of protection is not important, since the RP algorithm receives data after its processing by MP, CP and microprocessor. The threshold of protection operation is arbitrarily generated in such a way as to ensure the RP operation in all test modes. The starting point of the

time reference both for the model and for the real protection device is the moment when the input signal reaches the RP threshold ('SET' command in Figures 5-7).

Additional identification research conditions are presented below:

1. The measuring current transformer was not taken into account in the study, since it is an external element of the DRP MP. Despite this, the input signal was transmitted to the model with the transformation ratio 1000/1. This was done in order to adapt to the RETOM range ($0 \div 20$ A).

2. The current protection threshold in primary values is 1000 A (1 A is the real current from RETOM).

3. The LTS 15-NP is adopted as an active ICT. The burden impedance of the passive ICT is selected in such a way as to ensure maximum closeness of its frequency characteristics with the active ICT.

4. The cutoff frequency of the analog LPFs is adopted at 250 Hz [15].

5. The conversion time of the ADC as part of a specialized hybrid processor is in the range of $0.36 \div 1.8 \mu$ s.

6. To convert the input harmonic signal to a vector, the Fourier transform algorithm was used.

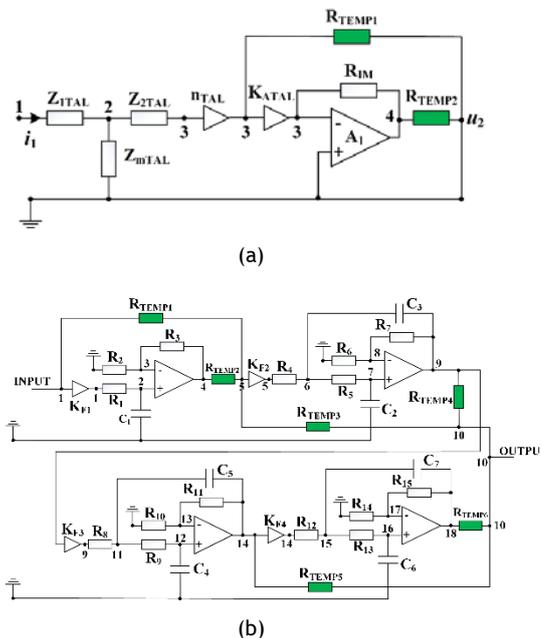


Fig.3. a) Universal equivalent scheme of ACT; b) Universal equivalent scheme of Butterworth LPF

Research results and discussion

The tests were performed for the EPS scheme shown in Figure 4. The primary signal was received (phase A current on the high voltage side of the transformer at Substation 5) via the HRTSim in the COMTRADE format. The recording was carried out for the following modes: internal (three-phase-to-ground, line-to-line, double line-to-ground and single line-to-ground) SCs at the terminals of the power transformer on the medium voltage side (point K1 in Figure 4), external (three-phase-to-ground, line-to-line, double line-to-ground and single line-to-ground) SCs on the substation medium voltage buses near the load (point K2 in Figure 5). It should be noted that the location of the SC is also not important.

The tripping time of the real terminal and the mathematical model is determined for all modes by the method described above and shown in Figures 5-7. All results are summarized in Table 1.

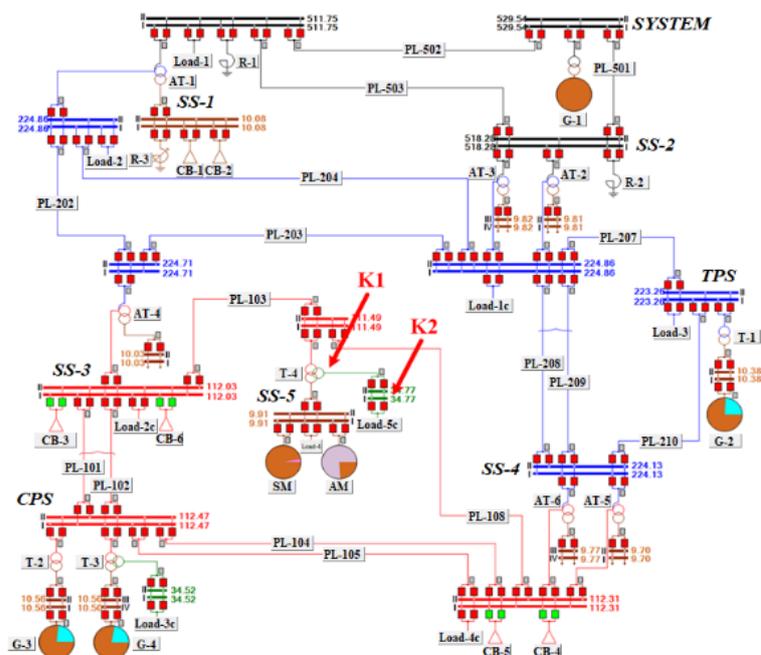


Fig.4. The Single-phase view of the simulated test EPS scheme in HRTSim, where G - generators; SM - synchronous motor; AM - asynchronous motor; PL - power transmission lines; AT - autotransformers; T - transformers

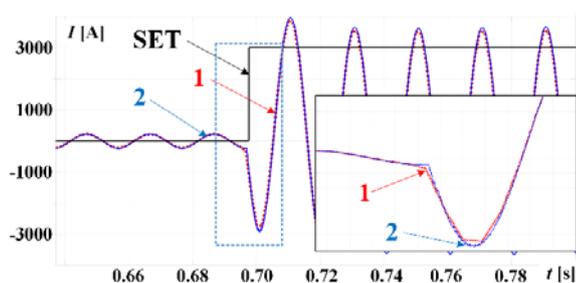


Fig.5. The oscillogram of the input signal in case of ABCG (point K1): 1 – recorded by the RP terminal, 2 – the original signal, recorded in COMTRADE

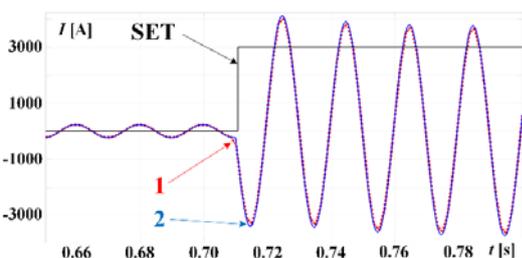


Fig.6. The oscillogram of the input signal in case of ABCG (point K1): 1 – recorded by the RP terminal, 2 – the original signal, recorded in COMTRADE

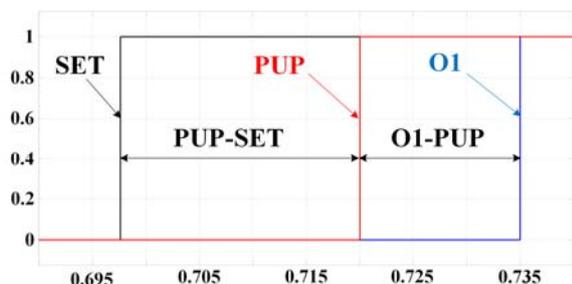


Fig.7. Logic signals in case of ABCG (point K1): O1 – tripping of the RP terminal output relay; PUP – tripping command of the microprocessor; SET – tripping of the 'ideal' protection (without internal delays)

Table 1. Protection tripping time determination

Mode	Tripping Formation Time (PUP-SET), ms	Output Signal Formation Time (O1-PUP), ms	DRP Tripping Time (selected combination), ms
ABCG (point K1)	11,8	15	14,5
AB (point K1)	15,5	15	19,1
ABG (point K1)	20,6	15	15,6
AG (point K1)	9,45	15	14,5
ABCG (point K2)	22,5	15	20,1
AB (point K2)	22,8	15	19,35
ABG (point K2)	25,65	15	20,15
AG (point K2)	19,05	15	20,55

The formation time of the O1-PUP output signal in all experiments was 15 μ s, i.e. the time from the moment of SC fixation to the formation of the tripping command (time delay of the output elements: DAC, amplifiers, output relays) for such particular DRP terminal does not change regardless on the type and location of fault.

The selection of the most 'optimal' elements combination, i.e. at which the tripping formation time was the closest, was carried out as follows. Combinations in which all deviations are minimal are initially selected. Of the remaining combinations, one was selected in which the deviation was at a mean level in each mode, i.e. those in which there were no significant differences from one mode to another. As a result, for a specific DRP terminal, the combination active ICT & 3rd order Chebyshev LPF & 4th order finite impulse response digital filter has been defined.

Conclusion

Given the previously indicated confidentiality, the implementation of such comparisons is the main way to make the RP mathematical model closer to real DRP

device. With the help of such studies, a table of 'typical' tripping times can be obtained and, in practice, depending on a specific type of protection terminal, a predetermined 'optimal' internal configuration of protection can be chosen which will be used in RP setting up via its comprehensive mathematical models.

Acknowledgment

This work was supported by the Ministry of Science and Higher Education of Russian Federation under the governmental grant "Science" № FSWW-2020-0017.

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