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Application of Multi-Stage Window Comparator Circuit with Safety Mode for Swell Voltage Control in Low Voltage Systems

Abstract. This article presents the application of a multi-stage window comparator circuit with safety mode for swell voltage control in low voltage systems that lack stability and electrical quality. High-voltage transistors were used to build a simple voltage detecting circuit with multi-stage functions and electronic load to detect and control swell voltage. SVSS as the overloaded energy receptor resulted in clamping voltage. The voltage of a device is equal to the voltage flowing to smart electronic loads and not over the IEEE 1159 and 1100 standards. The device worked normally without causing damages. Failure Mode and Effect Analysis (FMEA) might occur using a multi-stage window comparator circuit in the safety mode. The reliability and stability in detecting voltage and controlling electronic loads to work safely under many kinds of situations were also assessed.

Streszczenie. W artykule zaprezentowano wykorzystanie komparatorów do kontroli zwiększonego napięcia w systemach niskiego napięcia. Napięcie nie przekracza zaleceń norm IEEE 1159 i 1100. Zastosowanie kaskadowych komparatorów w trybie bezpieczeństwa do kontroli spiętrzenia napięcia w systemach niskonapię1)ciowych

Keywords: window comparator multi-stage, Failure Modes and Effects Analysis (FMEA), Swell Voltage Surge Suppressor (SVSS) **Słowa kluczowe:** komparatory kaskadowe, analiza zakłóceń pracy układu, przepięcvia.

Introduction

Advancement of electronic technology has resulted in many innovations that facilitate and improve the lives of people. For example, information and knowledge can be easily accessed by connecting to the internet, building smart homes, smart grids, solar PV rooftops [1] and smart farms. Smart electronic devices are now connected to the distribution system in the Provincial Electricity Authority (PEA). These advanced technological electronic devices have sensitivity towards noise. Quality problems of electricity systems or swell voltage cause damages to smart electronics used in the household as seen in Fig. 1.



Fig. 1. Effect from swell voltage resulting in the damages of Electronic devices $% \left({{{\rm{E}}_{{\rm{E}}}} \right)$

Problems of electric quality are often found in rural areas caused by lighting, switched capacitors, system maintenance, use of nonlinear devices, incorrect ground system and use of inconsistent technology in the electrical system [2-3]. These problems promote changes in electrical quality. If the devices have sensitivity towards the response this might cause failure or malfunction. Although many systems have Surge Protection Devices (SPDs) for AC surge [4-7], damage to electronic devices still occurs as seen in Fig. 1. Damages from the change of electrical quality or swell voltage occur when RMS voltage exceeds IEEE 1159 and 1100 standards [8-9] (Fig. 2). Installation of SPDs in low-voltage systems [10] cannot prevent swell voltage lower than the working level of the device, resulting in damages to smart electronic machinery. This is a big problem for electrical quality of distribution systems in PEA.

Apart from the damages, swell voltage also impacts users. As a result, analysis and improvement of electrical quality must adhere to real situations of specific areas in the country.

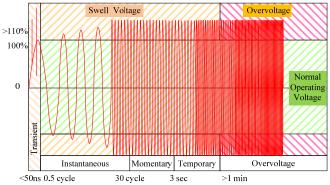


Fig. 2. Voltage Reduction Standard of IEEE Std 1159-1995

This article presents the concepts of application of a multi-stage window comparator circuit with safety mode for swell voltage control in low voltage systems through the development of a Swell Voltage Surge Suppressor (SVSS) to reduce damages to smart electronic devices conducted to distribution systems in PEA. Design of a multi-stage window comparator circuit with safety mode using high-voltage transistors [11-14] enhances the endurance of the circuit towards high voltage systems and prevents failure, resulting in improved circuit reliability.

Basic Window Comparator Circuit

Window comparator circuits (WCs) often used are IC Op-Amp, Logic gate, IC packet, IC CMOS and TTL [15-18]. The window comparator circuit type IC has low input voltage and current. It is suitable for analysing small signals. If devices inside the IC are damaged or lack qualification, the circuit will not work or work abnormally. For these IC devices, characteristics of damages inside the circuit cannot be examined. The window comparator circuit has different low-voltage levels (V_{Low}) and high-voltage levels (V_{high}). This qualification is called Hysteresis and is used to detect the signal as the designed function. If the analogue input (V_{in}) is in the range of standardised electrical level, the output signal will be 1 (High). However, apart from this condition, signal output will be 0 (Low).

Window Comparator Circuit with Transistors

After the IC window comparator circuits have been applied to detect the overvoltage [19], this might damage the devices inside IC. The use of transistors in the design of window comparator circuits is important [12-14]. Today, semi-conductors have been developed for use at higher voltage. Application of high-voltage transistors with V_{CE} ±300V of KSP42 and KSP92 transistors in the design can be adapted for other uses. Oscillator circuits made from a pair of transistors are used in window comparator design (Fig. 3). When V_{in} is higher than V_{ref_L} (V_{in} > V_{ref_L}), the transistor Q₁ works (on) with electricity flowing through Q₁, resulting in clamping voltage at R_3 (V_{\mathsf{R}3}). The resistors, R_4 and R₅, are voltage divider circuits. They control the function of low voltage (V_{ref L}) as seen in the equation.

(1)
$$R_{ref_L} = R_4 / R_5 = \left(\frac{R_4 \times R_5}{R_4 + R_5}\right)$$

(2)
$$I_{Bref_L} \cong \left(\frac{V_{in} - V_{be(on)}}{R_{Bref_L}}\right)$$

(3)
$$V_{ref_{-}L} = \left(\frac{R_5}{R_4 + R_5}\right) \times V_{cc}$$

$$(4) V_{out} = \frac{V_{R3}}{2}$$

When V_{in} has voltage higher than V_{ref_H} (V_{in} > V_{ref_H}), the transistor Q_2 will work (on) while the resistors, R_1 and R_2 , which are voltage divider circuits, control the function of low voltage (V_{ref H}). When the transistor Q₂ works and enters saturation, the output signal V_{out} =0V as seen in the equation.

(5)
$$R_{ref_{H}} = R_1 / R_2 = \left(\frac{R_1 \times R_2}{R_1 + R_2}\right)$$

(6)
$$V_{ref_{-}H} = \left(\frac{R_2}{R_1 + R_2}\right) \times V_{in}$$

(7)
$$I_{R3(sat)} = \frac{V_{in} - V_{R3(sat)}}{R_3}$$

(8)
$$I_{Bref_{H}} = \frac{V_{in} - V_{BE(sat)}}{R_{Bref_{H}}}$$

$$(9) V_{out} = 0V$$

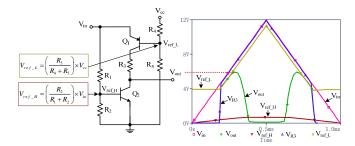


Fig. 3. Window Comparator Circuit with Transistors

Application of a window comparator circuit requires expansion of the output signal to make the output signal logic become 0 (OFF) or 1 (ON). When V_{in} is at the specified level, the voltage Vout at the Q3 transistor's base is around 0.7V, resulting in electricity flowing and the clamping voltage V_{ce} of the Q_3 transistor is 0V. The Q_4 transistor will not work (I_C =0). Therefore, the transistor works like a switch in an open circuit or in the cut-off state, causing clamping $V_{ce(cut-off)}$ at the Q₄ transistor equal to V_o and V_P as seen in the equation.

(10)
$$V_{ce(cut-off)} = V_P - I_C R_7 = V_P - 0V = V_P = V_{o(ON)}$$

When Vin is outside the standard voltage level, the voltage at the Q₃ transistor's base will be lost, causing flow of electricity ($I_C=0$). The clamping voltage has R_6 equal to I_CR₆, resulting in voltage at the Q4 transistor's base while the electricity I_C flows to the high position resulting in clamping voltage Vce=0V. Therefore, the transistor works like a switch in a closed circuit or in saturation state as seen in equation.

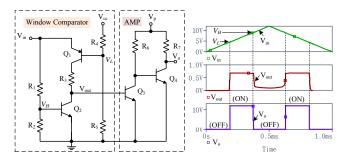


Fig. 4. Window Comparator Circuit with Extended Circuit

In Fig. 4, Vp is the output voltage that can control the voltage level of electronic loads. Characteristics of the output signal of a window comparator circuit with Q₃ and Q₄ transistors work like a switched circuit. When the signal of V_{in} in the windows of V_{ref_L} and V_{ref_H} is according to the set function as seen in Fig. 5, the output signal remains High (ON). If V_{in} is outside of $V_{ref L}$ and $V_{ref H}$, the output signal will be Low (OFF) as seen in the equation.

(12)
$$V_o = V_P \text{ when } V_{ref_L} < V_{in} < V_{ref_H}$$

(13)
$$V_o = 0V \text{ when } V_{ref_L} > V_{in} > V_{ref_H}$$

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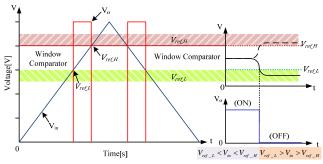


Fig. 5. Comparison of output signals of the window comparator circuit

To make it simple, a block diagram similar to Op-amp was drawn with single input and output. This means 1 Opamp symbol is equal to 1-stage window comparator circuit or WCS-1 as seen in Fig. 6.

From Fig. 6, set the function of window comparator with four resistors: R₁, R₂, R₃, and R₄, connecting in the voltage divider circuit as R1 and R2 to control the function of Vref H while R_3 and R_4 control the function of V_{ref_L} . To create the signal channel of the window comparator, the difference between voltage level V_{ref_L} and V_{ref_H} will be called hysteresis voltage or V_{hyst} [18]. This could cause a change of voltage level at two positions as seen in Fig. 7. Consequently, to calculate Window Comparator Hysteresis, the voltage level should be set to eliminate the swing of the input signal $V_{\rm in}$ due to error or noise as the equation below.

$$(14) V_{hsyt} = V_{ref \ H} - V_{ref \ L}$$

(15)
$$V_{hsyt} = V_{in} \left(\frac{R_2}{R_1 + R_2} \right) - \left(\frac{R_4}{R_2 + R_4} \right) \times V_{CC}$$

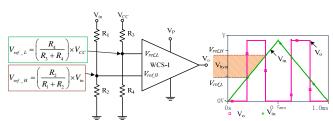


Fig. 6. Functionality of Window Comparator

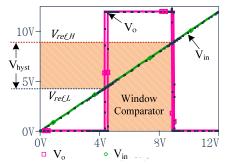


Fig. 7. Output Signal of Window Comparator with Hysteresis

Multi-stage Window Comparator Circuit

A multi-stage window comparator can set multi ranges of voltage level to assess the difference between V_{ref_L-N} and V_{ref_H-N} when an analog output signal V_{in} is added into the system. If it is from WCS-1 to WCS-N as the regulated function, the output signal from V_{o-1} to V_{o-N} of any stage will be 1. Apart from this condition, the output signal will be 0 as seen in Fig. 8.

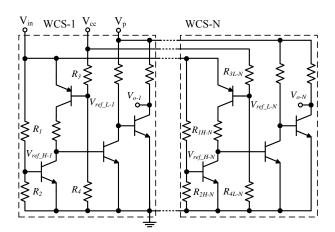


Fig. 8. Multi-stage Window Comparator Circuit

Fig. 8 demonstrates the overview of the multi-stage window comparator circuit. When used to detect swell voltage, it will assist by dividing the violent level of swell voltage that enters the low voltage system. Selection of device, resistor and transistor in the circuit must be endurable. The working function must be examined and failure mode analysed to check the abnormality of physical characteristics.

Principle of Swell Voltage Control

Swell voltage control by a Swell Voltage Surge Suppressor (SVSS) can be used as the electronic load that receives overvoltage in the system [20-21]. There are four sets of window comparator circuits for detecting swell voltage. Each set has a different window level. WCS-1 first detects the swell voltage. If V_{in} shares the same value as the window's voltage of WCS-1, the output signal V_{o1} becomes 1. When V_{in} rises to reach the window levels of WCS-2, WCS-3 or WCS-4, then one of the output signals at V_{o2}, V_{o3} or V_{o4} is 1. All three sets work under the window level of WCS-1 as seen in Fig. 9.

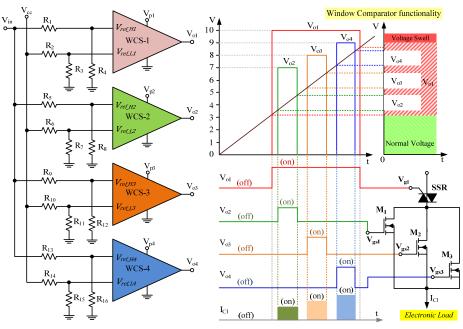


Fig. 9. Multi-stage Window Comparator Circuit and Output Signal

In Fig. 9, the electronic load controlled by the multi-stage window comparator circuit will work when Vin shares the same window level as WCS-1. The output signal Vo1 will force the switch of Solid-state Relay (SSR) [22] to activate (on) and when the voltage of V_{in} is equal to the window level of WCS-2 ,WCS-3 or WCS-4, it will cause Leakage Current (L_{C1}) through electronic loads M_1 , M_2 or M_3 , which connect in parallel. If the device at M₁ level becomes damaged and the voltage V_{in} continues to increase, M_2 and M_3 still work. $M_1,$ M₂, and M₃ are electronic device type Power MOSFET. Here, selected SCT3080KL MOSFET with voltage between Drain-Source could reach 1,200V. It is an electronic lead that works as the energy supporter and could be compared to a load in the system. The use of MOSFET enhances the endurance of the electronic circuit to be safer, more constant and prevent dangerous failure that might occur in the system. When Vin is lower, the window comparators WCS-2, WCS-3 or WCS-4 will cause M₁, M₂ or M₃ to stop working, while they are working under WCS-1, until the voltage is lower than WCS-1. It also causes the SSR to stop working (off). The electricity IC1 ceases to flow. Characteristics of electronic load control of M_1 , M_2 , and M_3 have different voltage control level.

This affects the flow of electricity through electronic loads and helps to control the loaded voltage at the standard level in accordance with IEEE Std 1159 and IEEE Std 1100.

The multi-stage window comparator for swell voltage control with RMS over the standard ($230V \pm 10\%$) [8-9] will be installed parallel to the power system. The swell voltage causes electricity to flow through the first rectifier circuit, which is the voltage sensor (V_{SS}), while the resistors R₁ and R₂ connect to the voltage divider circuit to reduce the voltage to remain at the appropriate level. The received V_{in} will be added to the window comparators WCS-1 WCS-2 WCS-3, and WCS-4 respectively, as seen in equation.

(16)
$$V_{in} = V_{SS} \frac{R_2}{R_1 + R_2}$$

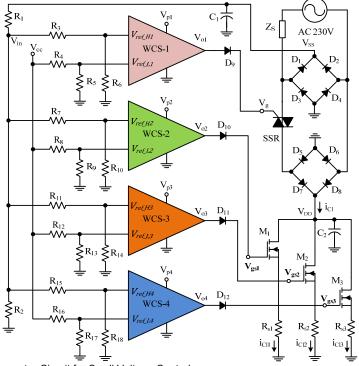


Fig. 10. Multi-stage Window Comparator Circuit for Swell Voltage Control

From Fig. 10, the voltage detector circuit by the window comparator with the safe mode will examine the voltage V_{in}. If V_{in} follows the condition, the output signals V₀₁, V₀₂, V₀₃ or V₀₄ will control electronic loads in accordance with the overvoltage level in the system. The electronic load control circuit will supply electricity and control voltage, resulting in clamping voltage at the electronic loads as seen in the equation.

(17)
$$V_{DD} = V_{M1} + (i_{Cl1}R_{S1})$$
 when $V_{o2} = 1$

(18)
$$V_{DD} = V_{M2} + (i_{Cl2}R_{S2})$$
 when $V_{o3} = 1$

(19)
$$V_{DD} = V_{M3} + (i_{Cl3}R_{S3})$$
 when $V_{o4} = 1$

If drawing the block diagram by replacing SVSS as the resistor load (R_{EL}), when removing the sensitive load out of the circuit, it is evident that R_{EL} makes the series with the resistant (Z_S) of the power distribution source by dividing from the voltage at V_{SVSS} . As seen in Fig. 11, the electronic

load pulls the power current I_{Cl} to flow through itself as a means to preserve the voltage level, $V_{\text{SVSS}} \cong V_L$ that is distributed to the load to remain level and not over the standard as seen in the equation.

(20)
$$V_{SVSS} = \frac{Z_{SVSS}}{Z_{S} + Z_{SVSS}} \times V_{S}$$

$$I_{Cl} = \frac{V_S}{Z_S + R_{FL}}$$

The electronic load is similar to the resistor load connecting to the AC source, resulting in swell voltage and swell current as seen in the equation.

(22)
$$V_{SVSS(t)} = V \cos(\omega t - \theta_V)$$

(23)
$$I_{Cl(t)} = I\cos(\omega t - \theta_{I})$$

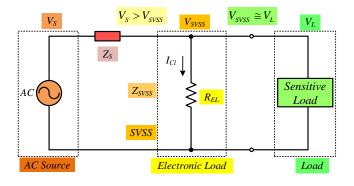


Fig. 11. Connection of electronic loads by dividing the voltage from the power source

To calculate the clamping voltage of the electronic load circuit, see the equation.

$$(24) V_{SVSS(t)} = I_{Cl(t)}R_{EL}$$

For consideration of the power of electronic loads in the AC power system during the electricity flow due to swell voltage, the multiple results of voltage and short current, see the equation.

$$(25) P_{SVSS(t)} = V_{SVSS(t)} I_{Cl(t)}$$

Table 1. Result of Failure Modes and Effects Analysis of the created Window Comparator Circuit

Devices	Failure Mode	Effect of Window Comparator	Effect of Failure	Effect of SVSS			
R₄	Open circuit	Change of circuit characteristic	d	Δ			
	Short circuit	No Output Signal	d	Δ			
	R ₁ *2	Change of circuit characteristic d		Δ			
	R ₁ * 0.5	Change of circuit characteristic					
R₅	Open circuit	No Output Signal	e	Δ			
	Short circuit	No Output Signal	d	Δ			
	R ₂ *2	Change of circuit characteristic	d	Δ			
	R ₂ * 0.5	Change of circuit characteristic	d	Δ			
Q ₃	Open circuit	Normal circuit	b	Δ			
	Short circuit	No Output Signal	b	Δ			
	R ₂ * 0.5 Open circuit Short circuit	characteristic Change of circuit characteristic Normal circuit No Output	d b b	Δ Δ Δ			

Notes *(0.5) and *(2) referred from the standard measurement. (a): Normal Output (b): No Output (c): window Voltage reduced (d): window Voltage increase (e): Output as V_p (f): Half reduction output Δ : no significant consequences of SVSS

Analytical Result of The Window Comparator's Safe Mode Circuit

Failure Modes and Effects Analysis (FMEA) [23-26] is the indicator in analysis of the safe failure of the window comparator that leads to prevention of damages. The principle of the analysis has been standardised and the result confirms that the window comparator circuit will work with the safe mode. If there is any dangerous failure with any device in the window comparator or the four sets, SVSS will stop working immediately and will not cause any dangerous failure to the system. See Table 1.

Testing Result of Swell Voltage Control

The SVSS device was tested for swell voltage control [27-29] by connecting to the top the system before distributing the voltage at 280V, 290V, 300V, 310V, 320V, 330V, 340V and 350V [20-21] and measuring the signal wave of clamping voltage at the output as seen in Fig. 12 and Fig. 13.

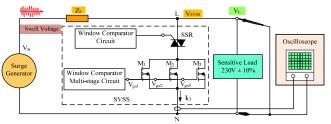


Fig. 12. Testing the SVSS Circuit for Swell Voltage Control



Fig. 13. Measurement of the model SVSS by Oscilloscope

The wave of the output signal of the multi-stage window comparator was measured for electronic load control by adding the triangle-wave signal to test its function. When the voltage reached the destined level, the output signal through the windows V_{o1} , V_{o2} , V_{o3} , and V_{o4} to control the electronic loads in accordance with the overvoltage. See Fig. 14 and Fig. 15.

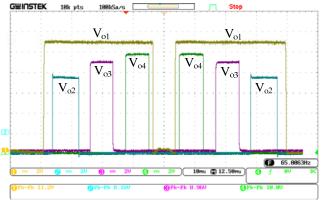


Fig. 14. Output signal of multi-stage window comparator for SVSS control

The distributed AC current was at 280-350V and the frequency was 50 Hertz. The wave of the signal to test the size of overrated voltage is shown in Fig. 16. The test applied an oscilloscope to measure the signal wave of current and clamping voltage at the output before recording (Table 2).

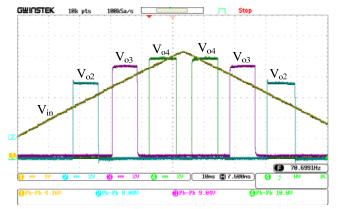


Fig. 15. Input and Output Signals of multi-stage window comparator for SVSS control

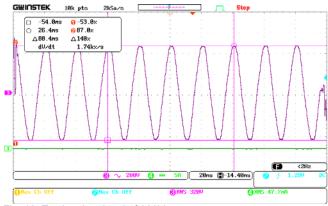


Fig. 16. Testing the signal of 320V

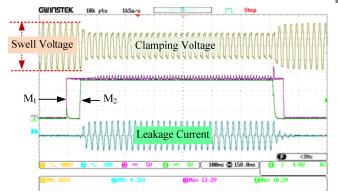


Fig. 17. Input and Output signal of SVSS for Swell Voltage Control

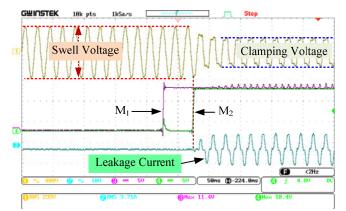


Fig. 18. Frontal expansion of swell voltage control

Fig. 17 shows the distributed overvoltage in the system. The signal detected CH1 as the signal wave of swell voltage and CH3 as the output signal from the window comparator with V₀₁ as the signal forcing M₁ CH4 as the output signal from the window comparator with V₀₄ as the signal forcing M₂, and CH2 as the wave of electric current I_{C1} flowing through the electronic loads for swell voltage control. as seen in Fig. 18 and Fig. 19.

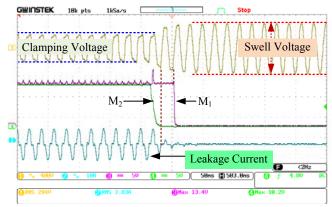
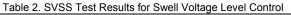


Fig. 19. Rear expansion of swell voltage control



Sequence test	Voltage test Vt[V]	Clamping voltage Vc[V]	Leakage current CI[A]	Power of SVSS P _{svss} [W]	
1	280	218	3.37	734.66	
2	290	220	3.56	783.2	
3	300	224	3.64	815.36	
4	310	226	3.77	852.02	
5	320	233	4.22	983.26	
6	330	234	4.43	1036.62	
7	340	237	4.54	1075.98	
8	350	245	4.97	1217.65	

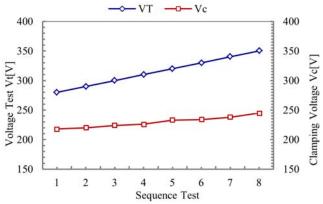


Fig. 20. Graph showing the relationship between voltage test and clamping voltage

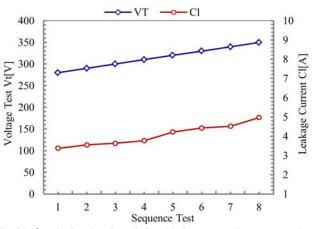


Fig. 21. Graph showing the relationship between voltage test and leakage current

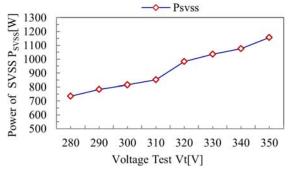


Fig. 22. Graph showing the relationship between transient power loss and voltage test

Data were demonstrated in the graph as the relationship between voltage, electric current and electric power of SVSS for swell voltage control as seen in Fig. 20, Fig. 21 and Fig. 22 respectively.

Conclusion

This article demonstrated the multi-stage window comparator circuit as safe for swell voltage control in low voltage systems. Problems are caused by the quality and stability of the power system and might affect smart electronic devices conducted on distribution systems in PEA. The design of swell voltage level control contains the main circuit as the window comparator circuit with safe mode to detect the overvoltage level from the high-voltage transistor, with the purpose of enhancing the endurance of high-voltage. It also reduces the effect of dangerous failure in the system. The created window comparator circuit can detect voltage level and control electronic loads with safe mode. The FMEA result based on IEC 61496-1 standard, assured the working process of the device to be reliable and stable to control safety under many kinds of situations. The testing result showed that SVSS for swell voltage level control was effective by allowing the electric current to flow through itself, resulting in reduction of voltage level. The current moving through smart electronic devices was not over the standards of IEEE Std 1159 and IEEE Std 1100.

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