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The Improvement of a Fail-safe Counter for Low-speed Detection

Abstract. *This paper presents a low-speed detection method by proposing a fail-safe counter. The features of this proposed method were the adoption of digital counter circuits for the detection of low-speed, the diagnosis of the digital counter circuit, and its result output as dynamic signals to a low-pass filter and a charge pump circuit. Moreover, an additional diagnosis of a fail-safe window comparator which evaluated the DC signal level from the charge pump circuit. The improvement of a fail-safe counter for low-speed detection required a simple calculation of the circuit without any use of CPUs. These diagnoses were regarded as the frequency domain and time domain. When the motor speed became lower than the predetermined speed and there were no parts of the digital counter circuit malfunction, the dynamic signals with the low-pass frequency would be provided to the filter and the DC signal would eventually be the output, as the low-speed detection results displayed a fail-safe manner. These have been revealed by the FMEAs of the fail-safe counter, including the failure modes.*

Streszczenie. *W artykule przedstawiono metodę wykrywania małej prędkości, proponując licznik odporny na uszkodzenia. Cechy proponowanej metody polegają na zastosowaniu cyfrowych obwodów licznika do detekcji małych obrotów, diagnostyce obwodu licznika cyfrowego i wyprowadzaniu wyniku w postaci dynamicznych sygnałów do filtru dolnoprzepustowego i obwodu pompy ładunkowej. Ponadto dodatkowa diagnostyka niezawodnego komparatora okienkowego, który oceniał poziom sygnału DC z obwodu pompy ładującej. Udoskonalenie niezawodnego licznika do wykrywania małej prędkości wymagało prostego obliczenia obwodu bez użycia procesorów. Rozpoznania te traktowano jako dziedzinę częstotliwości i dziedzinę czasu.. (**Poprawa niezawodnego licznika do wykrywania małej prędkości**)*

Keywords: Fail-safe, digital counter, window comparator, FMEA
Słowa kluczowe: licznik małej prędkości, .błędy zliczania

Introduction

Detection of low-speed or motor stoppage is an important function for safety-related applications, i.e, functions in standard IEC 61800-5-2 (adjustable speed electrical power drive systems) [1]. However, there is no conventional hardware design for low-speed detection in a secure manner. The most common measurement for this presentation is the generation and production of dynamic signals, which are widely used in the field of machine safety. Nevertheless, it is difficult to generate a dynamic signal only under a low-speed motor. As such, the method for low-speed detection would use a fail-safe counter. When the motor speed is below the rated speed and there is no fault in the counter circuit, the direct current would be the final output of the result of the low-speed detection in a safety manner [2]. Therefore, the method for low-speed detection could be conducted by using a safety counter. When the motor speed is below the rated speed and there is no fault in the counter circuit, the direct light would be the final output of the result of the low-speed detection in a safety manner. The analysis of the protection from the safety counter and the design concept of the safety counter was composed of three parts, a digital counter, band-pass filter with a pump-up circuit, and the windows comparator circuit (Figure 1).

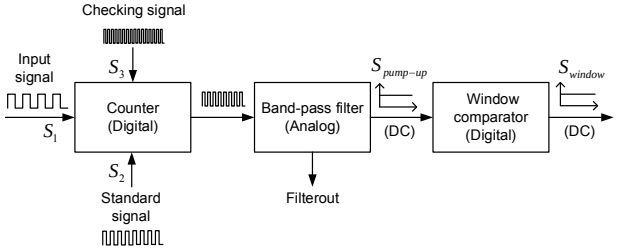

Fig. 1. The fail-safe counter with a window comparator [2]

Figure 1, if the frequency f_1 of the signal S_1 is lower than the frequency f_2 of the signal S_2, indicating that the motor speed is below the predetermined speed, the signal S_3 will be used to diagnose the digital counter and the signal S_0 to the frequency f_4, which will be the signal of f_3. Furthermore, the frequency pass filter will be intended for only the band-pass filter when the diagnostic result had the appropriate value and f_1 is lower than f_2. Then, the DC signal will be the output of the low-speed detection in a safety manner.

The safety principle could be achieved by dynamic processing in the safety conditions, which could be defined by dynamic signals [3-5]. The electronic circuit could be specifically designed, so that it could not generate dynamic signals and not cause fluctuations when any malfunction occurred in the circuit portion. Moreover, the dynamic signals would be obtained only under safe circumstances, and there was no malfunction.

Figure 1 shows the signal emerging from the fail-safe counter at a high-frequency signal. It needs to be filtered by a band-pass filter to the desired frequency band. In this article, the band-pass filter is proposed to compare with the band-pass filter. When the frequency is up to 3.2 MHz, and the CMOS Schmitt-trigger invertor ICs self-oscillation signal is approximately 100 kHz [6], filtering higher than that value will not be disturbed by any signal interference. Therefore, it will be failure within the circuit.

An analogue window comparator is a circuit used to monitor signals in industrial applications [2, 7-9]. The design concept is based on AND logic circuit that is on transistor oscillation, it is determined by the resistance and input voltage of each input. Nowadays, digital window comparator circuits have been invented and tested to detect signals [10-13].

There are also several methods of ensuring that the equipment or circuits do not fail dangerously; such as, the IEC 60812, analysis techniques for system reliability, and procedures for failure mode and effects analysis (FMEA) [14]. This is a test of the equipment in an electrical circuit where each device is tested for different failure values as specified in each standard. The mean time to failure [15-16] is a method for ensuring confidence by finding the mean time to the failure of a combined electronic device to determine the mean time to the failure of the system [17].

The purpose of the revision is to reduce the number of circuits, number of equipment, and fail-safe testing. So to meet the principle of a fail-safe circuit, this article presents an improvement of the fail-safe counter for low-speed detection using a fail-safe digital counter in conjunction with a 500 kHz low-pass filter and a digital window comparator.

A test for dangerous failures of low-pass filters and windows comparator circuits with the FMEA method will be conducted. This compared the mean time to fail between the band-pass filter and the low-pass filter. The functionality circuits will else be tested with a computer simulation program.

Design Concept

The fail-safe principle for variable speed electric drive systems comprised simple safety principles and technologies with no CPUs or software and no failure by itself. Therefore, the design of a fail-safe circuit must be require the detection of false signals, examination of hardware circuit failure, and the calculation of confidence by using statistical methods. The improvement of the fail-safe counter for low-speed detection using a fail-safe digital counter in conjunction with a low-pass filter and a digital window comparator that has a block diagram concept is shown in Figure 2.

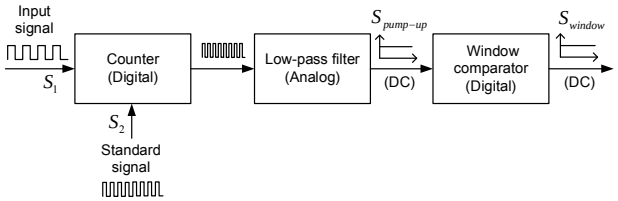

Fig. 2. The improvement of the fail-safe counter for the low-speed detection block diagram.

The basic structure of the counter is shown in Figure 1. The fail-safe counter has three inputs to the digital counter circuit. The S_1 is the square wave signal from the motor speed sensor, S_2 is a standard signal square wave signal with a frequency that is compared with S_1, and S_3 is a high-frequency square wave signal for the diagnosis.

The digital counter circuit uses presettable synchronous 4-bit binary counter ICs and 4-bit magnitude comparator ICs to compare the frequencies of the input S_1 from a speed sensor and S_2 from the standard signal. If the frequency f_1 is higher than f_2, then the output signal will be "0". The voltage output obtained from this circuit is given as a dynamic pulse signal. The diagnostic signal is the high signal obtained by the counted pulse signal of the safety counter, which divided the frequency by approximately 100 kHz.

In this article, it is proposed to change the diagnostics from a frequency of 100 kHz to a signal not exceeding the rated motor speed. Without using high frequency, this is inserted into the pulse signal. The improve counter circuit is shown in Figures 3 and results of the simulated waveforms are shown in Figures 4-5.

In Figures 4 and 5, the frequency of the output signal is equal to the frequency of the counted number of cycles, which has a low frequency that does not exceed the specified value. Therefore, in determining the pass frequency, the low-pass filter could be used.

The digital counter for low-speed detection is checked by a low-frequency signal and low-pass filter characteristics, which were provided for the low-pass filter only when both the diagnosis result was appropriate and the f_1 was lower than the f_2. Eventually, the DC signal was the output, as the low-speed detection result was in a fail-safe manner.

Although the f_o signal received from the digital counter does not have any error, in the FMEA analysis, other failures might be occur. Therefore, any established precautions would have to be analysed for signals that would not fail by filtering signals in both the frequency domain and the time domain.

The safety mechanism stated above would be the frequency window function in which the low-pass filter would operate. Additionally, the digital counter could provide the f_o frequency, which would pass through the frequency window under non-malfunctioning situations.

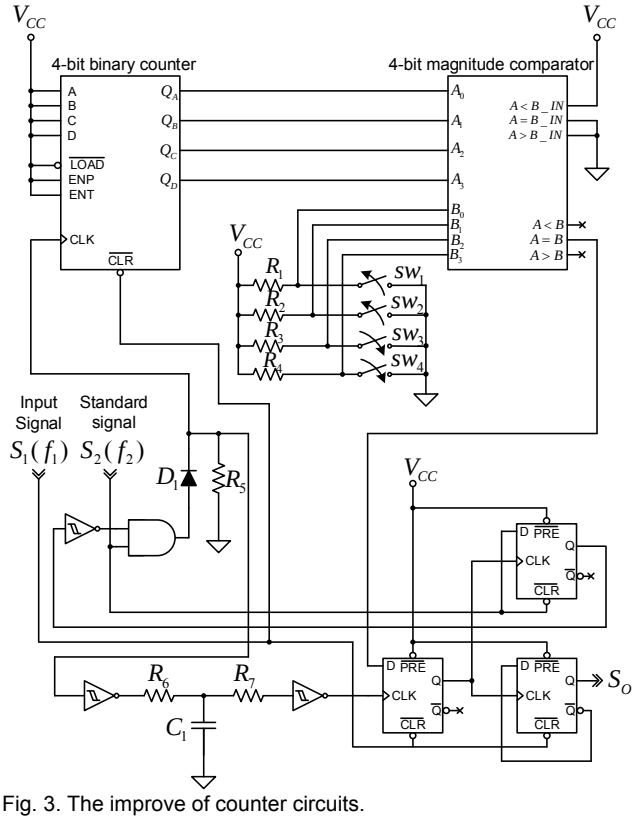

Fig. 3. The improve of counter circuits.

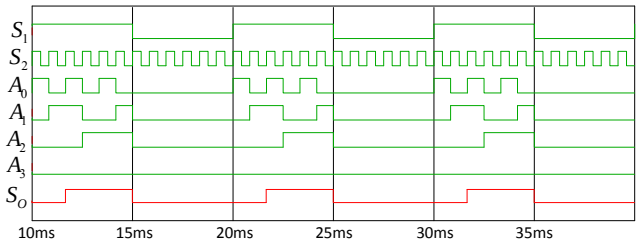

Fig. 4. The results of the simulated waveform diagram of the digital counter circuit; the frequency f_1 is lower than f_2 without S_3.

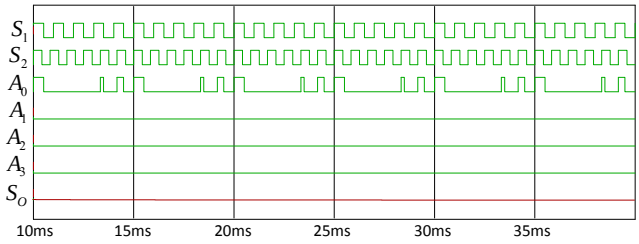

Fig. 5. The results of the simulated waveform diagram of the digital counter circuit; the frequency f_1 is higher than f_2 without S_3.

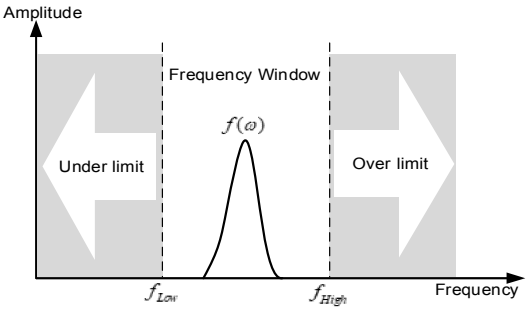

Fig. 6. The window frequency.

The frequency window for the low-speed sensing counter circuit is used in this case, as a low-pass filter that is used in conjunction with the charge pump circuit to raise the voltage over the supply voltage with the fo signal frequency. Whether the signal is lower or higher than the specified frequency could not be able to generate the voltage at the circuit output. The voltage obtained from the charging pump circuit had a voltage rating of 8 volts.

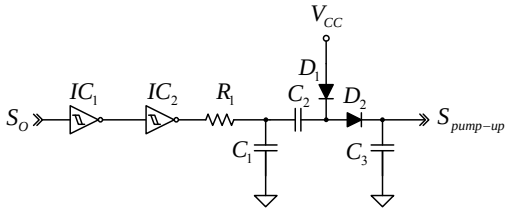

Fig. 7. The low-pass filter and charge pump circuit.

The frequency cut-off could be calculated by the passive RC low-pass filter as shown in Equation 1.

$$f_C = \frac{1}{2\pi R_1 C_1} \tag{1}$$

The detection of the signals in a time-domain manner is the detection of the voltage levels dividing by the signal level into the specified intervals.

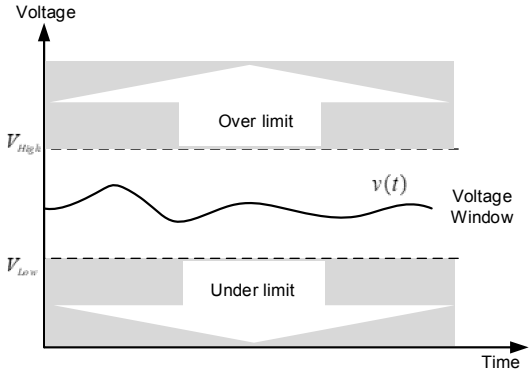

Fig. 8. The window voltage.

The window comparator circuit with the digital switching level [12-13] uses the differential of the threshold voltage, where the window boundary is between both threshold voltages. The input voltage in the range between the threshold level therefore has an output logic of “1”. The output logic is “0”, where the input voltage is higher or lower than the window boundary. The window boundary can be defined by Equation 2.

$$V_{T\_TTL}\left[\frac{R_1+R_2}{R_2}\right] < V_{in} < V_{T\_CMOS}\left[\frac{R_1+R_2}{R_2}\right] \tag{2}$$

where: V_{T_TTL} is the threshold voltages of TTL logic IC; V_{T_CMOS} is the threshold voltages of CMOS logic IC

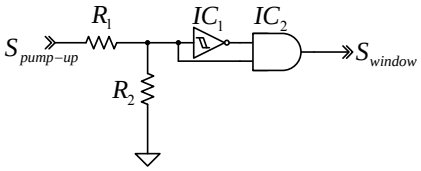

Fig. 9. The window comparator circuit with the digital switching level [13].

The IEC 61800-5-2 adjustable speed electrical power drive systems [1] are the standard for variable speed electric motor drives and testing of the equipment used in the system by the FMEA method. FMEA is a simulation of the failure of a system or device with reference to the IEC 60812 (analysis techniques for system reliability – procedure for the FMEA) [14] standard method. For example, the discrete semiconductors have two faults to consider that are the open circuit and short circuit between any connections.

In addition, reliability engineering is recognised as essential in military electronic systems. It is seen as a cost-reduction method in a factory where the inspection of redundant parts increases the ineffective cost, and where repair costs would include the effectiveness of the forced measurement in terms of the availability or size and sizing. As mentioned above, that the designed circuit had no dangerous failures, but in the order to verify the timing of the circuit to function without any failures, the mean time to failure would have to be calculated. This would be obtained from the sum of the failure rates of the electronic equipment (Military Handbook “Reliability Prediction of Electronic Equipment” (MIL-HDBK-217F)) [15]. As such, the mean time of failure [17] would be the approximation of the reliability at a time or inverse of the failure rate.

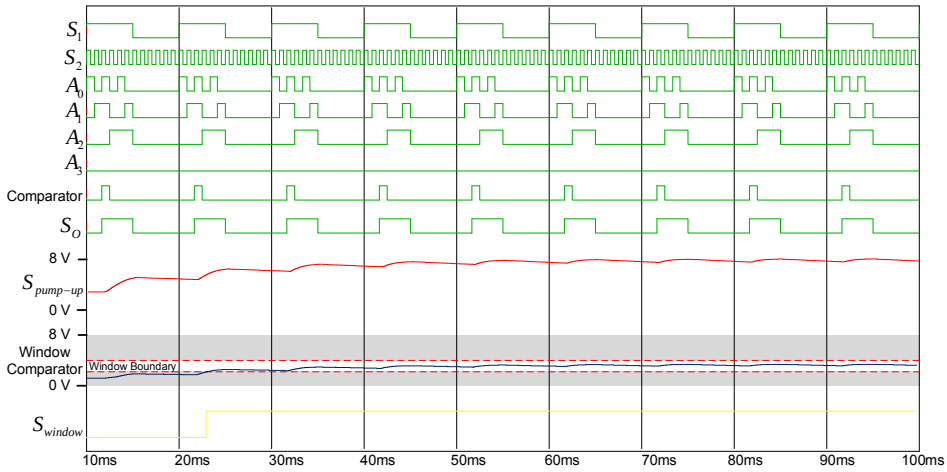

Fig. 10. The simulated waveform diagram of the normal condition.

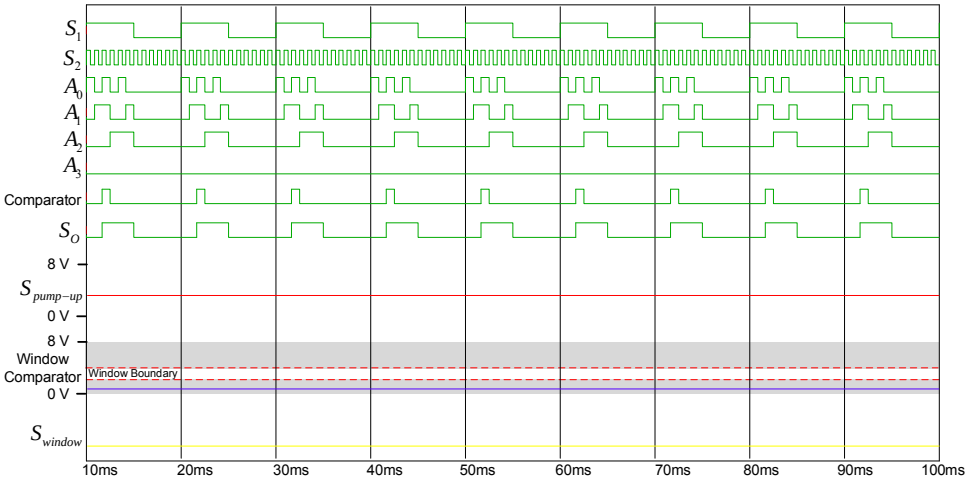

Fig. 11. The simulated waveform diagram of the fault situation over the speed limit.

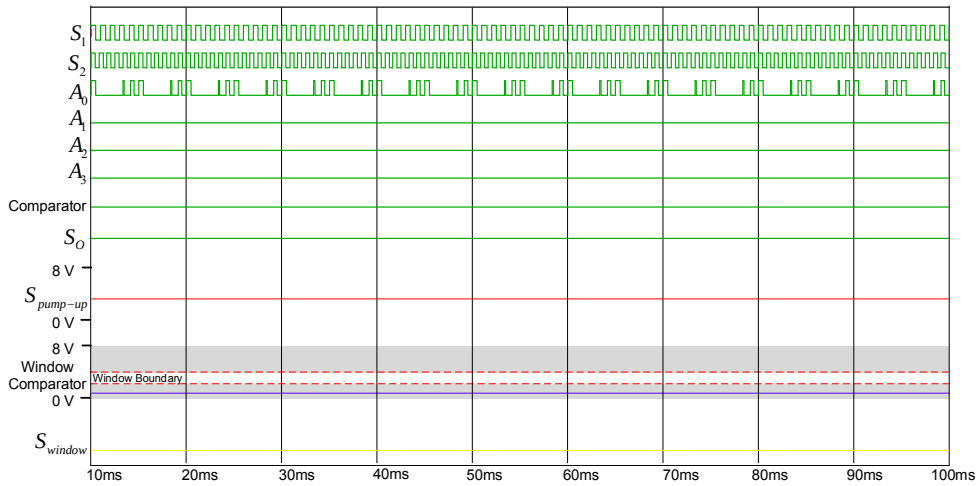

Fig. 12. The simulated waveform diagram of the fault situation in the low-pass filter and pump-up circuit single stuck-at 1 IC

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Result and Discussion

The performance and signal of the circuit were conducted by a computer simulation programme.

In normal conditions, the motor speed will not be greater than the rated speed, as the counter circuit work normally. Moreover, the output signal will be of a specified low frequency. Through the low-pass filter, this is a pulsed signal to excite the charging pump circuit, which would expand the voltage from 5 volts to 8 volts. The signal pass through a voltage divider circuit before entering the window comparator circuit, which is create the window boundary from the difference of the threshold voltage level with digital logic ICs to a constant voltage (depending on the ICs type). The output signal is given to Logic “1” (Figure 10).

If the input signal is greater than the specified standard failure conditions, the counter will not generate the signal to the low-pass filter circuit and no pulses will be fed to the charge pump circuit. Thus, there will be no voltage passing through the charge pump circuit resulting in a lower level than the window boundary. This resulted in the output signal to be a logic of “0” (Figure 11).

Other failures; such as, the fault situation in the low-pass filter and pump-up circuit single stuck-at 1 IC_1, which the resulting output signal is a logic of “0” (Figure 12).

For the determination of other circuit failures, the FMEA method can be used to calculate the effect of the failure and its effect.

Table 1. FMEA of the single failures in the low-pass filter and charge pump circuit.

Device	Failure Mode	Effect of the Failure	Remark
R_1	R x 0.5	Change of the circuit’s characteristic.	Δ
	R x 2	Change of the circuit’s characteristic.	Δ
	Short circuit	Output appears.	▲
	Open circuit	Output 4 V.	Δ
C_1	C x 0.5	Change of the circuit’s characteristic.	Δ
	C x 2	Change of the circuit’s characteristic.	Δ
	Short circuit	Output 3.8 V.	Δ
	Open circuit	Output appears.	▲
C_2	C x 0.5	Change of the circuit’s characteristic.	Δ
	C x 2	Change of the circuit’s characteristic.	Δ
	Short circuit	Output 4 V ripple 0.2V.	Δ
	Open circuit	Output 4 V.	Δ
C_3	C x 0.5	Change of the circuit’s characteristic.	Δ
	C x 2	Change of the circuit’s characteristic.	Δ
	Short circuit	No output signal.	Δ
	Open circuit	Output ripple 4-8V.	▲
D_1	Short circuit	Output 4.3 V.	Δ

	Open circuit	Output 0.9 V.	Δ
D_2	Short circuit	Output ripple 4.2-3.6V.	Δ
	Open circuit	Output 3.9 V.	Δ
IC_1	Struck at 1	Output 5 V.	Δ
	Struck at 0	Output 3.5 V.	Δ
	Open fault	Output 3.5 V.	Δ
IC_2	Struck at 1	Output 3.5 V.	Δ
	Struck at 0	Output 3.5 V.	Δ
	Open fault	Output 3.5 V.	Δ

Remark : Δ: no significant consequences; ▲: abnormal condition.

Table 2. FMEA of the single failures in the window comparator circuit with the digital switching level.

Device	Failure Mode	Effect of the Failure	Remark
R_1	R x 0.5	Change of the circuit's characteristic.	Δ
	R x 2	Change of the circuit's characteristic.	Δ
	Short circuit	No output signal.	Δ
	Open circuit	No output signal.	Δ
R_2	R x 0.5	Change of the circuit's characteristic.	Δ
	R x 2	Change of the circuit's characteristic.	Δ
	Short circuit	No output signal.	Δ
	Open circuit	No output signal.	Δ
IC_1	Struck at 1	No output signal.	Δ
	Struck at 0	No output signal.	Δ
	Open fault	No output signal.	Δ
IC_2 pin1	Struck at 1	Output appears.	▲
	Struck at 0	No output signal.	Δ
	Open fault	No output signal.	Δ
IC_2 pin2	Struck at 1	No output signal.	Δ
	Struck at 0	No output signal.	Δ
	Open fault	No output signal.	Δ

Remark : Δ: no significant consequences; ▲: abnormal condition.

In Tables 1 and 2, the FMEA of the single failures in the low-pass filter and charge pump circuit and single FMEA for the low-frequency filter and the window comparator circuit with the digital switching level showed that the element device values increased and decreased. This changed the circuit's characteristics but did not fail the operation of the circuit. A semiconductor device was used for the short-circuit and open-circuit test according to the characteristic of the semiconductor device failure. Digital IC devices also tested the open and high or low logic of the input pin.

The low-pass filter and charge pump circuit were designed to filter the frequencies higher than the rated cycle. In this case, this was set at a motor speed of 300 rpm, and the pump-up voltage in the normal operating range of 6 - 8 volts. Table 1 shows the single failure of the circuit according to the FMEA (IEC 61800-5-2:2007) method. There were three cases of abnormal conditions in this circuit:

1) Short circuit on R_1 would obtain the output signal. Since the circuit would work normally, the filtering properties would be higher. When a high-frequency failure occurred, the circuit would function normally.

2) Opening of the circuit at C_2 would have the same result as in case 1.

In the two cases mentioned above, the failure would only affect the low-pass filters and charge pump circuit. However, it would not affect the system's output since the signal to the low-pass filter would pass through the fail-safe counter.

3) Opening of the circuit at C_3 would prevent the output frequency filtering. The output signal would be 4-8 volts pulse signal, thus allowing it to pass through the passage of the window comparator circuit.

The window comparator circuit with the digital switching level define the window boundary according to the threshold voltage level using a resistor voltage divider to set the voltage level within the window boundary. From Table 2, there was only one abnormal failure: the input pin 1 of the AND gate that was stuck at Logic 1. This caused the resulting output signal to be Logic 1 throughout, which was a dangerous failure.

To confirm the safety of the circuit operation, the failure time value can be calculated to verify the time the circuit could operate. This would be obtained from the sum of the failure rates of the electronic equipment (Table 3).

Table 3. The failures of the electronic equipment.

No	Components	Failure Rate (10^{-6}h)
1	CMOS digital gate	0.15
2	Diode	0.17556
3	Resistor	0.01395
4	Capacitor	0.0286

The failure rate of the low-pass filter and charge pump circuit could be calculated by the sum of the failure rate (Equation 3).

$$\lambda = 6.6195 \times 10^{-6} hr \quad (3)$$

The failure rate of the window comparator circuit with the digital switching level could be calculated by the sum of the failure rate (Equation 4).

$$\lambda = 3.0279 \times 10^{-6} hr \quad (4)$$

The overall failure rate was shown in Equations 3 and 4, and the mean time to the failure of the low-pass filter and charge pump circuit was shown in Equation 5.

$$MTTF = 151{,}068hr = 17.24y \quad (5)$$

The mean time to the failure of the window comparator circuit with the digital switching level was shown in Equation 6.

$$MTTF = 330{,}261hr = 37.70y \quad (6)$$

The calculated mean time to failure would guarantee that the circuit would operate without errors from itself. Therefore, in normal conditions, the low-pass filter and charge pump circuit could operate without failure for 151,068 hours or 17.24 years, and the window comparator circuit with digital switching level could operate without failure for 330,261 hours or 37.70 years.

Conclusion

The improvement of a fail-safe counter for low-speed detection required a simple operation without any use of CPUs and simple calculation of the circuit. However, the safety model would be required for the fail-safe counter, as it would be an important feature in which the safety functions would be attained primarily by structural measures; namely, in an inherently safe manner.

A low-speed detection method by a fail-safe counter was proposed. Specific features of this proposed method were the adoption of digital counter circuits for the detection of low-speed, the diagnosis of the digital counter circuit, and its result output as dynamic signals to a low-pass filter and a charge pump circuit, as well as an additional diagnosis of a fail-safe window comparator which evaluated the DC signal level from the charge pump circuit. These diagnoses were regarded as the frequency domain and time domain. When the motor speed became lower than the predetermined speed and there were no parts of the digital counter circuit malfunctioning, the dynamic signals with the

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REFERENCES

[1] IEC 61800-5-2:2007, adjustable speed electrical power drive systems - Part 5-2: Safety requirements - Functional.

[2] S. Deeon, Y. Hirao and K. Futsuhara, “A Fail-safe Counter and its Application to Low-speed Detection”, Transactions of Reliability Engineering Association of Japan, Vol.33, No.3, pp.135-144, 2011.

[3] J. Marcos, E. Mandado and C.M. Penalver, “Implementation of fail-safe control systems using programmable logic controllers.” Proceeding of International Conference on Industrial Automation and Control, 1995 (IA&C'95). Hyderabad, India. 5-7 Jan 1995. pp. 395 – 400.

[4] K. Otake, Y. Hirao, T. Fukuda and K. Futsuhara, “A Safety Relay with Contacts in a safe Operational Order and Its Application.” Proceeding of The 6th International Conference on Safety of Industrial Automated Systems. New York. 13-15 Sep 2010. pp.1-6.

[5] S. Deeon, Y. Hirao and K. Tanaka, “A Relay Drive Circuit for a Safe Operation Order and its Fail-safe Measures.” The journal of Reliability Engineering Association of Japan. Vol. 34, no.7. July 2012. pp. 489–500.

[6] C.Summatta and S. Deeon, “Simple anti capacitor open-circuit self-oscillation in a CMOS schmitt trigger-invertor oscillator circuit.” Przeglad Elektrotechniczny. Vol. 95, no.3. Mar 2019. pp. 97–100.

[7] S.Wongcharoen and S.Deeon “Multi-level swell voltage control for minimizing the damage to an on-grid system.” Indonesian Journal of Electrical Engineering and Informatics (IJEEI). Vol. 8, no.2. June 2020. pp. 306–319.

[8] S.Wongcharoen, S.Deeon and N. MUNGKUNG, “ Application of Electronic Load Circuit for Electrical Safety by using a Serial Mode Comparator.” Przeglad Elektrotechniczny. Vol. 96, no.4. Apl 2020. pp. 17–22.

[9] S.Wongcharoen and S.Deeon “Application of Multi-Stage Window Comparator Circuit with Safety Mode for Swell Voltage Control in Low Voltage Systems.” Przeglad Elektrotechniczny. Vol. 96, no.5. May 2020. pp. 84–90.

[10] V. A. Pedroni, “Low-voltage high-speed Schmitt trigger and compact window comparator.” Electronics Letters. Vol. 41, vol.22. pp. 1213–1214.

[11] P. Sagar, and M. Panicker P. R., “A Novel High Speed Window Comparator Circuit.” International Conference on Circuit Power and Computing Technologies (ICCPCT). pp. 691 – 693.

[12] C. Summatta, and S. Deeon, “A Window Comparator Circuit with Digital Switching Level,” in The 9th International Conference on Sciences, Technology and Innovation for Sustainable Well-Being(STISWB 2017), China, pp. 74-78.

[13] C.Summatta and S. Deeon, “Design and Analysis of 2oo3 Static Voter for SMT function in an Adjustable Speed Electrical Power Drive System.” Journal of Telecommunication, Electronic and Computer Engineering (JTEC). Vol. 11, no.1. Jan 2020. pp. 1–6.

[14] IEC 60812, Analysis techniques for system reliability – Procedure for failure mode and effects analysis (FMEA) Second edition 2006-01, 2006

[15] MIL-HDBK-2 17F, Military handbook reliability prediction of electronic equipment, U.S. Department of Defense, 1991.

[16] J. C. Whitaker, The electronics handbook, 2nd ed., Taylor & Francis Group, LLC, 2005, pp. 687-693.

[17] M. Krasich, “How to estimate and use MTTF/MTBF would the real MTBF please stand up?,” in Reliability and Maintainability Symposium, Jan. 2009, pp. 353-359.