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Multi-input Memristor Rationed Logic Full Adder Circuit for Efficient Processing Time

Abstract. *This research proposes a multi-input memristor rationed logic (MRL) 1-bit full adder circuit as an alternative to conventional multi-stage MRL full adders. The proposed multi-input 1-bit full adder circuit consisted of 25 memristors without CMOS transistor. Ripple carry adder was utilized to realize multi-input MRL 8-bit full adder circuit by cascading eight blocks of multi-input MRL 1-bit full adder. The advantages of the multi-input MRL 8-bit full adder include straightforwardness, compactness, and improved delay time. Simulations were carried out by using LTspice simulator and results compared with multi-stage full adders. The multi-input MRL 8-bit full adder circuit achieved higher processing-time efficiency and thereby holds great potential as an alternative to multi-stage full adders. The novelty of this research lies in the use of multi-input MRL technique to realize full adder circuits that effectively mitigate voltage degradation and improve delay time.*

Streszczenie. *Badania te proponują wielowejściowy układ memristor rationed logic (MRL) 1-bitowego pełnego sumatora jako alternatywę dla konwencjonalnych wielostopniowych sumatorów MRL. Proponowany wielowejściowy 1-bitowy układ pełnego sumatora składał się z 25 memrystorów bez tranzystora CMOS. Sumator przenoszenia Ripple został wykorzystany do realizacji wielowejściowego 8-bitowego pełnego sumatora MRL poprzez kaskadowanie ośmiu bloków wielowejściowego 1-bitowego pełnego sumatora MRL. Zalety wielowejściowego, 8-bitowego pełnego sumatora MRL obejmują prostotę, zwartość i poprawiony czas opóźnienia. Symulacje przeprowadzono przy użyciu symulatora LTspice, a wyniki porównano z wielostopniowymi pełnymi sumatorami. Obwód wielowejściowego 8-bitowego pełnego sumatora MRL osiągnął wyższą wydajność w czasie przetwarzania, a tym samym ma ogromny potencjał jako alternatywa dla wielostopniowych pełnych sumatorów. Nowość tych badań polega na wykorzystaniu wielowejściowej techniki MRL do realizacji pełnych obwodów sumatorów, które skutecznie łagodzą degradację napięcia i poprawiają czas opóźnienia. (**Wielowejściowy układ logiczny Memristor racjonowany z pełnym sumatorem dla wydajnego czasu przetwarzania***)*

Keywords: memristor, logic gate, full adder, multi-input, processing time
Słowa kluczowe: układ logiczny, memristor, sumator.

Introduction

Just as modern CMOS transistors are encountering miniaturization limitations, integrated circuits (IC) could no longer accommodate exponential growth in elemental devices. The predicament presages the end of Moore's Law [1] and thus necessitates the development of alternative circuit architectures that require minimal number of CMOS transistors. As a result, IC realization techniques requiring fewer CMOS transistors were proposed [2]–[5]. In [6], a technique was proposed to embed logics in memory circuits, and [7] deployed memristors as logic gates.

Memristors first emerged in 1971 and have been used as a passive element [8]. The memristor device possesses the characteristics of pinched heterolysis loop based on the relationship between electric charge and magnetic flux [9]. The characteristics render memristor devices suitable for logic gates and memory circuits [10, 11].

A typical memristor consists of two layers of thin titanium dioxide (TiO2) inserted between two metal electrodes. The upper layer is doped TiO2-x functioning as electrical conductivity (positive polarity), and the lower layer is neat TiO2 (undoped TiO2) as electrical insulation (negative polarity). Applying positive voltage input to positive polarity alters the resistance of memristor to minimum resistance (R_{on}), while applying positive voltage input to negative polarity changes the resistance of memristor to maximum resistance (R_{off}).

There exist three commonly used memristor-based logic gates: material implication (IMPLY) [12], memristor aided logic (MAGIC) [13], and memristor rationed logic (MRL) [14]. By comparison, MRL possesses significantly less complex computational steps and enjoys ease of fabrication. This research thus utilized MRL gates (rather than IMPLY and MAGIC) to substitute CMOS-based logic gates.

The MRL technology replaces CMOS transistors with memristors and thus enables the realization of denser and more scalable circuit architectures. However, conventional multi-stage MRL logic gate circuits suffer from voltage degradation, and the situation becomes more severe with increase in cascading [15-16]. To mitigate voltage degradation, this study employed multi-input MRL principle in realizing logic gates. Typically, logic gates are derived from Boolean algebra equations and could be customized to specific needs.

Full adder circuits play an essential role in digital circuits and memory [17]. In addition to multi-input MRL logic gates, this research utilized the multi-input MRL principle in realizing full adder circuits. The multi-input full adders are straightforward and involve fewer computational steps, vis-à-vis multi-stage full adder circuits.

In practice, the delay time of MRL circuits is largely attributable to CMOS transistors. As a result, a reduction in CMOS transistors in the circuit contributes to improved delay time, as evidenced by simulation results of the proposed multi-input MRL full adder circuits. Specifically, this research proposed multi-input MRL full adder circuits to improve delay time and mitigate voltage degradation.

The organization of this research is as follows: Section 1 is the introduction. Section 2 describes AND and OR logic gates, conventional multi-stage and proposed multi-input MRL circuits. Section 3 details the proposed multi-input MRL 1- and 8-bit full adder circuits, and Section 4 discusses the LTspice simulation results of the multi-input MRL 1- and 8-bit full adder circuits, in comparison with existing full adders. The concluding remarks are provided in Section 5.

Memristor-based logic gates and MRL circuits

Just as modern CMOS transistors are encountering miniaturization limitations, integrated circuits (IC) could no longer accommodate exponential growth in elemental devices. The predicament presages the end of Moore's Law [1] and thus necessitates the development of alternative circuit architectures that require minimal number of CMOS transistors. As a result, IC realization techniques requiring fewer CMOS transistors were proposed [2]–[5]. In [6], a

technique was proposed to embed logics in memory circuits, and [7] deployed memristors as logic gates.

Memristor-based AND and OR gates

and positive voltage input was fed through negative polarity, as shown Fig. 1(a). In Fig. 1(a), if the voltage input (V1 and V2) were HIGH, the resistance of the memristors (U1 and U2) would increase. Meanwhile, the OR gate design required connecting the negative polarity of two memristors and negative voltage input was fed through positive polarity, as illustrated Fig. 1(b). In the figure, if the voltage input (V1 and V2) were HIGH, the resistance of the memristors (U1 and U2) would decrease. voltage input (V1 and V2) were HIGH, the resistance of the memristors (U1 and U2) would decrease.

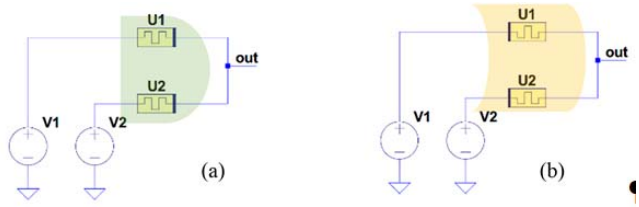

Fig. 1 Two-input MRL gates: (a) AND gate, (2) OR gate [9]

The relationship in Fig. 1 can be mathematically expressed in equation (1), where R1 is the resistance of memristor U1 and R2 is the resistance of memristor U2.

(1) $$V_{out} = V_1 \frac{R_1}{R_1 + R_2}$$

Conventional multi-stage MRL full adder circuit

In the conventional (multi-stage) MRL full adder, the logics of logic gates could be mathematically expressed in equations (2) – (3). Equation (2) is XOR logic gate, and equation (3) is carry-out logic gate. Fig. 2 illustrates the multi-stage half adder circuit based on XOR and carry-out logic circuit.

(2) $$sum = \overline{A}B + A\overline{B}$$

(3) $$C_{out} = AB$$

Equations (4) and (5) are logics of the multi-stage memristor-based full adder circuit. Fig. 3 illustrates the multi-stage full adder circuit based on sum and carry-out logics of full adder.

(4) $$sum = C_{in}\left(AB + \overline{A}\overline{B}\right) + C_{in}\left(\overline{A}B + A\overline{B}\right)$$

(5) $$C_{out} = AB + BC_{in} + AC_{in}$$

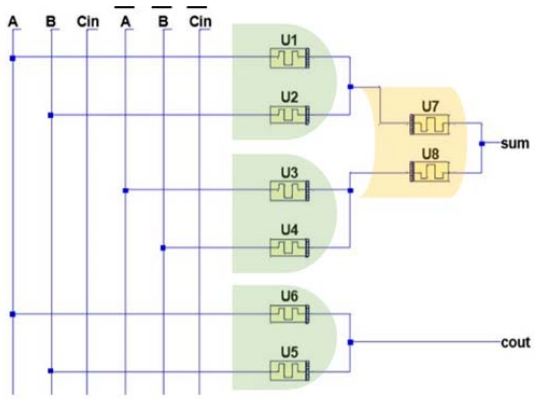

Fig. 2 Multi-stage memristor-based half adder circuit

The inherent problem of multi-stage memristor-based devices lies in voltage degradation, and the degradation becomes more severe as the number of stages is increased. To demonstrate voltage degradation inherent in multi-stage memristor-based devices, Fig. 4(a) illustrates a two-stage AND/OR logic circuit with four-input nodes: A, B, C, and D. In Fig. 4(a), given the voltage input of A= HIGH, B = HIGH, C = LOW, and D = LOW, the voltage output was approximately 0.67HIGH (equation (6)). Fig. 4(b) depicts the two-stage AND/OR logic circuit in operation where the resistance of U1, U2, and U6 were altered to R_{off} and that of U3, U4, and U5 to R_{on}.

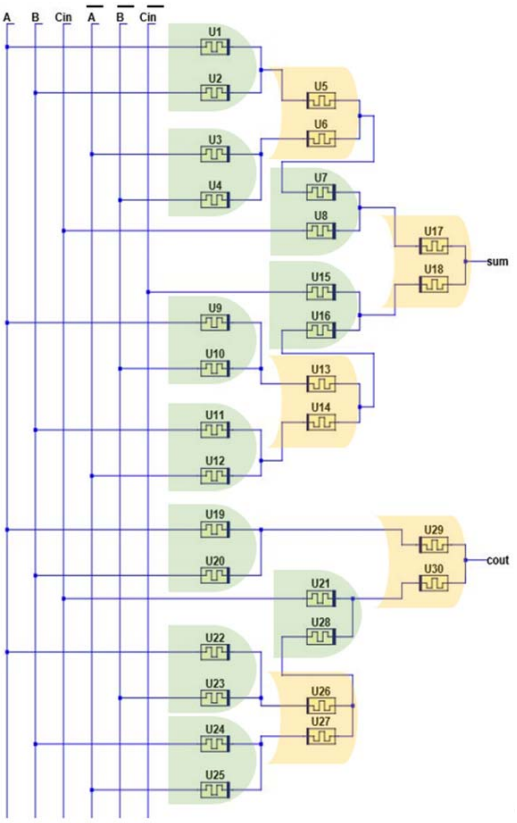

Fig. 3 Multi-stage memristor-based full adder circuit

The voltage output of two-stage AND/OR logic circuit with four-input nodes can be mathematically written in equation (6). In the equation, the voltage output is approximately 0.67HIGH. To improve the voltage output of the two-stage AND/OR logic circuit, the minimum (R_{on1}) and maximum resistance (R_{off1}) of AND gate were set at 100 and 10k, and the corresponding (R_{on2} and R_{off2}) of OR gate at 100 and 100k. The improved voltage output of the two-stage AND/OR logic circuit was 0.91HIGH, as shown in equation (7).

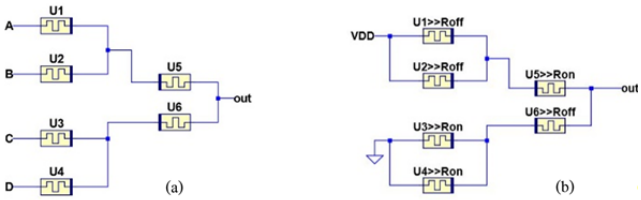

Fig. 4 Multi-stage memristor-based circuits: (a) two-stage AND/OR logic circuit, (b) two-stage logic circuit functioning

In this research, the realization of multi-input MRL 1-bit full adder circuit involved two stages of memristor logic circuits. This sub-section was thus focused on two-stage logic circuits. Besides, equation (7) would be utilized in realizing the proposed multi-input MRL 1-bit full adder.

(6) $$V_{out} = \frac{1/2R_{on} + R_{off}}{1/2R_{on} + R_{off} + 1/2R_{off} + R_{on}} V_{high}$$

$$V_{out} \approx \frac{2}{3} V_{high}$$

(7) $$V_{out} = \frac{1/2R_{on2} + R_{off\,2}}{1/2R_{on2} + R_{off\,2} + 1/2R_{off\,1} + R_{on1}} V_{high}$$

$$V_{out} \approx 0.91 V_{high}$$

Multi-input MRL full adder circuit

In this research, the proposed multi-input (N-input) MRL AND and OR gates were realized based on the two-input MRL circuits (Fig. 1), as respectively shown in Figs. 5(a) and (b). In Fig. 5(a), if a given voltage input of the multi-input MRL AND gate were LOW, the voltage output would be LOW. The voltage output of multi-input MRL AND gate is mathematically expressed in equation (8), where N is the number of memristors of multi-input MRL AND gate which is determined by the resistance ratio of R_{off} to R_{on} ($\frac{R_{off}}{R_{on}} + 1$).

In Fig. 5(b), if a given voltage input of the multi-input MRL OR gate were HIGH, the voltage output would be HIGH. The voltage output of multi-input MRL OR gate is mathematically expressed in equation (9), where N is the number of memristors of multi-input MRL OR gate which is determined by the resistance ratio of R_{off} to R_{on} ($\frac{R_{off}}{R_{on}} + 1$).

Fig. 6 shows the simulated voltage output of multi-input MRL AND and OR gates, given four voltage inputs.

(8) $$V_{out} = \frac{R_{on}}{R_{on} + \frac{R_{off}}{N-1}} V_{high} \simeq V_{high} \Rightarrow N << \frac{R_{off}}{R_{on}} + 1$$

(9) $$V_{out} = \frac{\frac{R_{off}}{N-1}}{R_{on} + \frac{R_{off}}{N-1}} V_{high} \simeq V_{high} \Rightarrow N << \frac{R_{off}}{R_{on}} + 1$$

Multi-bit Full Adder Circuit Using Ripple Carry Adder

In this research, the multi-input MRL 8-bit full adder was realized by cascading the multi-input MRL 1-bit full adder circuits using ripple carry adder (RCA). In practice, there are two commonly used adder cascading methods: RCA and carry-lookahead adder (CLA). By comparison, CLA requires a greater number of elemental devices, giving rise to fabrication challenges and cost-ineffectiveness. Besides, the computation complexity of CLA exponentially increases with increase in cascading. As a result, this study utilized RCA in realizing the proposed multi-input MRL 8-bit full adder circuit. Nonetheless, the realization of the 8-bit full adder circuit required 180 nm CMOS transistors.

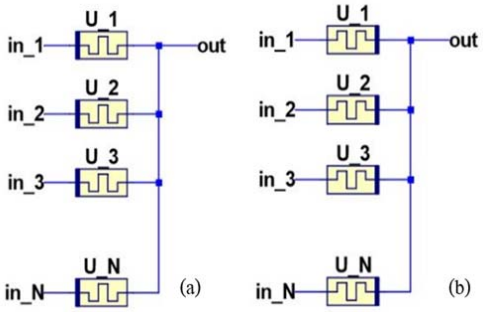

Fig. 5 The proposed multi-input MRL gates: (a) multi-input AND gate, (b) multi-input OR gate

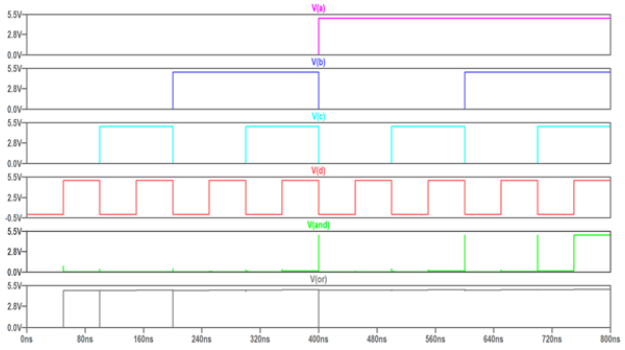

Fig. 6 Simulated voltage outputs of multi-input MRL AND and OR gates, given four voltage inputs

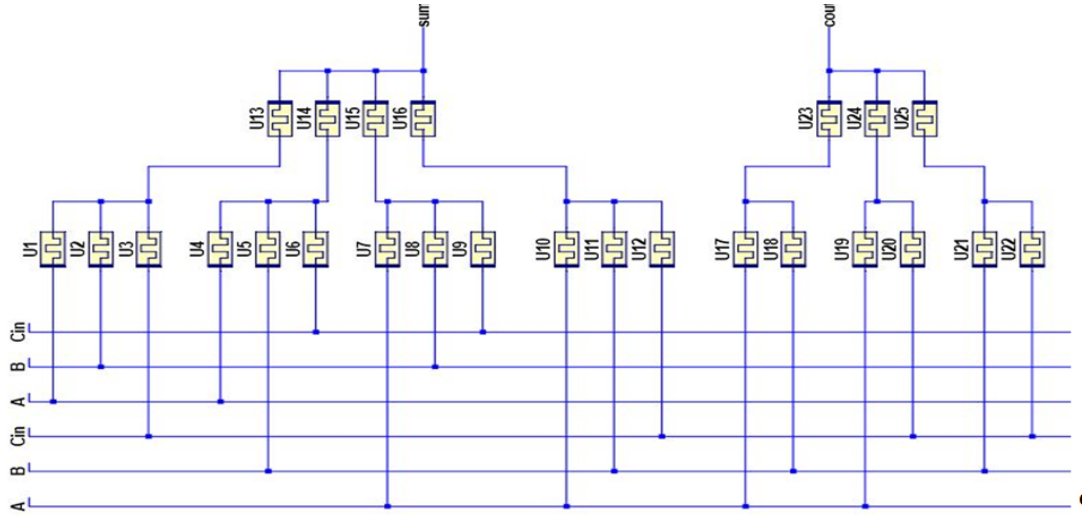

Fig . 7 The proposed multi-input MRL 1-bit full adder circuit consisting of 25 memristors

Table 1 The voltage input A, B, C_{in}, and voltage output of the multi-input MRL 1-bit full adder

Voltage Input					Voltage Output	
A	B	C_{in}	Memristor (R_{int} to R_{on})	Memristor (R_{int} to R_{off})	Sum	Carry out
LOW	LOW	LOW	U1, U2, U4 ,U6, U8, U9, U13, U14,U15	U3, U5, U7, U10, U11, U12, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25	LOW	LOW
LOW	LOW	HIGH	U1, U2, U3, U4, U8, U12, U13, U14, U16, U21, U22, U24, U25	U5, U6, U7, U9, U10, U11, U17, U18, U19, U20, U13	HIGH	LOW
LOW	HIGH	LOW	U1, U4, U5, U6, U9, U10, U11, U13, U14, U15, U16, U18, U21, U23, U25	U2, U3, U7, U8, U17, U19, U20 U22, U24	HIGH	LOW
LOW	HIGH	HIGH	U1, U3, U4, U5, U11, U12, U13, U14, U16, U18, U20, U21, U22, U23, U24, U25	U2, U6, U7, U8, U9, U10, U15, U17, U19	LOW	HIGH
HIGH	LOW	LOW	U2, U6, U7, U8, U9, U10, U13, U14, U15, U16, U17, U19, U23, U24	U1, U3, U4, U5, U11, U12, U18, U20, U21, U22, U25	HIGH	LOW
HIGH	LOW	HIGH	U2, U3, U7, U8, U10, U12, U13, U15, U16, U17, U19, U20, U22, U23, U24, U25	U1, U4, U5, U6, U9, U11, U14, U18, U21	LOW	HIGH
HIGH	HIGH	LOW	U5, U6, U7, U9, U10, U11, U14, U15, U16, U17, U18, U19, U21, U23, U24, U25	U1, U2, U3, U4, U8, U12, U13, U20, U22	LOW	HIGH
HIGH	HIGH	HIGH	U3, U5, U7, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25	U1, U2, U4, U6, U8, U9	HIGH	HIGH

Multi-input MRL Full Adder Circuits

Multi-input MRL 1-bit full adder circuit

Unlike the conventional multi-stage MRL full adder, the proposed multi-input MRL 1-bit full adder circuit requires no simplification of logic equation. Sum of maxterms was used in the multi-input MRL 1-bit full adder. In this research, the number of memristors (U1-U25) and delay time of sums of maxterms and minterms were identical.

The sum and carry-out logics of the multi-input MRL 1-bit full adder circuit were mathematically expressed in equations (10) and (11). The proposed multi-input MRL 1-bit full adder circuit consisted of 25 memristors (U1-U25) without CMOS, as shown in Fig. 11. In the figure, U1-U12 and U17-U22 were memristors of OR gate where R_{on} = 100 ohm and R_{off} = 10k ohm, while the rest (U13-U16 and U23-U25) were memristors of AND gate where R_{on} = 100 ohm and R_{off} = 100k ohm.

$$sum = (\overline{A}+\overline{B}+C_{in})\bullet(\overline{A}+B+\overline{C_{in}})\bullet(A+\overline{B}+\overline{C_{in}})\bullet(A+B+C_{in}) \quad (10)$$

$$C_{out} = (A+B)\bullet(A+C_{in})\bullet(B+C_{in}) \quad (11)$$

Table 1 tabulates the voltage input ($A, B, C_{in}, \overline{A}, \overline{B}, \overline{C}_{in}$), R_{on}, R_{off}, and voltage output of the proposed multi-input MRL 1-bit full adder circuit (Fig. 11). For example, given A= LOW, B = LOW, C_{in} = LOW, $\overline{A}$ = HIGH, $\overline{B}$ = HIGH, $\overline{C}_{in}$ = HIGH (i.e., scenario 1), the resistance of U1, U2, U4, U6, U8, U9, U13, U14, and U15 became R_{on}, while that of the rest became R_{off}. The sum and carry out were LOW. In scenario 2, given A= LOW, B = LOW, C_{in} = HIGH, $\overline{A}$ = HIGH, $\overline{B}$ = HIGH, $\overline{C}_{in}$ = LOW, the resistance of U1, U2, U3, U4, U8, U12, U13, U14, U16, U21, U22, U24, and U25 became R_{on}, while that of the rest became R_{off}. The sum was HIGH and the carry out was LOW.

The proposed multi-input MRL 1-bit full adder circuit involved two computational stages (Fig. 7). Since the proposed 1-bit adder circuit contained only two stages, the delay time of the adder was predominantly attributable to the switching of memristor resistance from R_{on} to R_{off} and from R_{off} to R_{on} (Table 1). The voltage output (sum and carry out) of the 1-bit full adder was between 0V-5V.

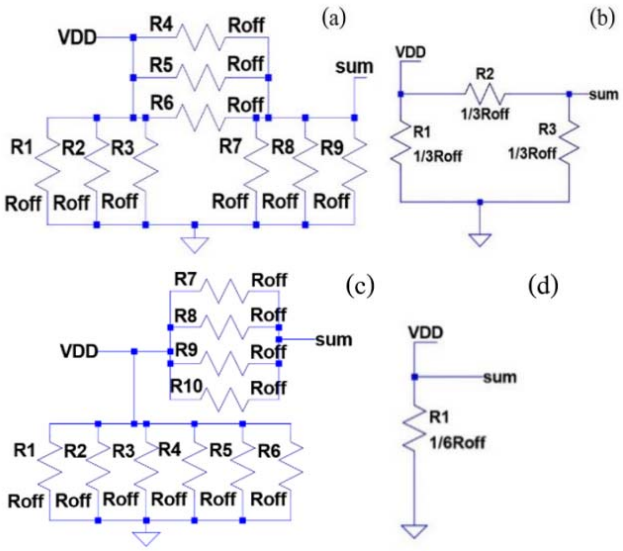

Fig. 8 The equivalent circuit of the multi-input MRL 1-bit full adder: (a) even number of HIGH, (b) simplified equivalent circuit given even number of HIGH, (c) odd number of HIGH, (d) simplified equivalent circuit odd number of HIGH

Figure 8(a) illustrates the equivalent circuit of the multi-input MRL 1-bit full adder, given the even number of HIGH voltage input (scenarios 1, 4, 6, 7), and Fig. 8(b) shows the corresponding simplified equivalent circuit of the proposed

1-bit full adder. The simplified equivalent circuit (Fig. 8 (b)) could be mathematically expressed in equation (12). Meanwhile, Fig. 8(c) depicts the equivalent circuit of the multi-input MRL 1-bit full adder, given the odd number of HIGH voltage input (scenarios 2, 3, 5, 8), and Fig. 8(d) shows the corresponding simplified equivalent circuit of the proposed 1-bit full adder.

$$\frac{sum-5}{1/3}+\frac{sum}{1/3}=0\,,\ \text{where } R_{on}\approx 0 \tag{12}$$

$$sum = 0.45V$$

Multi-input MRL 8-bit full adder circuit

The multi-input MRL 8-bit full adder circuit was realized by cascading eight blocks of the multi-input 1-bit full adder using ripple carry adder. Existing CMOS-based 8-bit full adders required approximately 400 CMOS transistors [20, 21], while multi-stage MRL 8-bit full adders were proposed for further development into processing units [22]. On the other hand, this current research proposed an 8-bit full adder circuit based on multi-input MRL principle.

In Fig. 9, a direct connection between $C_{o[N-1]}$ and $C_{in[N]}$ resulted in voltage degradation. As a result, four CMOS transistors were required between $C_{o[N-1]}$ and $C_{o[N]}$ to mitigate voltage degradation. Specifically, the proposed multi-input MRL 8-bit full adder circuit consisted of eight blocks (blocks 1-8) of 1-bit full adders with four CMOS transistors per block, except for the final block (block 8). The number of memristors and CMOS transistors of multi-input MRL N-bit full adder could be determined by equations (13) and (14). The propagation delay (T_{pd}) of the multi-input MRL 8-bit adder circuit involved four steps: two steps for 1-bit full adder block and two steps for CMOS transistors except for the final block, as mathematically expressed in equation (15).

$$memristor = 25N \tag{13}$$

$$CMOS = 4(n-1) \tag{14}$$

$$T_{pd[N]} = 2nT_{mem} + 2T_{CMOS}(N-1) \tag{15}$$

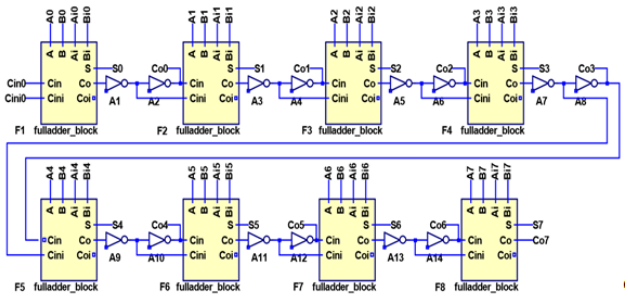

Fig. 9 The proposed multi-input MRL 8-bit full adder circuit consisting of eight blocks of 1-bit full adders with CMOS inverters

Simulation Results

The proposed multi-input MRL 1-bit full adder circuit was simulated by LTspice simulation software, given the threshold memristor model [18] and 180 nm CMOS transistors. Fig. 10 illustrates the simulated voltage output (sum and carry out) of the multi-input MRL 1-bit full adder circuit given six voltage inputs, based on Fig. 10 and Table 1.

Table 2 tabulates the number of devices of logic gates, multi-stage MRL 1-bit full adders, and multi-input MRL 1-bit full adder circuit. The conventional multi-stage MRL 1-bit full adder contained 30 memristors and 8 CMOS transistors, while the proposed multi-input MRL 1-bit full adder circuit required 25 memristors without CMOS transistor. Nevertheless, the realization of multi-input MRL 8-bit full adder circuit required 4 CMOS transistors in each 1-bit full adder block (blocks 1-7) except for the final block (block 8), resulting in 28 CMOS transistors in the 8-bit full adder circuit (Table 3). By comparison, the significantly lower number of CMOS transistors in the proposed multi-input MRL 8-bit full adder circuit enhanced the processing speed and shortened delay time..

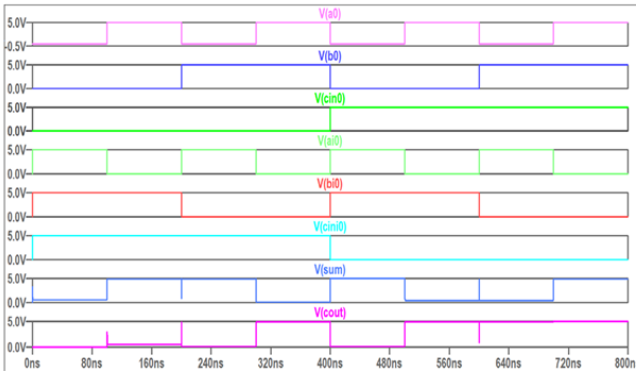

Fig. 10 Simulated voltage output (sum and carry out) of multi-input MRL 1-bit full adder circuit given six voltage inputs

Table 2 Number of devices of logic gates, multi-stage MRL 1-bit full adders, and multi-input MRL 1-bit full adder circuit

	Memristor	CMOS transistor
NOT gate	0	2
AND gate	2	0
OR gate	2	0
NAND gate	2	2
NOR gate	2	2
Multi-stage MeMOS logic-based full adder [16]	18	20
Multi-stage NAND gate-based full adder [23]	18	18
Conventional multi-stage MRL full adder	30	8
Proposed multi-input MRL 1-bit full adder circuit	25	0

Table 3 Number of devices of multi-stage and multi-input MRL 8-bit full adder circuit

	Memristor	CMOS transistor
Multi-stage MeMOS logic-based full adder [16]	144	160
Multi-stage NAND gate-based full adder [23]	144	144
Conventional multi-stage MRL full adder	240	64
Proposed multi-input MRL 8-bit full adder circuit	200	28

Table 4 compares the rise time (T_r), fall time (T_f), and delay time (T_{pd}) of logic gates, multi-stage MRL 1-bit full adders, and multi-input MRL 1-bit full adder circuit. Table 5 compares T_r, T_f, and T_{pd} of the multi-stage MRL and proposed multi-input MRL 8-bit full adder circuits. The delay time was predominantly governed by CMOS transistors. Specifically, the delay time increased with increase in the number of CMOS transistors. As a result, memristors were deployed in the proposed multi-input MRL full adder to

improve delay time. Besides, the proposed full adder required fewer computational steps since it contained only two stages.

The delay time of the multi-input and multi-stage MRL 1-bit full adder circuits were 18.95 and 69.31 ps, indicating an improvement of 72.65 % (Table 4). Meanwhile, the delay time of the corresponding 8-bit full adders were 319.50 and 633.29 ps, equivalent to a 49.52 % improvement in delay time (Table 5). Figure 11 shows the simulated delay time (T_{pd}) of multi-input MRL 8-bit full adder circuit as a function of incremental adder blocks (S[0] – S[7]).

In essence, the proposed multi-input MRL 8-bit full adder circuit holds great potential as alternative to the multi-stage full adders due to its straightforwardness, compact size, and substantially shorter delay time. Nonetheless, the proposed multi-input full adder requires higher energy consumption given the greater number of voltage inputs.

Table 4. Comparison of processing time between logic gates, multi-stage MRL 1-bit full adders, and multi-input MRL 1-bit full adder circuit

	T_r (ps)	T_f (ps)	T_{pd} (ps)
NOT gate	11.05	13.76	10.33
AND gate	22.81	22.36	0.02
OR gate	37.67	24.01	0.03
NAND gate	22.31	17.36	19.79
NOR gate	9.92	20.98	19.42
Multi-stage MeMOS logic-based full adder [16]	27.51	35.50	69.31
Multi-stage NAND gate-based full adder [23]	69.41	13.37	68.21
Conventional multi-stage MRL full adder with buffer	114.12	31.34	60.15
Proposed multi-input MRL 1-bit full adder circuit	47.61	32.45	18.95

Table 5. Comparison of processing time between logic gates, multi-stage MRL 8-bit full adders, and multi-input MRL 8-bit full adder circuit

	T_r (ps)	T_f (ps)	T_{pd} (ps)
Multi-stage MeMOS logic-based full adder [16]	78.24	24.56	633.29
Multi-stage NAND gate-based full adder [23]	69.41	13.37	562.52
Conventional multi-stage MRL full adder with buffer	84.12	31.34	532.854
Proposed multi-input MRL 1-bit full adder circuit	72.509	28.911	319.499

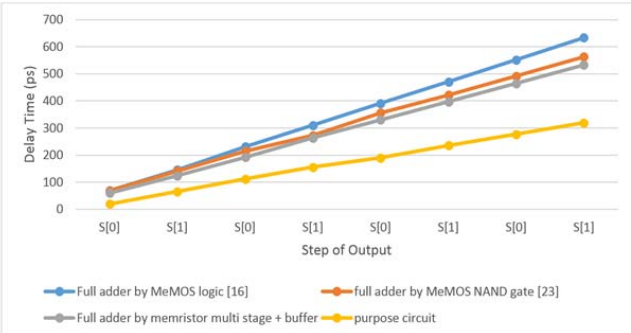

Fig .11 Simulated delay time of multi-input MRL 8-bit full adder circuit as a function of incremental adder blocks

Conclusion

As an alternative to conventional multi-stage MRL 1-bit full adders, this research proposed a multi-input MRL 1-bit full adder circuit. The proposed multi-input 1-bit adder consisted of 25 memristors without CMOS transistor. The multi-input MRL 8-bit full adder circuit was further realized by cascading eight blocks of 1-bit full adder (blocks 1-8) using ripple carry adder. However, since a direct connection between multi-input full adder blocks resulted in voltage degradation, four CMOS transistors were required in each full adder block (blocks 1-7) except for the final block (block 8). The advantages of the multi-input MRL 8-bit full adder include straightforwardness, compactness, and improved delay time. In the study, simulations were carried out by using LTspice simulation software, and simulation results were compared with multi-stage MRL 1- and 8-bit full adders. The delay time of the multi-input and multi-stage MRL 1-bit full adder circuits were 18.95 and 69.31 ps, indicating an improvement of 72.65%. Meanwhile, the delay time of the corresponding 8-bit full adders were 319.50 and 633.29 ps, equivalent to a 49.52% improvement in delay time. The smaller delay time improvement of the 8-bit full adder was attributable to the existence of CMOS transistors in the 1-bit full adder blocks. Essentially, the multi-input MRL 8-bit full adder circuit could be adopted as an alternative to existing multi-stage full adders. Nonetheless, due to greater number of voltage inputs, the multi-input full adder requires higher energy consumption. Subsequent research would thus explore techniques to improve power consumption efficiency of the multi-input full adder circuit.

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