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Design and Analysis of Passive LC^3 Component Boost-SEPIC Converter

Abstract. *A cascaded DC-DC LC^3 Boost-SEPIC converter is proposed and analyzed in this paper. In addition, the AC-DC topology and closed-loop topology of the converter are explored. The proposed DC-DC converter is capable of delivering maximum efficiency of 98.06%. For the AC-DC topology of the proposed converter, the peak efficiency of the converter is 97.77%. With the use of a controller, the performance of the AC-DC topology improved. Input THD reduced to 11.05%, and the input power factor of the converter increased to 0.983. Load analyses of both DC-DC and AC-DC topologies of the proposed converter are also carried out. Simulations of the converter are conducted using PSIM 12.0 software to facilitate the results.*

Streszczenie. *W artykule zaproponowano i przeanalizowano kaskadowy konwerter DC-DC LC3 Boost-SEPIC. Ponadto badana jest topologia AC-DC i topologia pętli zamkniętej konwertera. Proponowany konwerter DC-DC jest w stanie zapewnić maksymalną sprawność 98,06%. Dla topologii AC-DC proponowanego konwertera, szczytowa sprawność konwertera wynosi 97,77%. Dzięki zastosowaniu kontrolera poprawiono wydajność topologii AC-DC. THD wejściowe zmniejszono do 11,05%, a współczynnik mocy wejściowej konwertera wzrósł do 0,983. Przeprowadzane są również analizy obciążenia zarówno topologii DC-DC, jak i AC-DC proponowanego przekształtnika. Symulacje konwertera są przeprowadzane przy użyciu oprogramowania PSIM 12.0, aby ułatwić uzyskanie wyników.* (***Projektowanie i analiza pasywnego konwertera LC3 Component Boost-SEPIC***)

Keywords: DC-DC, AC-DC, THD, Power factor, Boost-SEPIC
Słowa kluczowe:przekształtnik typu boost, perzekształtnik DC/DC.

Introduction

As a consequence of the rapid evolution of the electronic industry, electronic converters play a crucial role for DC microgrids as they link and manage power flow from renewable sources like solar PV, wind, and fuel cells with the DC grid. The power converters focus on the conversion and regulation of electric power while preserving the closed-loop system's steady-state stability by integrating the concepts of electronics, electric power and control systems [1]. High gain converters are the pre-requisite for boosting up the output voltage. Numerous methods, including voltage lift, switching capacitors, coupled inductors, and so on, are deployed to improve the converter's static gain.

Researchers have established a number of high-gain DC-DC and AC-DC converter topologies. Each converter has its own disadvantages, and these disadvantages inspire researchers to develop new topologies. For instance, to increase the gain, switching capacitors, inductors and voltage multiplier topologies, insulated gate bipolar transistors (IGBT) are employed extensively [2-3]. AC-DC converter circuits using active elements e.g. diodes and thyristors have limitations such as strong electromagnetic interference (EMI), massive filters, high harmonic, low efficiency, and low power factor [4]. The authors of [5] developed a unique high gain DC-DC converter that boosts the voltage gain from 48 V to 380 V by employing an inductive reactive element in series with a switch. The limitation of parasitic effects with reduced output voltage and low efficiency of conventional DC-DC Boost or SEPIC converters can be mitigated by incorporating a voltage lift component, a single inductor and capacitor to the conventional SEPIC converter which gives a better voltage conversion ratio [6]. In reference [8], the authors presented an integrated double Boost SEPIC (IDBS) converter that functions as a high step-up converter that uses a single regulated power switch and two inductors to deliver high voltage gain without a massive switch duty-cycle. A novel high-gain Boost and SEPIC converter with a continual input current is suggested by the authors of [8-9]. A SEPIC-based topology for a high gain DC-DC converter using a single switch and switched inductors is proposed in [10]. [11] Suggested a SEPIC DC-DC converter using an active switched-inductor and a passive switched-capacitor. In addition, [12] describes a transformer-less high step-up SEPIC converter with the continuous input current. The key benefits of these converters are low-voltage stress across the switches and the reduced number of elements. The use of two switches in the setup, however, makes the control process more complicated.

To address the restrictions of a high voltage gain curve and a small range of duty ratios, two innovative SEPIC converters based on coupled inductors with a broader control range have been developed in [13-14]. The proposed converter in [16] has only one controlled device that increases voltage gain without employing a transformer or coupled inductor construction. However, like other DC-DC converter topologies that may raise the input voltage, both of these converters [14-15] have limitations in terms of operating with a high duty cycle. Voltage increase in both modified SEPIC converters is limited to 5–10% in practice due to actual duty cycle constraints of roughly 70–80%. Even though a conventional converter can achieve significant voltage gain at high duty ratios, the power switch will cause the converter performance to be adversely degraded and deteriorated.

The traditional Boost converters produce a discontinuous input current as well as massive current ripple and, both of which exacerbate EMI that results in poor power factor (PF) and significant total harmonic distortion (THD) and affect the efficiency of the system [16]. Researchers have recently adopted active power factor correction (PFC) methods to address these issues. One such research has been published by Yasemin et al. (2015) in which they presented a SEPIC converter based on a single-ended primary inductance converter topology to achieve low THD as well as high PF [17]. To reduce input current total harmonic distortion, [18] proposes a quasi-resonant bridgeless PFC converter. Controlled Boost Power (CBP) converters help to make better use of power networks by minimizing reactive and harmonic components of power flow across the system; as a result, energy losses in transmission and distribution lines are decreased, and energy quality improves. In general, the deployment of CBP converters to boost power quality, not only for PF correction

but also for EMI and THD reduction, is a concern for consumers, distributors, and generators [19–24].

Hence a LC^3 DC-DC Boost-SEPIC converter is developed in paper. The AC-DC topology of the converter generates better power factor and THD with higher efficiency. Circuit configuration of the proposed converter is shown followed by the circuit operation. Simulation results of the proposed converters are also shown.roposed circuit configuration.

The schematic diagram of the proposed converter is shown in Fig. 1. From the diagram it can be observed that the converter consists of DC input V_s. The input is connected with LC^3 topology. The topology consists of three capacitors (C_1-C_3), arranged in a delta configuration and an inductor L_1. The LC^3 topology is connected with inductor L_2. The inductor L_2 is connected with switch S_1. The inductor L_1 and switch S_1 are the common parts of conventional Boost and SEPIC converter. Diode D_1 and capacitor C_5 forms the Boost part of the proposed converter. Capacitors C_4 and C_6, inductor L_3 and diode D_2 forms the SEPIC part of the converter. The AC-DC topology of the proposed converter is developed by adding a full wave rectifier. The circuit diagram is shown in Fig. 2. Fig. 3 shows the closed loop topology of the AC-DC converter, by using a PI controller.

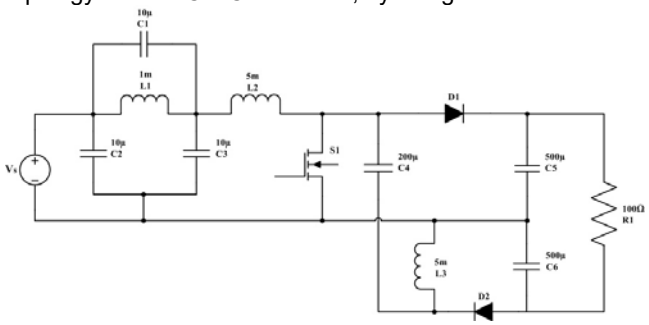

Fig.1. Proposed LC^3 DC-DC Boost-SEPIC converter

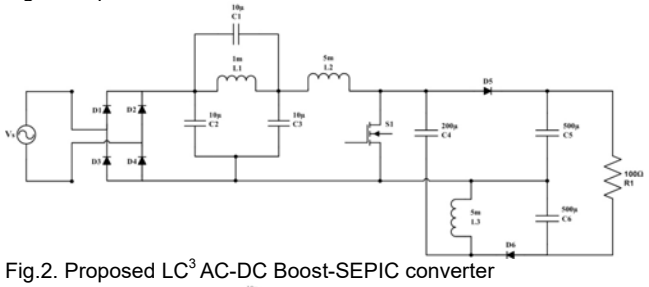

Fig.2. Proposed LC^3 AC-DC Boost-SEPIC converter

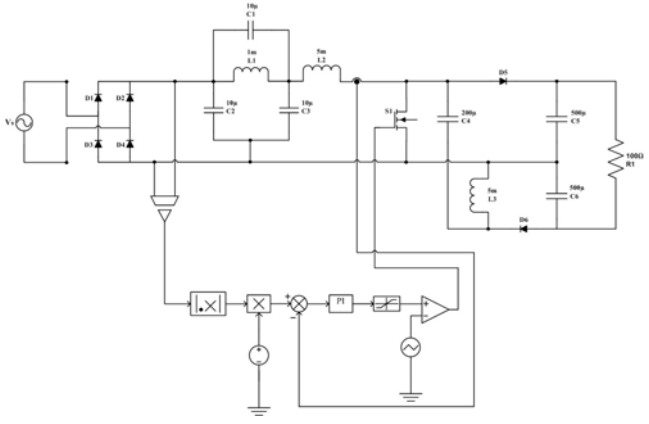

Fig.3. Proposed LC^3 AC-DC Boost-SEPIC converter

Operation of the proposed circuit

Fig. 4 shows the working principle of the proposed LC^3 Boost-SEPIC converter. The developed converter operates on two modes. In mode 1, when switch is in on state and mode 2 when the switch is in off state. When the switch is on, current flows from voltage source V_s through the inductor of the LC^3 topology. After that current flows through inductor L_2, it returns back to the source via switch S_1. Capacitors C_2 and C_3 which are charged during the off state are discharged during the on state of the switch. Capacitor C_4 which is charged during the off state discharges and charges capacitor C_6. When the switch S_1 is off, the current flows from the source V_s through inductor L_1 and L_2. Then the current splits through capacitor C_4 and diode D_1. Capacitor C_4 is charged in the process.

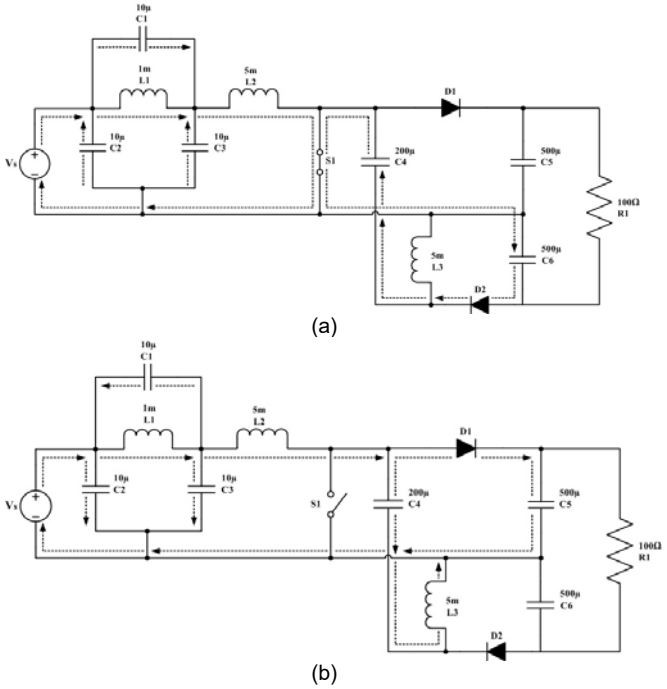

Fig.4. Operating principle of the proposed converter (a) Mode 1 when switch is on (b) Mode 2 when switch is off.

Results and analysis

Theoretical analysis of the converters are done using PSIM software. Table 1 shows the component values of the proposed converter.

Table 1. The parameters and component values of the converter

Parameters	Symbols	Values
Frequency	F	5000Hz
Input voltage	V_s	100V
Inductors	L_1	1mH
	L_3	5mH
	L_2	5mH
Capacitors	C_1	10uF
	C_2	10uF
	C_3	10uF
	C_4	200uF
	C_5	500uF
	C_6	500uF
Resistor	R_L	100Ω

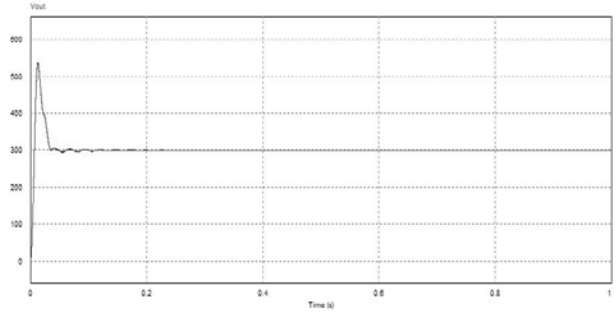

Fig.5. Output voltage at 50% duty cycle

DC-DC topology

Output voltage of the proposed converter for DC-DC topology, at 50% duty cycle is shown in Fig. 5

Efficiency comparison with conventional converters

Fig. 6 shows the efficiency comparison between proposed and conventional converters. From the graph it can be observed that the efficiency of the proposed converter is constant at around 96%. Efficiency of the conventional Boost converter also remains constant but its value is less than LC^3 Boost-SEPIC. On the other hand, efficiency of the SEPIC converter increases with increase in duty cycle but its efficiency is less than the proposed converter.

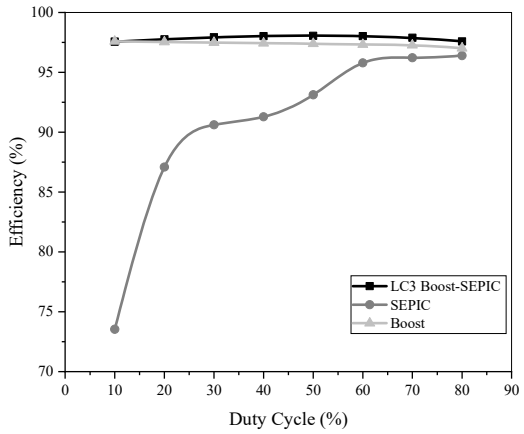

Fig.6. Efficiency comparison between proposed and conventional converters

Output voltage comparison with conventional converters

The output voltage comparison between the proposed and conventional converters are shown in the Fig. 7. The graph illustrates that the output voltage of the proposed converter is almost twice more than conventional converters. The output voltage of LC^3 Boost-SEPIC converter increases with increase in duty cycle and peaks at around 600V.

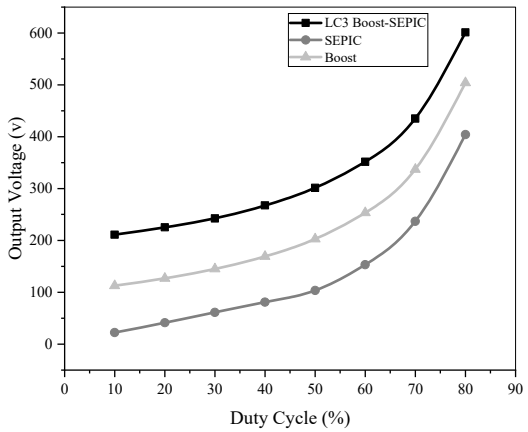

Fig.7. Output voltage comparison between proposed and conventional converters

Efficiency comparison with Boost-SEPIC converter

Fig. 8 illustrates the efficiency comparison between proposed LC3 Boost-SEPIC and Boost-SEPIC converter. From the graph it can be observed that the efficiency of both the converters are similar. Efficiency of both converters peaks at around 50% duty cycle.

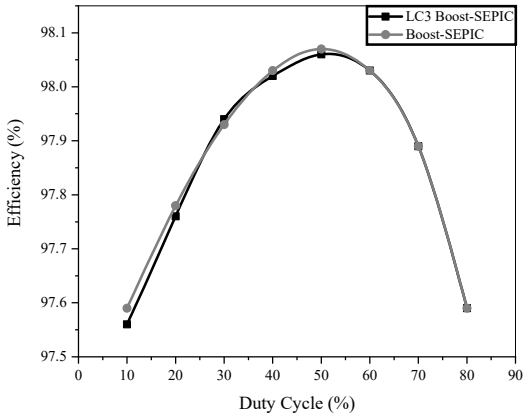

Fig.8. Efficiency comparison between proposed and Boost-SEPIC converter

Output voltage comparison with Boost-SEPIC converter

Fig. 9 shows the output voltage comparison between LC^3 Boost-SEPIC and Boost-SEPIC converter. The graphs depicts that the output voltage of both the converters are very similar and experience an increasing trend. With increase in duty cycle, the output voltage of the converters also increases.

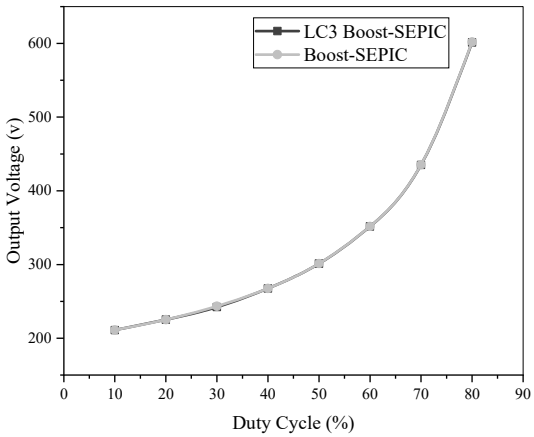

Fig.9. Output voltage comparison between proposed and Boost-SEPIC converter

AC-DC topology

Fig. 10 shows the output voltage of the proposed AC-DC topology at 50% duty cycle.

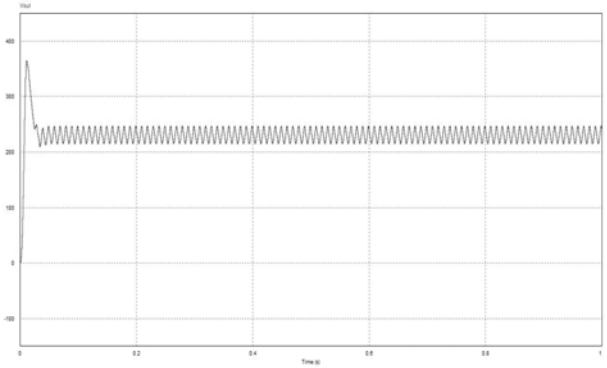

Fig.10. Output voltage at 50% duty cycle.

Efficiency comparison with conventional converter

From below illustrates the efficiency comparison between proposed and conventional AC-DC topology of the converters. It can be observed from the graph that efficiency of the conventional AC-DC SEPIC converter rises

with increase in duty cycle. Efficiency of the proposed AC-DC LC^3 Boost-SEPIC and AC-DC Boost are very similar and remains almost constant with increase in duty cycle.

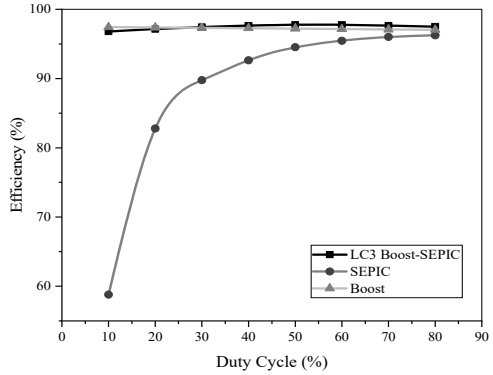

Fig.11. Efficiency comparison between proposed and conventional converters

Power factor comparison with conventional converter

Power factor comparison of the AC-DC topology between conventional Boost and SEPIC and proposed LC^3 Boost-SEPIC converter is sho9wn in Fig. 12. The graph illustrates that the power factor of the proposed converter is higher than conventional AC-DC boost converter. In case of conventional AC-DC SEPIC converter, the power factor increases and is higher than the proposed converter but only for 70% duty cycle.

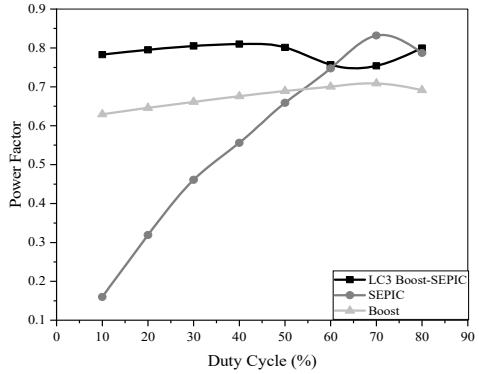

Fig.12. Power Factor comparison between proposed and conventional converters

Input THD comparison with conventional converters

Fig. 13 illustrates the THD comparison. From the graph it can be observed that input THD of the proposed converter is significantly lower than when compared with the conventional arrangements. THD of the proposed converter decreases with increase in duty cycle. Only after 60% duty cycle, THD of the proposed converter increases.

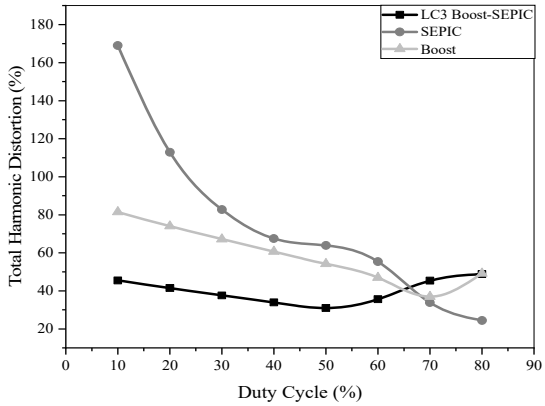

Fig.13. THD comparison between proposed and conventional converters

Output voltage comparison with conventional converters

Fig. 14 illustrates the output voltage of the converters. The graph shows that the output voltage of the converters increases when duty cycle is increases. It can be observed from the graph that the output voltage of the proposed converter is almost 1.5 times more than conventional Boost converter.

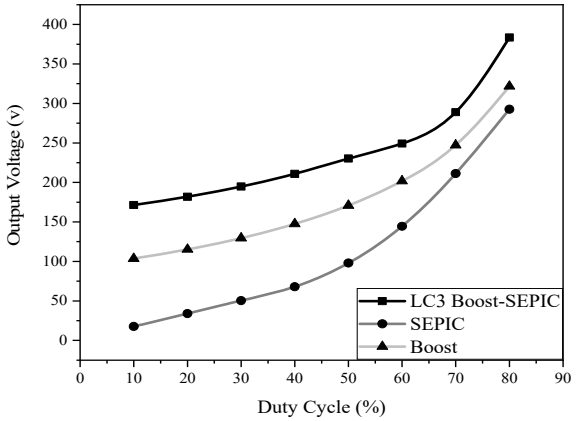

Fig.14. Output voltage comparison between proposed and conventional converters

Efficiency comparison with Boost-SEPIC converter

The efficiency comparison graph is illustrated in Fig. 15. From the graph it can be observed that initially, efficiency of both the LC^3 Boost-SEPIC converter and Boost-SEPIC converter is similar. After 20% duty cycle, efficiency of the proposed converter is higher than Boost-SEPIC converter.

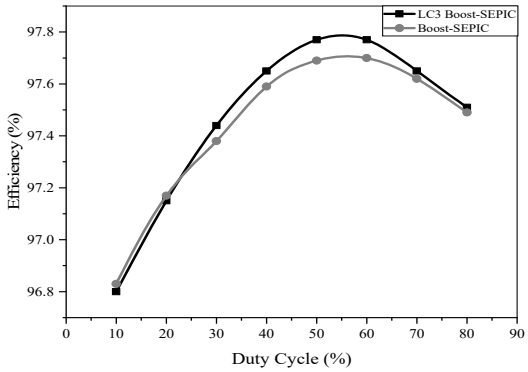

Fig.15. Efficiency comparison between proposed and Boost-SEPIC converters

Power Factor comparison with Boost-SEPIC converter

Fig. 16 shows the power factor comparison between proposed and Boost-SEPIC converter. The graph illustrates that the power factor of the proposed converter is higher than Boost-SEPIC converter. The peak power factor of the proposed converter is around 0.81.

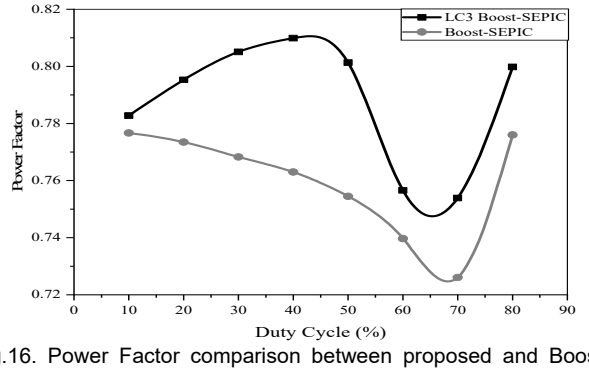

Fig.16. Power Factor comparison between proposed and Boost-SEPIC converter

THD comparison with Boost-SEPIC converter

Fig. 17 shows the THD comparison between the converters. It can be observed from the graph that THD of the proposed converter is lower than Boost-SEPIC converter. It can also be illustrated from the graph that for up to 50% duty cycle THD of both the converters decreases. After that THD of the converters increases. Without controller the lowest THD of the proposed converter is around 31%.

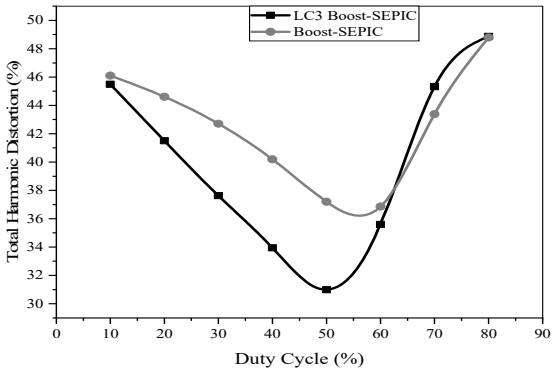

Fig.17. THD comparison between proposed and Boost-SEPIC converter

Output voltage comparison with Boost-SEPIC converter

The figure below shows the output voltage comparison between LC^3 Boost-SEPIC and Boost-SEPIC converter. From the graph, it can be concluded that the output voltage of both the converters is similar. With increase in duty cycle, output voltage of the converters also increases.

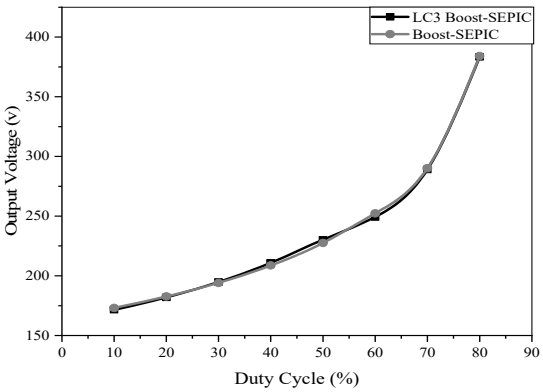

Fig.18. Output voltage comparison between proposed and Boost-SEPIC converter

Closed loop topology

Comparison between closed loop and open loop topology of the AC-DC arrangement is shown in the table below. From the table, it can be observed that the power factor and THD of the converter are significantly improved. Power factor is improved from 0.8099 to 0.983. THD is also improved from 30.99% to 11.05%. Efficiency for both the topology is very similar. Best value of the open loop is taken for comparison.

Table 1. Comparison between open loop and closed loop

	Efficiency %	Power Factor	THD %
Closed Loop	97.71	0.983	11.05
Open Loop	97.77	0.8099	30.99

Load analysis of proposed DC-DC topology

The graph below shows the load analysis of the DC-DC topology of the proposed converter. The analysis is done by keeping duty cycle constant at 50% and increasing the output load with an increment of 100 ohm. From the figure, it can be concluded that the efficiency of the converter decreases with increase in load. Maximum efficiency is obtained at 100 ohm.

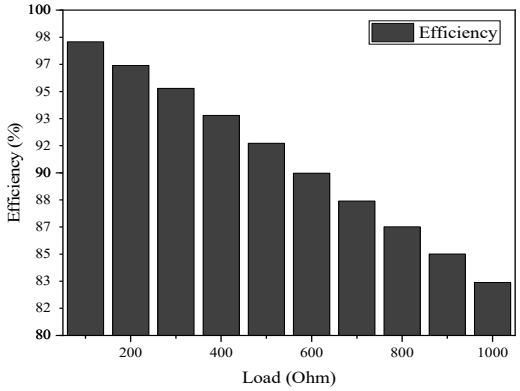

Fig. 19. Load analysis of proposed DC-DC topology

Load Analysis Of Proposed AC-DC Toppology

Fig. 20 shows the load analysis of the AC-DC topology of the proposed converter. The analysis is done with an increment of 100 ohm in load, with constant duty cycle at 50%. Similar to the AC-DC topology, it can be observed that with increase in load, efficiency of the converter decreases. The lowest efficiency of the converter is at 1000 ohm.

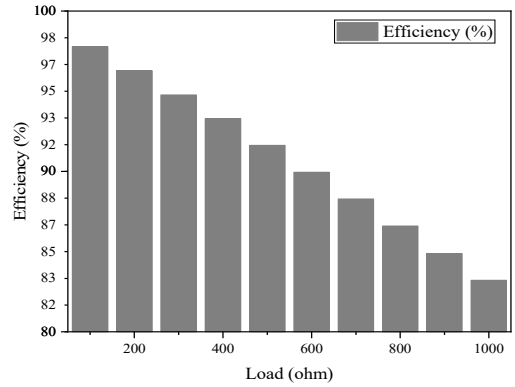

Fig. 20. Load analysis of proposed AC-DC topology

Conclusion

A cascaded LC^3 Boost-SEPIC converter has been analyzed in this paper with optimized performances. Compared to traditional converters, the described circuit achieves superior efficiency for DC-DC and AC-DC topologies. The converter's AC-DC topology and closed-loop architecture are also investigated. The proposed DC-DC and AC-DC topologies exhibit maximum efficiency of 98.6 % and 97.77 %, respectively, which are higher when compared with the standard Boost and SEPIC converter. The efficiency of both the topologies is similar compared with the Boost-SEPIC converter. In the case of AC-DC topology, the power factor and input THD suffered. The inclusion of a PI controller improved the scenario. Hence, improved power factor and input current THD yield corresponding values of 0.983 and 11.05 %.

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