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The Window Comparator Circuit with CMOS and TTL Logic ICs Switching levels

Abstract. *The digital window comparator circuits with digital switching levels use different threshold voltages. The proposed circuit consists of a Schmitt-trigger inverter gate and the AND gate. Both gates have different switch levels, and the circuit has a window boundary between both threshold voltages. The input voltages range between the threshold levels, and the output logic is "High". The input voltage is higher or lower than the range, and the output logic is "Low". This paper presents the coupling of different types of logic ICs for the development of digital window comparator circuits, the simulation results, and the experimental circuit results that create a window boundary between* $V_{IL(D)} < V_{in} < V_{IH(R)}$.

Streszczenie. *Obwody cyfrowego komparatora okienkowego z cyfrowymi poziomami przełączania wykorzystują różnicowe napięcia progowe. Proponowany układ składa się z bramki falownika z wyzwalaczem Schmitta i bramki AND. Obie bramki mają różne poziomy przełączania, a obwód ma granicę okna między obydwoma napięciami progowymi. Napięcia wejściowe mieszczą się w zakresie między poziomami progowymi, logika wyjściowa jest „wysoka". Napięcie wejściowe jest wyższe lub niższe niż zakres, logika wyjściowa jest „niska". W artykule przedstawiono sprzężenie różnych typów logicznych układów scalonych w celu opracowania obwodów cyfrowego komparatora okienkowego, wyniki symulacji oraz wyniki obwodów eksperymentalnych, które tworzą granicę okna między* $V_{IL(D)} < V_{in} < V_{IH(R)}$. (***Obwód komparatora okiennego z poziomami przełączania układów logicznych CMOS i TTL***)

Keywords: window comparator, digital switching levels, voltage detector, window boundary
Słowa kluczowe: komparator okienkowy, cyfrowe poziomy przełączania, detektor napięcia, granica okienkowa

Introduction

A window comparator circuit considers multi-level inputs or analogue signals to output as two-levels logic signals, using logic devices with a different threshold voltage. The input value between the threshold level and the output logic is "High." When the input voltage is higher than or less than the threshold level, that output logic is "Low." There are two types of Windows comparators, the analogue windows comparators which are used to detect signals in industrial applicationsand[1-5], and the digital windows comparators [6-10] which use various ICs such as op-amp, comparator, digital logic, that depend on the difference in the voltage difference within the semiconductor device and compared to create a window boundary. It detects signals in circuits that require safety [11-15].

The paper [8] design concept is based on AND logic with properties of digital ICs in fact operation. When the Schmitt trigger inverter is CMOS ICs and AND gate is TTL ICs, there are different switching levels, and the circuit has a window boundary between both threshold voltages. The circuit consists of the CMOS Schmitt-trigger inverter and the TTL AND gate, as shown in Figure 1.

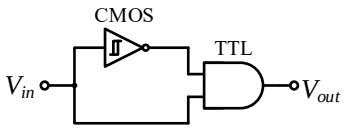

Fig.1. A window comparator circuit with digital switching levels [8].

The circuit is proposed as a window comparator by properties of digital ICs, and a ICs is the switch to a logic "High" or "Low." That the input logic is "Low" or "High" to make the output only logic "Low." The logic "High" is not in such conditions because the input logic "High" through the inverter becomes logic "Low" the AND gate logic ICs receive the signal to both legs are "Low" and "High," respectively, and the output is logic "Low". Moreover, the input logic "Low" through the inverter becomes logic "High"; both legs of AND gate logic ICs receive the signal that is "High" and "Low," respectively, and the output still has the logic "Low."

From the explanation above, either the input logic signal 'High' or 'Low' cannot cause the output signal due to the arrangement of the circuit, as shown in Figure 1, which prevents the AND gate logic ICs from having a "High" signal at the same time at the input.

The operation of this window comparator to output a signal that is logic "High" must be a signal that is in the range between the V_{IL} of the CMOS inverter ICs and the V_{IH} of the TTL AND Gate ICs, which causes the signal gap to appear as in Figure 2

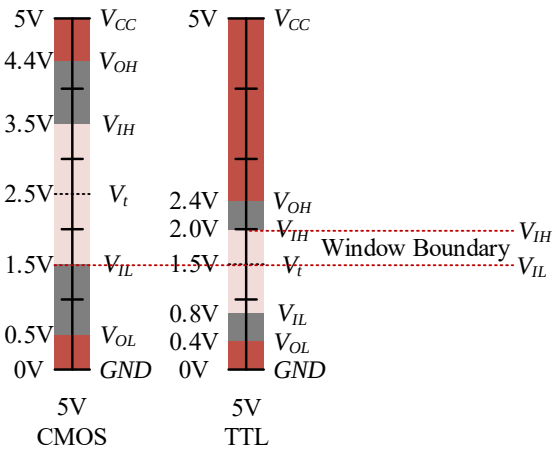

Fig.2. Comparison of switching levels for window boundary [16].

Figure 2 shows the window boundary obtained by comparing the voltage between the CMOS logic ICs and the TTL logic ICs. The channel at 1.5V to 2.0V, the window boundary, can be written as Equation (1).

$$V_{T\_TTL} < V_{in} < V_{T\_CMOS} \quad (1)$$

The circuit has a window boundary between both threshold voltages, as shown in Figure 3.

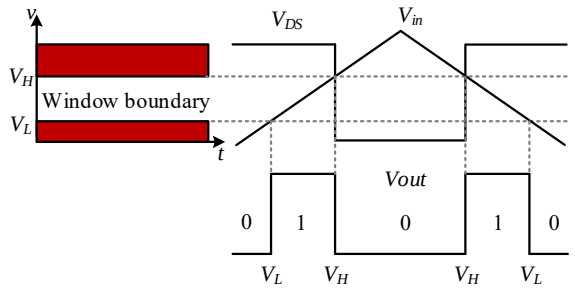

Fig.3. Window boundary and voltage waveforms.

This papers present a window comparator circuit by comparing the voltage gap of each type of logic ICs by assigning the ICs input to be a 5V CMOS and the ICs output being different. Test the circuit with computer simulation programs and experimental circuits.

Fundamental Method

There are only two types of signals, that "High" and "Low," in logic gate circuits, as shown by the variable voltage, which is designed to provide input and output of the voltage from sources for the "High" state and zero voltage or ground for the "Low" state in ideal logic ICs. In the actual logic ICs, the logic signal voltage levels rarely reach these perfect limits. Due to the voltage drop across the transistor circuit, the gate circuit's signal level limitations must be understood.

The 5V TTL gate ICs operate at 5 volts, the "High" signal at 5.0 volts, and the "Low" signal at the ground or 0 volts. The acceptable input signal voltages range is 0 to 0.8 volts for the "Low" logic state and 2 to 5 volts for the logic state "high". The acceptable output signal voltages range from 0 to 0.5 for the logic state "Low" and 2.7 to 5 for the logic state "High". The acceptable 5V TTL gates signal is shown in Figure 4.

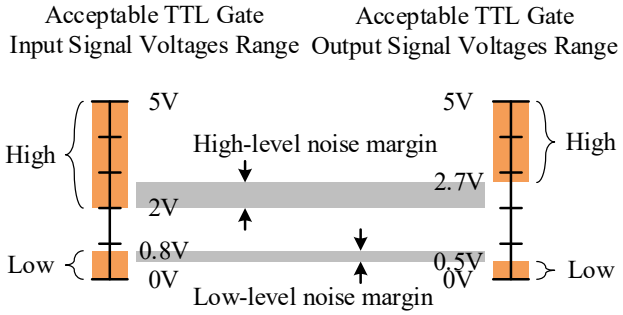

Fig.4. The acceptable signal of TTL gate ICs operates [17].

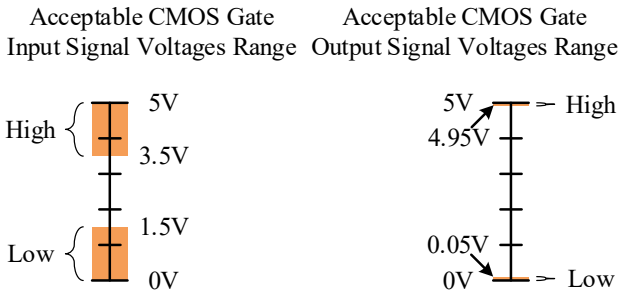

Fig.5. The acceptable signal of CMOS gate ICs operates [17].

The 5V CMOS gate ICs operate, and the acceptable input signal voltages range is 0 to 1.5 volts for the logic state "Low" and 3.5 to 5 volts for the logic state "High". The acceptable output signal voltages range is 0 to 0.05 volts for the logic state "Low" and 4.95 volts to 5 volts for the logic state "High". The acceptable 5V CMOS gates signal is shown in Figure 5.

Each type of digital ICs has different input and output acceptance levels, as shown in Figure 6.

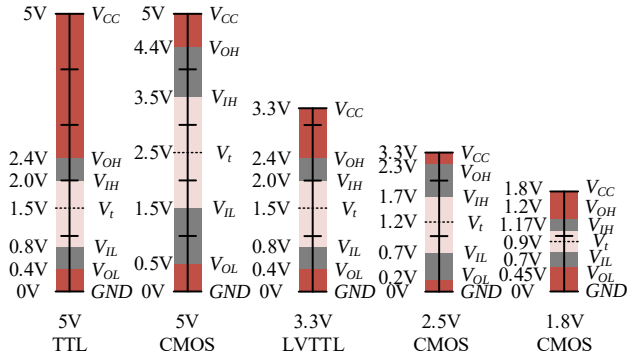

Fig.6. The digital ICs logic switching levels [16].

There have some points of borderline dividing the gate's "Low" input signal range from the "High" input signal range for the "uncertain" range of any gate input. The point between the lowest signal voltage level is "High", and the highest is "Low". The borderline voltage thresholds are shown in Figure 7.

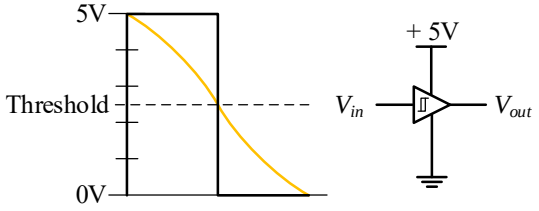

Fig.7. The borderline voltage thresholds [17].

The coupling between each type of digital ICs must look at the details of the switching properties of each type of ICs. The minimum operating switching levels are the switching input/output, which illustrates V_{IH} and V_{IL}. V_t is the approximate switching level, and the V_{OH} and V_{OL} levels are the outputs for the V_{CC} specified. The coupling between digital logic ICs, as shown in Figure 8, and the switching input/output comparison table, as shown in Table 1.

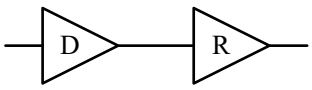

Fig.8. The coupling between digital logic ICs [16].

Table 1. Switching input/output comparison [16].

D \ R	5 TTL	5 CMOS	3 LVTTL	2.5 CMOS	1.8 CMOS
5 TTL	Yes	No	Yes*	Yes*	Yes*
5 CMOS	Yes	Yes	Yes*	Yes*	Yes*
3 LVTTL	Yes	No	Yes	Yes*	Yes*
2.5 CMOS	Yes	No	Yes	Yes	Yes*
1.8 CMOS	No	No	No	No	Yes*

*Requires V_{IH} Tolerance

Design Propose

From the fundamental method mentioned above, the windows comparator circuits [8] are defective due to the limitation of the properties of the TTL ICs, the difference between the input voltage and the logic output voltage, resulting in both noise margins at High-Level and Low-Level aspects make the windows comparator circuits that operates during this gap unstable. The CMOS logic ICs are more stable on the output side, with logic "High" about 5 volts and logic "Low" and the input High-Low voltage range switching at the centre. Of the voltage of the power supply, both are 5 V, 2.5 V and 1.8 V**.**

The coupling of different types of logic ICs is shown in Figure 8 and Table 1. Row 2 of Table 1 shows the 5 V CMOS ICs as (D) input ICs that can be coupled to all (R) output ICs. Therefore, the development of a digital window comparator circuit by switching the voltage of IC logic [8] by setting the input to IC 5 V CMOS can create a window comparator circuit with three levels of signal detection range, as shown in the Figure. 9, 10 and 11.

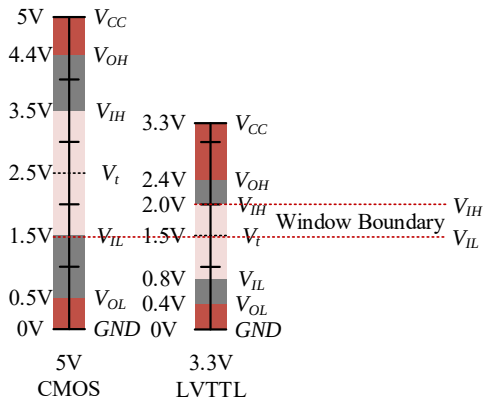

Fig.9. Comparison of switching levels between 5 V CMOS and 3 V LVTTL for window boundary.

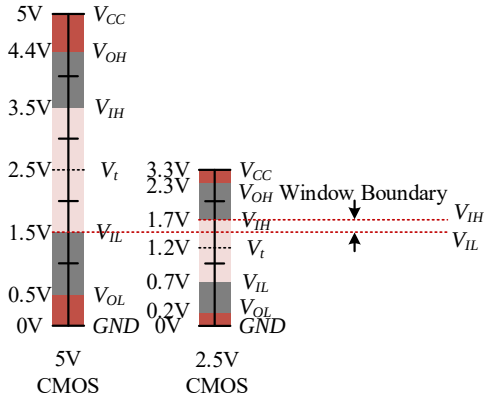

Fig.10. Comparison of switching levels between 5 V CMOS and 2.5 V CMOS for window boundary.

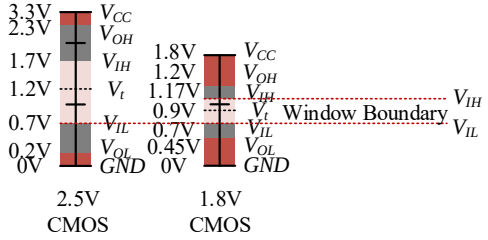

Fig.11. Comparison of switching levels between 2.5 V CMOS and 1.8 V CMOS for window boundary.

From Figure 9-11, three levels of window comparator ranges are obtained. Figure 9 compares 5 V CMOS and 3 V LVTTL, resulting in a signal range of 1.5 - 2.0 Volts. Figure 10 is a comparison of 5. V CMOS and 2.5 V CMOS result in a signal range of 1.5 - 1.7 volts. Figure 11 compares 2.5 V CMOS and 1.8 V CMOS, resulting in a signal range of 0.7 - 1.17 volts. Which can be written as Equation (2)

$$V_{IL(D)} < V_{in} < V_{IH(R)} \quad (2)$$

Results

Test the operation of the designed circuit by simulating the operation with the computer program and according to the circuit in Figure 1, changing the IC type as designed. The simulation uses a computer program and a behavioural device to simulate the proposed circuit. The input triangle waveform signal simulates at 7 Volts with a frequency of 100 kHz, as shown in Figure.12, 13 and 14.

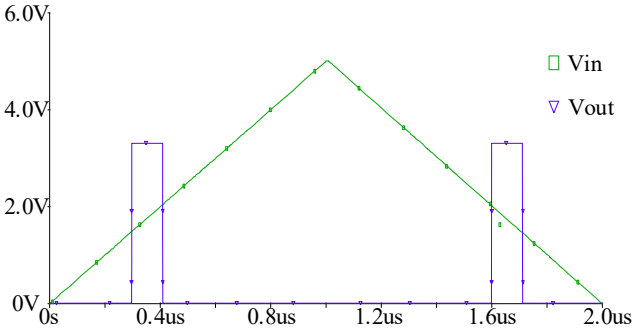

Fig.12. Simulation results between 5 V CMOS and 3 V LVTTL for window boundary.

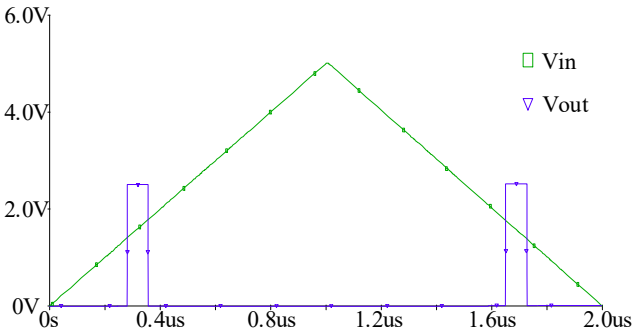

Fig.13. Simulation results between 5 V CMOS and 2.5 V CMOS for window boundary.

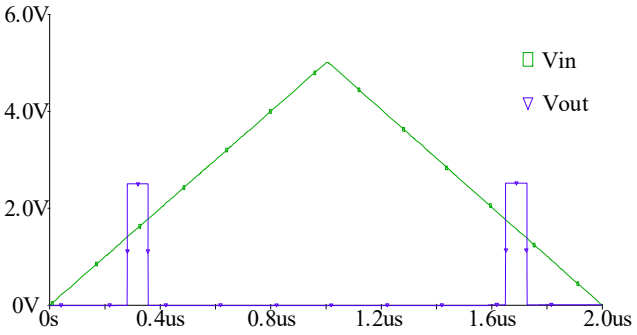

Fig.14. Simulation results between 2.5 V CMOS and 1.8 V CMOS for window boundary.

The laboratory implements the proposed circuit, working efficiently for a 100 kHz triangular signal frequency at 6 Volts.

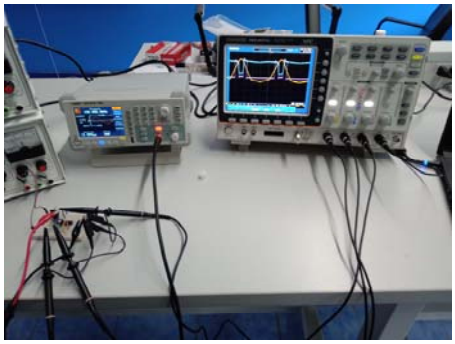

Fig.15. Experimental circuit.

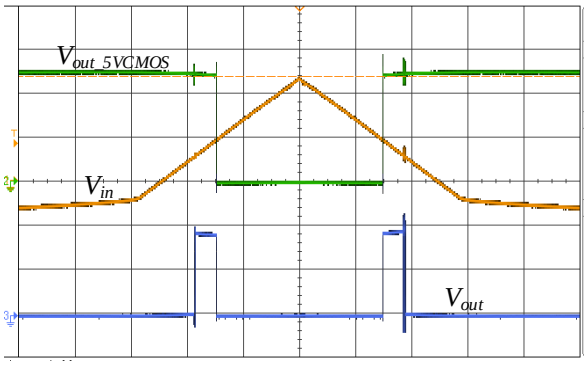

Fig.16. Experimental circuit.

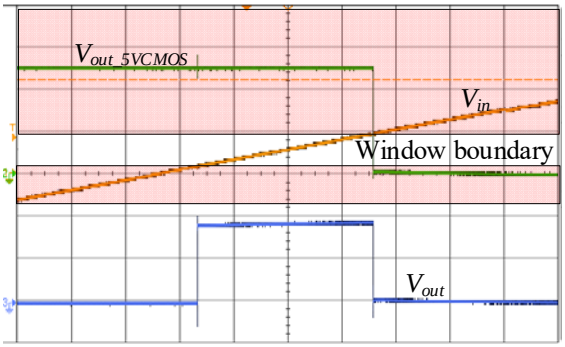

Fig.17. Results of Experimental circuit with lower window boundary

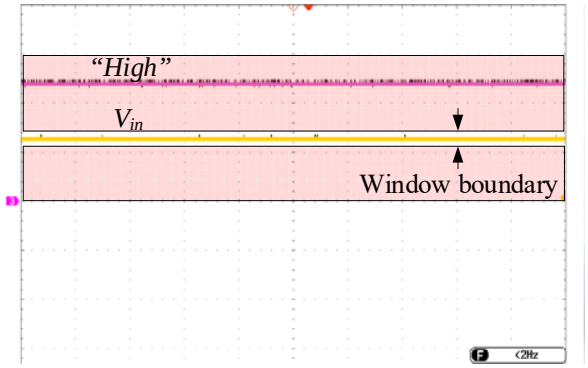

Fig.18. Experimental circuit results with input are in the window boundary.

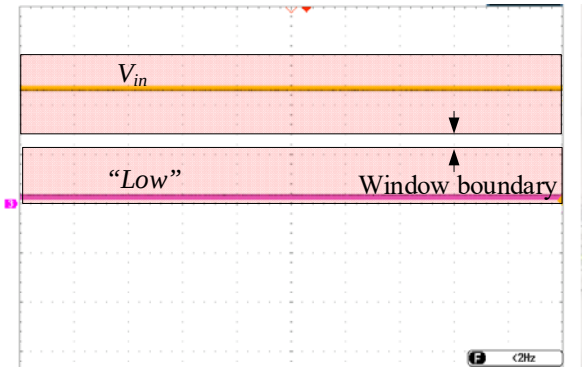

Fig.19. Experimental circuit results with input are out of window boundary.

The experimental circuit results, the window comparator circuit designed to create the window boundary is between $V_{IL(D)} < V_{in} < V_{IH(R)}$. Figures 16-17 result between 5 V CMOS and 3 V LVTTL. Testing of the circuit operation by DC signal from Figures 18-19 shows the operation of the circuits. The signal output is logic "High", which is in the window boundary range, and logic "Low", that the signal is out of the window boundary range.

Conclusion

By switching levels the digital comparator circuits can be done by switching levels of the signals of each type of digital IC. Coupling the CMOS side to the various ICs on the output side can be done according to the requirements. This article shows 5 V CMOS and 3 V LVTTL, resulting in a signal range of 1.5 - 2.0 Volts. 5 V CMOS and 2.5 V CMOS result in a signal range of 1.5 - 1.7 volts, and 2.5 V CMOS and 1.8 V CMOS result in a signal range of 0.7 - 1.17 volts. The simulation results from the computer program and experimental circuits resulted in the designed performance. The output logic signal from the ascending and descending triangle input signal is symmetrical.

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