1. Taha Ahmad Hussein[1] , 2. DahamanIshak[2] , 3. Mohamad Tarnini[3]

Northern Technical University, Mosul, (1) Iraq
Universiti Sains Malaysia, Penang, (2) Malaysia
Beirut Arab university , USM offshore center(3), Türkiye
ORCID: 1. 0000-0001-9516-6860 2. 0000-0001-9363-6339 3. 0000-0001-7726-4598

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Reduced Components Count with Optimal Switching for Minimum THD in Multilevel Inverter

Abstract--- *This paper presents the design and implementation of a 31 multi-level inverter (31-MLI) suitable for medium and high-power industrial applications. The research considers the reduction of the components in the switches and the DC sources used, as well as the reduction of the total harmonics distortion (THD) at the output voltage by selective harmonics elimination (SHE). For this purpose, three efficient algorithms are used to determine the optimum values of switching angles. Those algorithms are genetic algorithm_(GA), gray wolf optimization _(GWO) and slime mold algorithm_ (SMA). The switching angles that give the lowest value of THD were selected from each algorithm and tabulated for a wide range of modulation index (m), and named the integrated hybrid optimizer (IHO). A reduced switches model of 31-MLI is built, controlled by Arduino, and programmed with the selected optimized angles. A comparison study is carried out for all optimized cases. To validate the effectiveness of the proposed IHO, a 31-MLI is modeled in MATLAB Simulink environment. An experimental prototype was also built and tested. Comprehensive results from both simulation and experiment are analyzed and compared under different operating conditions. The results show the proposed IHO can achieve minimum THD in a 31-MLI.*

Streszczenie. *W artykule przedstawiono projekt i realizację wielopoziomowego falownika 31 (31-MLI) odpowiedniego do zastosowań przemysłowych średniej i dużej mocy. Badania uwzględniają redukcję komponentów stosowanych w przełącznikach i źródłach prądu stałego, a także redukcję całkowitego zniekształcenia harmonicznych (THD) napięcia wyjściowego poprzez selektywną eliminację harmonicznych (SHE). W tym celu stosuje się trzy wydajne algorytmy wyznaczające optymalne wartości kątów przełączania. Algorytmy te to algorytm genetyczny_(GA), optymalizacja szarego wilka_(GWO) i algorytm śluzowca_ (SMA). Z każdego algorytmu wybrano kąty przełączania, które dają najniższą wartość THD, zestawiono w tabeli dla szerokiego zakresu współczynnika modulacji (m) i nazwano zintegrowanym optymalizatorem hybrydowym (IHO). Zbudowany jest zredukowany model przełączników 31-MLI, kontrolowany przez Arduino i programowany pod wybranymi zoptymalizowanymi kątami. Dla wszystkich zoptymalizowanych przypadków przeprowadzane jest badanie porównawcze. Aby zweryfikować skuteczność proponowanej IHO, model 31-MLI jest modelowany w środowisku MATLAB Simulink. Zbudowano i przetestowano także eksperymentalny prototyp. Kompleksowe wyniki symulacji i eksperymentów są analizowane i porównywane w różnych warunkach operacyjnych. Wyniki pokazują, że proponowana IHO może osiągnąć minimalne THD w 31-MLI.* (***Zmniejszona liczba komponentów przy optymalnym przełączaniu zapewniającym minimalne THD w falowniku wielopoziomowym***)

Keywords: Multilevel inverter, MLI, GA , GWO , SMA
Słowa kluczowe: Falownik wielopoziomowy, MLI, GA, GWO, SMA

1. Introduction

In industrial applications, power conversion systems widely used rely very much on multi-level inverters (MLI) because of many distinctive characteristics. MLI can provide an output voltage very close to the sine wave. MLI switches also operate at a lower frequency, which helps in obtaining a lower blocking voltage with a lower ratio of dv/dt, which in turn leads to improved electromagnetic capability. The shape of the output voltage close to the sine wave reduces the number of harmonics, which leads to a decrease in the filter size. MLI is used mostly for medium and high-power ratings, therefore, MLI has found extensive practical applications in motor drives as well as medium/high voltage drives [1-5]. MLI also finds extensive applications in customized and commercial products such as flexible ac transmission (FACTS), high voltage direct current (HVDC) transmission, battery energy storage systems (BESS), and electrical vehicles [6-9]. There are three main structures for MLI i.e., cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) [10-15]. These MLI topologies have found applications for different capability levels and each of these topologies has its benefits and drawbacks. These drawbacks include the use of a larger number of components (switches and DC sources) as the number of levels of MLI increases, in addition to the problems of balancing the voltages of different capacitors. To overcome these problems, researchers are racing to provide new topology and innovative ways to control MLI. The most important design goal of the new MLI topology is to reduce the number of switches and the number of dc sources [16-24], as well as the total standing voltage (TSV) of the topology [25-30]. In most of the recent research, high levels of MLI were obtained using staircase technique with equal on-time duration. Although the MLI output voltage is close to the sinewave shape, this does not ensure the cancellation of many harmful harmonics without using large-size filters.

2. THE Proposed 31- mli

Researchers are working hard to increase the number of MLI levels while simultaneously decreasing the number of switches and DC sources used [34-36]. The proposed 31-level MLI topology is shown in Fig. 1 [37]. There are 4 asymmetrical DC sources and 10 MOSFET switches. This topology fabricates 31-levels with maximum value equal the sum and differences of the DC sources. Number of DC sources governs the number of required switches and the number of levels according to the following equation:

(1)
$$\left.\begin{array}{c} N_{sources} = M = 4 \\ N_{levels} = 2^{M+1} - 1 = 31 \\ N_{switches} = 2(M+1) = 10 \\ V_{DC1} + V_{DC2} + V_{DC3} + V_{DC4} = V_{out(\max)} \\ V_{DC2} = 5V_{DC1}\,,\ V_{DC3} = 2V_{DC1}\,,\quad V_{DC4} = 10V_{DC1} \end{array}\right\}$$

Considering that the desired maximum output voltage $V_{out(max)}$ = 216V, then:

$$V_{DC1} = \frac{216V}{18} = 12V, V_{DC2} = 60V$$

$$V_{DC3} = 24V, V_{DC4} = 120V.$$

From Fig.1, it is obvious that each DC source surrounds two transistors. For example, V_{dc1} surrounds S_1 and S_2 which must operate in complementary mode to avoid short

circuits. The same is true for the other transistors. To get higher levels, two DC sources and four switches are to be added to the topology in Fig. 1. This MLI topology can be extended to any desired levels such as 127-level MLI:
(2)

$$\left.\begin{aligned} N_{sources} &= M = 6 \\ N_{levels} &= 2^{M+1} - 1 = 127 \\ N_{switches} &= 2(M+1) = 14 \end{aligned}\right\}$$

$$V_{DC2} = 5V_{DC1}, V_{DC3} = 2V_{DC1}, V_{DC4} = 10V_{DC1}, V_{DC5} = 25V_{DC1}, V_{DC6} = 50V_{DC1}$$

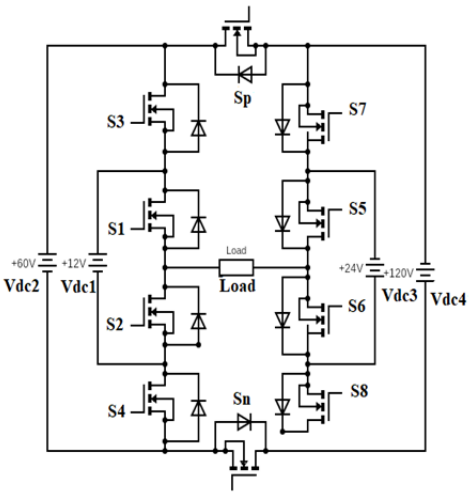

Fig. 1. Proposed 31-MLI

3. Selective harmonic elimination technique

The modulated pulses supplied to the gates of power switches are classified according to the switching frequency. There are two main types. The first is the high switching frequency which includes the castigatory of sinusoidal pulse width modulation (SPWM). In this type, a carrier of high frequency is employed besides the low fundamental frequency. The switches are turned on and off for a very small-time duration which results in high switching losses. The second type of modulated pulses is the fundamental switching frequency which results in small switching losses. In the stair voltages as in Fig. 2, if the period of the angles is divided equally, many harmonics are produced which reduce the efficiency of the system.

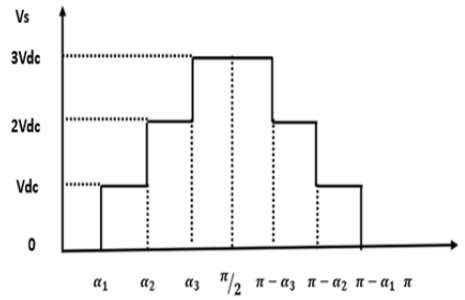

Fig. 2. Staircase waveform

To remove or even reduce the value of these harmonics, the selective harmonic elimination technique is used in this research. The MLI output voltage is first analyzed using the Fourier series, and then its harmonics are extracted. The equations of the harmonics are presented to the minimization algorithms for the purpose of getting optimized switching angles. The Fourier series for a stair periodic function can be expressed:

$$(3) \qquad v_0(t) = \frac{a_o}{2} + \sum_{k=0}^{n} a_n \cos(nwt) + b_n \sin(nwt)$$

where a_o, is the average value of the output voltage , a_n and b_n, are even and odd components of the staircase periodic signal respectively. The stair waveform possesses a quarter wave symmetry which sets a_o , a_n and the odd b_n values to zero and modifies equation (3) to:

$$(4) \qquad v_0(t) = \sum_{i=1,3,5,7,..}^{n} b_n \sin(nwt)$$

Where $\quad b_n = \frac{4V_{dc}}{n\pi} \sum_{k=1,3,5,7..}^{m} \cos(n\,\theta_k)$

The relation between number of levels and the harmonic contents to be eliminated in the stair waveform can be written as follows:

$$(5) \qquad N_{harmonics} = (N_{levels} - 1)/2..$$

In this work, the MLI topology generates 31 levels. This means there are 15 trigonometric equations to be solved. This allows 14 harmonics to be eliminated, leaving only the fundamental. The lower order harmonics from 3rd,5th,7th, …up to 29th order harmonics are selected to be eliminated. This technique is known as selective harmonic elimination pulse width modulation (SHEPWM). The nonlinear restriction that must be maintained is that the gating angles ($\theta_1 < \theta_2 < \theta_3, .. < \theta_{29} < \frac{\pi}{2}$). The required 15 trigonometric equations to be solved for the minimum values of gating angles are as follows:

$$(6) \qquad b_1 = \frac{4V_{dc}}{\pi} \{\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cdots + \cos(\theta_{15}) = V_{fund}$$

$$b_3 = \frac{4V_{dc}}{3\pi} \{\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) + \cdots + \cos(3\theta_{15}) = 0$$

$$b_5 = \frac{4V_{dc}}{5\pi} \{\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cdots + \cos(5\theta_{15}) = 0$$

$$b_{15} = \frac{4V_{dc}}{15\pi} \{\cos(15\theta_1) + \cos(15\theta_2) + \cos(15\theta_3) + \cdots + \cos(15\theta_{15}) = 0$$

where V_{fund} is the fundamental component, calculated as follows :

$$(7) \qquad V_{fund} = \frac{2V_{DC} * m * (N_{switches} - 1)}{\pi}$$

4. Optimization algorithms

There are many algorithms dedicated to obtaining the optimal solutions for a given problem. The output of the multi-level inverter with low values of THD can be achieved by presenting their non-linear equations to such algorithms. This results in optimal gating angles that eliminates many of the undesired harmonics at the inverter output voltage. When using a wide range of modulation index, each algorithm has distinct solutions for each value of modulation index. Three algorithms known for their efficiency in finding optimal solutions are chosen in this research, namely GA, GWO and SMA [31-33]. Each algorithm is examined separately to find the relationship between modulation index (m) and the THD for the proposed 31-MLI inverter output voltages. The algorithm solutions present the global minimum 15 gating angles. These optimized angles fabricates the desired 31 different

voltage levels. Table 1 shows the relationship between triggering angles and THD and for modulation index, ranging from 0.6 to 1 for the three algorithms. Comparing these THDs, it can be noted that GA gives the best results for m values between 0.6 and 0.65. While SMA gives the best results for the values of m between 0.7 and 0.75. Lastly, GWO gives the best results for the values of m between 0.8 and 1.

Table 1. Modulation index vs THD for GA, SMA, and GWO

m	THD		
	GA	SMA	GWO
0.6	7.48	9.77	9.86
0.65	7.49	8.85	10.15
0.7	7.13	6.16	8.17
0.75	5.67	5.65	6.75
0.8	7.15	5.63	5.53
0.85	7.99	6.25	4.62
0.9	7.19	6.44	3.94
0.95	7.26	8.25	3.55
1	7.05	8.54	3.69

In this research, the optimal solutions among the three algorithms are collected and an integrated relationship between m and THD is initiated. This relationship is tabulated in Table 2, and it is named as the integrated hybrid optimizer (IHO).

Fig. 3 shows the relationship between modulation index m and THD for GA , SMA , GWO and IHO.

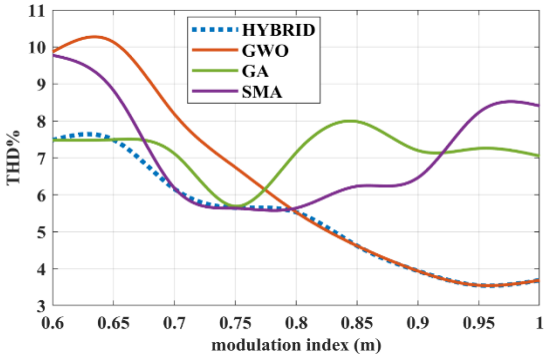

Fig. 3. THD vs modulation index m for GA , SMA , GWO and IHO

Fig. 4 , Fig. 5, Fig. 6, and Fig. 7 show the variation of the triggering angles as a function of the modulation index m for GA, GWO SMA and IHO respectively.

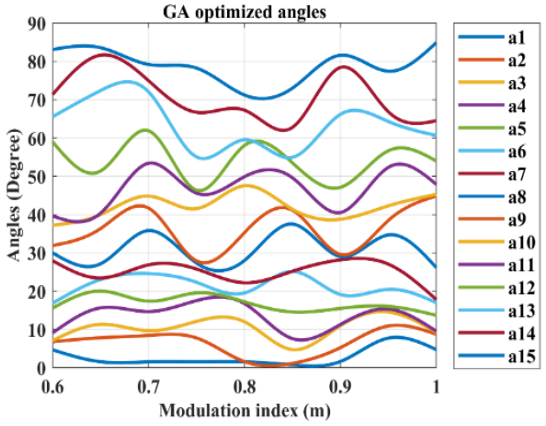

Fig. 4. Optimized angles vs m for GA

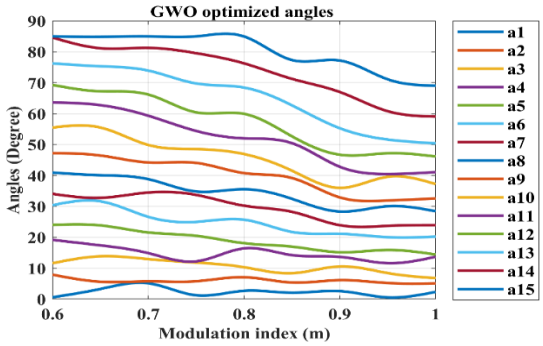

Fig. 5. Optimized angles vs m for GWO

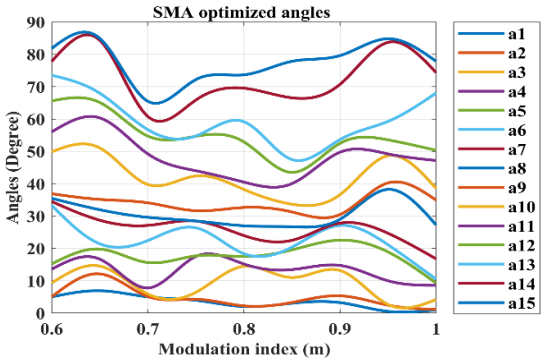

Fig. 6. Optimized angles vs m for SMA

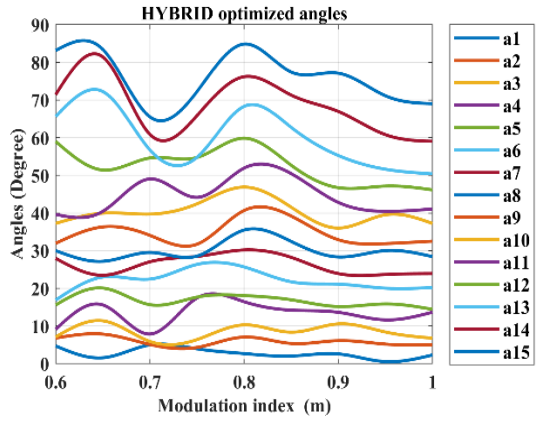

Fig7. Optimized angles vs m for IHO

Table 2. ABLE 2. IHO THDs vs m

m	THD
0.6	7.48
0.65	7.49
0.7	6.16
0.75	5.65
0.8	5.53
0.85	4.62
0.9	3.49
0.95	3.55
1	3.69

Table (3) shows the switching states for ten switches along with the duration of the on time for each switch during positive half cycle. Table 4 shows states during negative half cycle. These values are used in programming the Arduino controller to provide the gating signals for experimental work . When simulating the proposed topology, the gating signals are performed using the pulse generator box in the environment of the MATLAB Simulink model. The phase shift in the pulse generator is fed by the data in the 'shift' column in Table 3 and Table 4.

Table 2. SWIT codes states for positive ha;f cyclre

S1	S2	S3	S4	S5	S6	S7	S8	Sp	Sn	Vdc	Duration	DC sources	Shift
1	0	1	0	1	0	1	0	1	0	0	α_1	No DC source	0
0	1	1	0	1	0	1	0	1	0	1	$\alpha_2 - \alpha_1$	V_{DC1}	α_1
1	0	1	0	0	1	1	0	1	0	2	$\alpha_3 - \alpha_2$	V_{DC3}	α_2
0	1	1	0	0	1	1	0	1	0	3	$\alpha_4 - \alpha_3$	V_{DC1+} V_{DC3}	α_3
1	0	0	1	1	0	1	0	1	0	4	$\alpha_5 - \alpha_4$	V_{DC2-} V_{DC1}	α_4
0	1	0	1	1	0	1	0	1	0	5	$\alpha_6 - \alpha_5$	V_{DC2}	α_5
1	0	0	1	0	1	1	0	1	0	6	$\alpha_7 - \alpha_6$	V_{DC2+} V_{DC3-} V_{DC1}	α_6
0	1	0	1	0	1	1	0	1	0	7	$\alpha_8 - \alpha_7$	V_{DC2+} V_{DC3}	α_7
1	0	1	0	1	0	0	1	1	0	8	$\alpha_9 - \alpha_8$	V_{DC4-} V_{DC3}	α_8
0	1	1	0	1	0	0	1	1	0	9	$\alpha_{10} - \alpha_9$	V_{DC4-} V_{DC3+} V_{DC1}	α_9
1	0	1	0	0	1	0	1	1	0	10	$\alpha_{11} - \alpha_{10}$	V_{DC4}	α_{10}
0	1	1	0	0	1	0	1	1	0	11	$\alpha_{12} - \alpha_{11}$	V_{DC4+} V_{DC1}	α_{11}
1	0	0	1	1	0	0	1	1	0	12	$\alpha_{13} - \alpha_{12}$	V_{DC4+} V_{DC2-} V_{DC3-} V_{DC1}	α_{12}
0	1	0	1	1	0	0	1	1	0	13	$\alpha_{14} - \alpha_{13}$	V_{DC4+} V_{DC2-} V_{DC3}	α_{13}
1	0	0	1	0	1	0	1	1	0	14	$\alpha_{15} - \alpha_{14}$	V_{DC4+} V_{DC2-} V_{DC1}	α_{14}
0	1	0	1	0	1	0	1	1	0	15	$\pi - 2\alpha_{15}$	V_{DC4+} V_{DC2}	α_{15}
1	0	0	1	0	1	0	1	1	0	14	$\alpha_{15} - \alpha_{14}$	V_{DC4+} V_{DC2-} V_{DC1}	$\pi - \alpha_{15}$
0	1	0	1	1	0	0	1	1	0	13	$\alpha_{14} - \alpha_{13}$	V_{DC4+} V_{DC2-} V_{DC3}	$\pi - \alpha_{14}$
1	0	0	1	1	0	0	1	1	0	12	$\alpha_{13} - \alpha_{12}$	V_{DC4+} V_{DC2-} V_{DC3-} V_{DC1}	$\pi - \alpha_{13}$
0	1	1	0	0	1	0	1	1	0	11	$\alpha_{12} - \alpha_{11}$	V_{DC4+} V_{DC1}	$\pi - \alpha_{12}$
1	0	1	0	0	1	0	1	1	0	10	$\alpha_{11} - \alpha_{10}$	V_{DC4}	$\pi - \alpha_{11}$
0	1	1	0	1	0	0	1	1	0	9	$\alpha_{10} - \alpha_9$	V_{DC4-} V_{DC3+} V_{DC1}	$\pi - \alpha_{10}$
1	0	1	0	1	0	0	1	1	0	8	$\alpha_9 - \alpha_8$	V_{DC4-} V_{DC3}	$\pi - \alpha_9$
0	1	0	1	0	1	1	0	1	0	7	$\alpha_8 - \alpha_7$	V_{DC2+} V_{DC3}	$\pi - \alpha_8$
1	0	0	1	0	1	1	0	1	0	6	$\alpha_7 - \alpha_6$	V_{DC2+} V_{DC3-} V_{DC1}	$\pi - \alpha_7$
0	1	0	1	1	0	1	0	1	0	5	$\alpha_6 - \alpha_5$	V_{DC2}	$\pi - \alpha_6$
1	0	0	1	1	0	1	0	1	0	4	$\alpha_5 - \alpha_4$	V_{DC2-} V_{DC1}	$\pi - \alpha_5$
0	1	1	0	0	1	1	0	1	0	3	$\alpha_4 - \alpha_3$	V_{DC1+} V_{DC3}	$\pi - \alpha_4$
1	0	1	0	0	1	1	0	1	0	2	$\alpha_3 - \alpha_2$	V_{DC3}	$\pi - \alpha_3$
0	1	1	0	1	0	1	0	1	0	1	$\alpha_2 - \alpha_1$	V_{DC1}	$\pi - \alpha_2$
1	0	1	0	1	0	1	0	1	0	0	α_1	No DC source	$\pi - \alpha_1$

Table 4. SWIT codes states for negative half cyclers

S1	S2	S3	S4	S5	S6	S7	S8	Sp	Sn	Vdc	Duration	DC sources	Shift
0	1	0	1	0	1	0	1	0	1	0	α_1	No DC source	π
1	0	0	1	0	1	0	1	0	1	-1	$\alpha_2 - \alpha_1$	$-V_{DC1}$	$\pi + \alpha_1$
0	1	0	1	1	0	0	1	0	1	-2	$\alpha_3 - \alpha_2$	$-V_{DC3}$	$\pi + \alpha_2$
1	0	0	1	1	0	0	1	0	1	-3	$\alpha_4 - \alpha_3$	$-(V_{DC1+}$ $V_{DC3})$	$\pi + \alpha_3$
0	1	1	0	0	1	0	1	0	1	-4	$\alpha_5 - \alpha_4$	$-(V_{DC2-}$ $V_{DC1})$	$\pi + \alpha_4$
1	0	1	0	0	1	0	1	0	1	-5	$\alpha_6 - \alpha_5$	$-(V_{DC2})$	$\pi + \alpha_5$
0	1	1	0	1	0	0	1	0	1	-6	$\alpha_7 - \alpha_6$	$-(V_{DC5+}$ V_{DC3-} $V_{DC1})$	$\pi + \alpha_6$
1	0	1	0	1	0	0	1	0	1	-7	$\alpha_8 - \alpha_7$	$-(V_{DC5+}$ $V_{DC3})$	$\pi + \alpha_7$
0	1	0	1	0	1	1	0	0	1	-8	$\alpha_9 - \alpha_8$	$-(V_{DC4-}$ $V_{DC3})$	$\pi + \alpha_8$
1	0	0	1	0	1	1	0	0	1	-9	$\alpha_{10} - \alpha_9$	$-(V_{DC4-}$ V_{DC3} $+V_{DC1})$	$\pi + \alpha_9$
0	1	0	1	1	0	1	0	0	1	-10	$\alpha_{11} - \alpha_{10}$	$-(V_{DC4})$	$\pi + \alpha_{10}$
1	0	0	1	1	0	1	0	0	1	-11	$\alpha_{12} - \alpha_{11}$	$-(V_{DC4+}$ $V_{DC1})$	$\pi + \alpha_{11}$
0	1	1	0	0	1	1	0	0	1	-12	$\alpha_{13} - \alpha_{12}$	$-(V_{DC4+}$ V_{DC2-} V_{DC3-} $V_{DC1})$	$\pi + \alpha_{12}$
1	0	1	0	0	1	1	0	0	1	-13	$\alpha_{14} - \alpha_{13}$	$-(V_{DC4+}$ V_{DC2-} $V_{DC3})$	$\pi + \alpha_{13}$
0	1	1	0	1	0	1	0	0	1	-14	$\alpha_{15} - \alpha_{14}$	$-(V_{DC4+}$ V_{DC2-} $V_{DC1})$	$\pi + \alpha_{14}$
1	0	1	0	1	0	1	0	0	1	-15	$\pi - 2\alpha_{15}$	$-(V_{DC4+}$ $V_{DC2})$	$\pi + \alpha_{15}$
0	1	1	0	1	0	1	0	0	1	-14	$\alpha_{15} - \alpha_{14}$	$-(V_{DC4+}$ V_{DC2-} $V_{DC1})$	$2\pi - \alpha_{15}$
1	0	1	0	0	1	1	0	0	1	-13	$\alpha_{14} - \alpha_{13}$	$-(V_{DC4+}$ V_{DC2-} $V_{DC3})$	$2\pi - \alpha_{14}$
0	1	1	0	0	1	1	0	0	1	-12	$\alpha_{13} - \alpha_{12}$	$-(V_{DC4+}$ V_{DC2-} V_{DC3-} $V_{DC1})$	$2\pi - \alpha_{13}$
1	0	0	1	1	0	1	0	0	1	-11	$\alpha_{12} - \alpha_{11}$	$-(V_{DC4+}$ $V_{DC1})$	$2\pi - \alpha_{12}$
0	1	0	1	1	0	1	0	0	1	-10	$\alpha_{11} - \alpha_{10}$	$-(V_{DC4})$	$2\pi - \alpha_{11}$
1	0	0	1	0	1	1	0	0	1	-9	$\alpha_{10} - \alpha_9$	$-(V_{DC4-}$ V_{DC3} $+V_{DC1})$	$2\pi - \alpha_{10}$
0	1	0	1	0	1	1	0	0	1	-8	$\alpha_9 - \alpha_8$	$-(V_{DC4-}$ $V_{DC3})$	$2\pi - \alpha_9$
1	0	1	0	1	0	0	1	0	1	-7	$\alpha_8 - \alpha_7$	$-(V_{DC5+}$ $V_{DC3})$	$2\pi - \alpha_8$
0	1	1	0	1	0	0	1	0	1	-6	$\alpha_7 - \alpha_6$	$-(V_{DC5+}$ V_{DC3-} $V_{DC1})$	$2\pi - \alpha_7$
1	0	1	0	0	1	0	1	0	1	-5	$\alpha_6 - \alpha_5$	$-(V_{DC2})$	$2\pi - \alpha_6$
0	1	1	0	0	1	0	1	0	1	-4	$\alpha_5 - \alpha_4$	$-(V_{DC2-}$ $V_{DC1})$	$2\pi - \alpha_5$
1	0	0	1	1	0	0	1	0	1	-3	$\alpha_4 - \alpha_3$	$-(V_{DC1+}$ $V_{DC3})$	$2\pi - \alpha_4$
0	1	0	1	1	0	0	1	0	1	-2	$\alpha_3 - \alpha_2$	$-V_{DC3}$	$2\pi - \alpha_3$
1	0	0	1	0	1	0	1	0	1	-1	$\alpha_2 - \alpha_1$	$-V_{DC1}$	$2\pi - \alpha_2$
0	1	0	1	0	1	0	1	0	1	0	α_1	No DC source	$2\pi - \alpha_1$

5. Simulation results

A Simulink model for the 31-MLI is built in MATLAB Simulink environment as shown in Fig. 8.

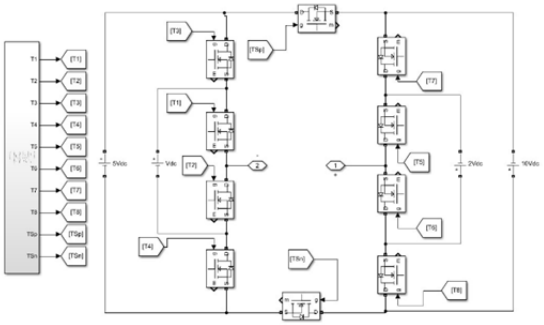

Fig. 8. Simulink model for 31-MLI

At first, the angles are simulated for the un-optimized staircase. Fig. 9 shows output voltage and current when the 31-MLI is connected with a resistive load R=180Ω.

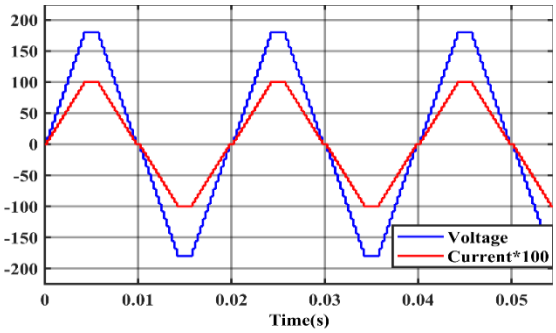

Fig. 9 31-MLI output voltage and current for unoptimized staircase angles (resistive load)

Fig. 10 shows the corresponding output voltage THD = 11.56% with significant effect of the third harmonics.

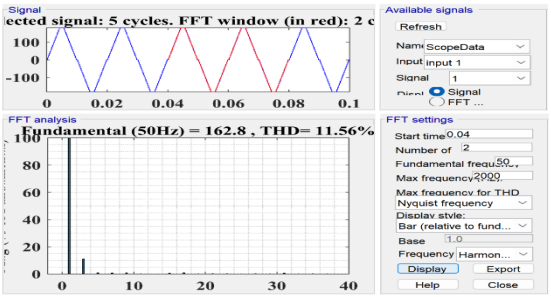

Fig. 10. Frequency spectrum for unoptimized angles

The output voltage and current under inductive load are shown in Fig. 11.

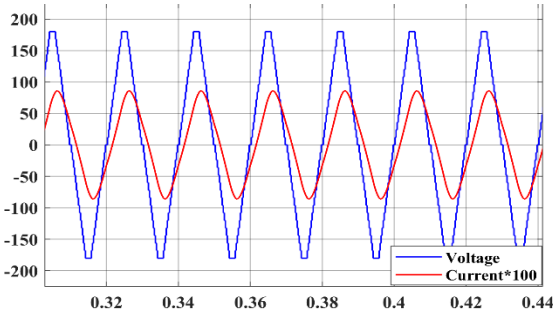

Fig. 11 31-MLI output voltage and current for unoptimized staircase angles (inductive load)

Then, the simulation is performed using IHO optimized gating angles. Fig. 12 shows the output voltage and current for a resistive load R=180Ω.

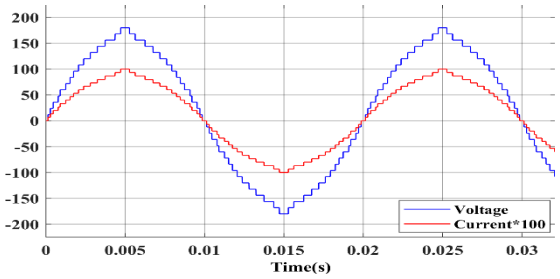

Fig. 12. 31-MLI output voltage and current for IHO angles (resistive load)

Fig. 13 shows the value of THD=4.71% which is a significant reduction, compared to THD=11.56% obtained from the unoptimized angles.

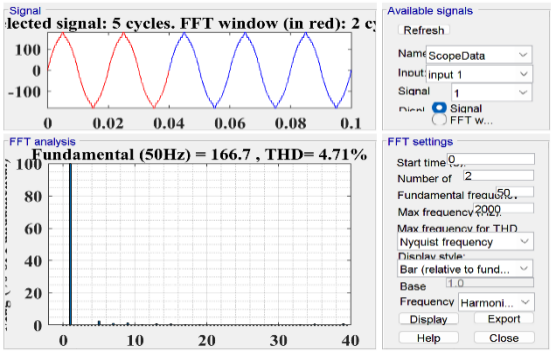

Fig. 13. Frequency spectrum for IHO for staircase

The output voltage and current for an inductive load using IHO optimized angles are shown in Fig. 14.

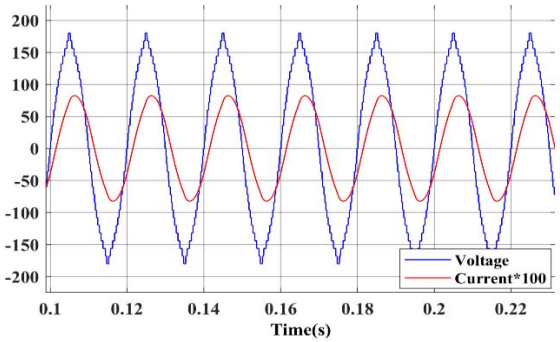

Fig. 14. 31-MLI output voltage and current for IHO optimized angles (inductive load)

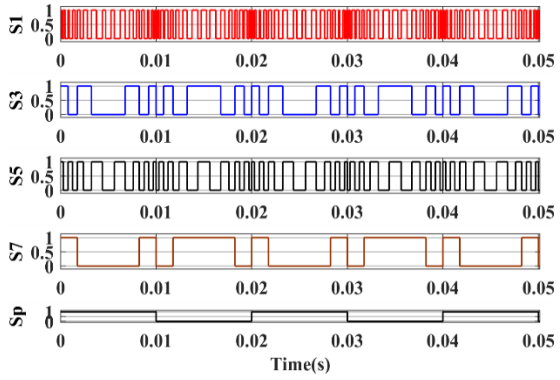

Fig. 15. Gating drive signals to the switches

Gating drive signals for switches S1, S3, S5, S7, and Sp are shown in Fig. 15.

6. Practical results

A. *Digital Controller*

Arduino board mega 2560 is employed as the digital controller for the 31-MLI. The Arduino program is initiated using the states of Tables 3 and 4. The Arduino digital outputs are connected to the TLP 250 optocoupler, providing electrical isolation from the power circuit. Figs. 16 to 20 show the gating signals to the switched S1, S3, S5, S7, and S_p respectively. While the adjacent switches S2, S4, S6, S8 and S_n are fed with the complementary mode of the above switches to avoid short circuits.

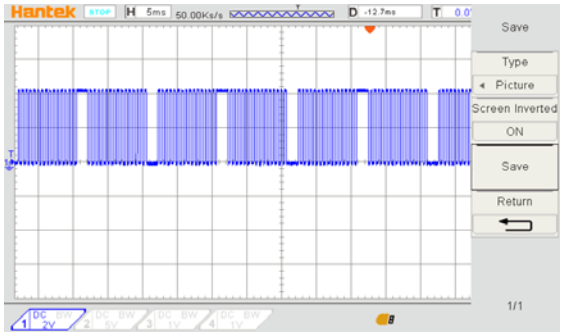

Fig. 16. Gating signal for S_1

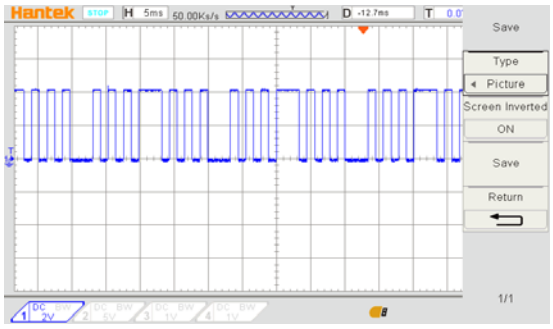

Fig. 17. Gating signal for S_3

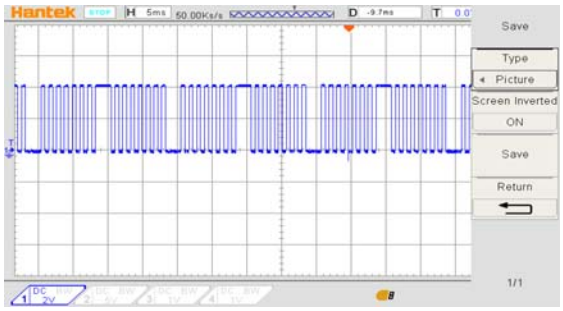

Fig. 18. Gating signal for S_5

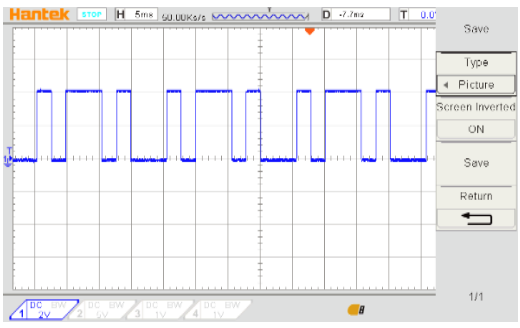

Fig. 19. Gating signal for S_7

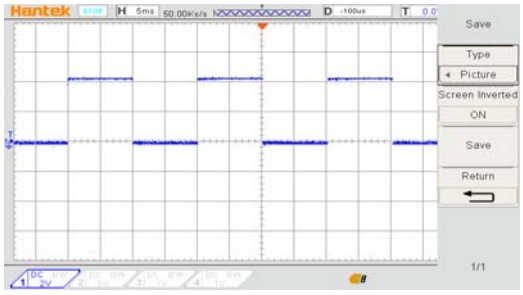

Fig. 20. Gating signal for S_p

The proposed MLI inverter is configured to obtain 31-levels in the output voltage, hence, 15 gating angles are needed. It is well known that Arduino kit is widely affordable, and this will reduce the overall cost of prototyping the MLI.

B. *Experimental Results*

The MLI inverter experimental set-up is shown in Fig. 21

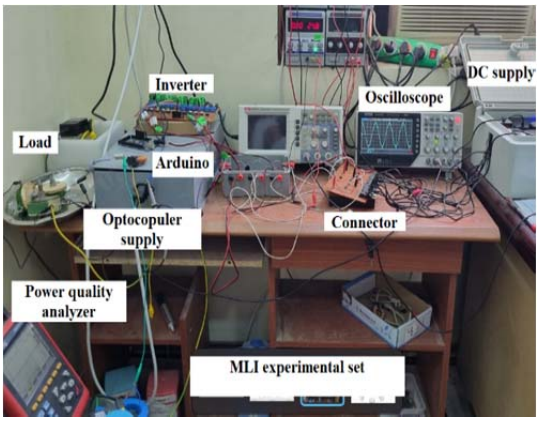

Fig. 21 MLI experimental set-up

The staircase output voltage is first determined using 5^0 per step such that $\alpha_1 = 5°$, $\alpha_2 = 10°, \ldots\ldots\ldots \alpha_{15} = 75°$ for unoptimized angles. Fig. 22 shows the 31-levels staircase obtained.

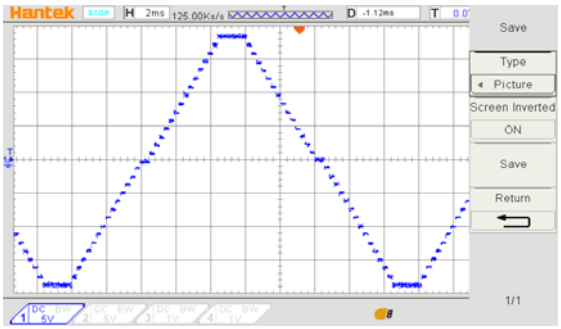

Fig. 22 31-MLI output voltage for unoptimized gating angles

The corresponding THD is shown in Fig. 23 measured using power quality analyzer HZCR-5000. It shows a relatively high value of THD about 11.3%.

To reduce the THD, the optimized angles from IHO are used for m= 0.8, for example. The optimized angles are extracted from Fig. 7 for IHO as follows:

$$\alpha_1 = 2.44^{\circ}, \alpha_2 = 5.21^{\circ}, \alpha_3 = 8.42^{\circ}, \alpha_4 = 14.21^{\circ}$$

$$\alpha_5 = 16.36^{\circ}, \alpha_6 = 22.64^{\circ}, \alpha_7 = 27.46$$
$$\alpha_8 = 31.65^{\circ}, \alpha_9 = 37.1^{\circ}, \alpha_{10} = 42.92^{\circ}$$
$$\alpha_{11} = 50.53^{\circ}, \alpha_{12} = 58.42, \alpha_{13} = 67.46^{\circ}$$
$$\alpha_{14} = 78.64^{\circ}, \alpha_{15} = 85^{\circ}$$

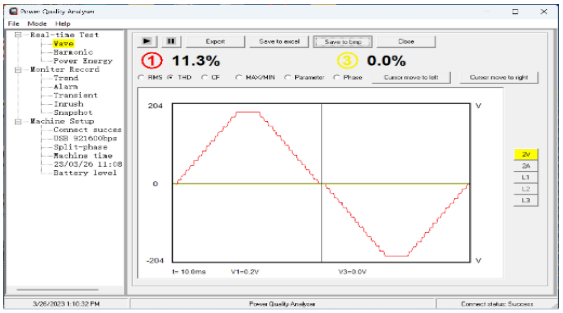

Fig. 23 THD for 31-MLI output voltage for unoptimized angles

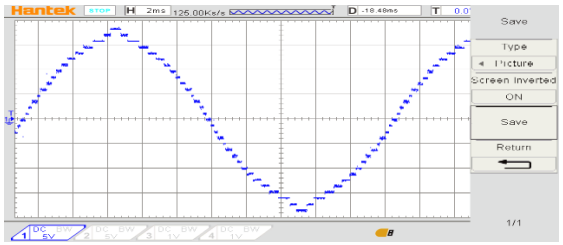

Fig. 24. 31-MLI output voltage for IHO

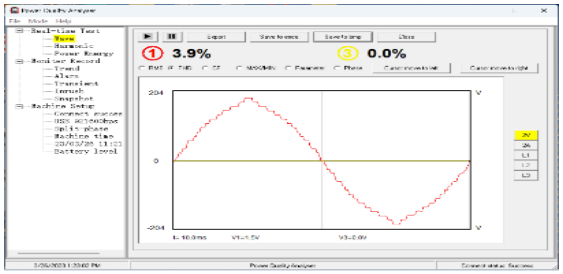

Fig. 25 THD for 31-MLI output voltage for IHO

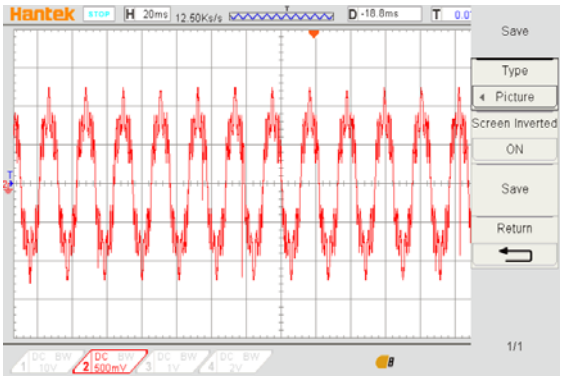

Fig.26 31-MLI output current for resistive load

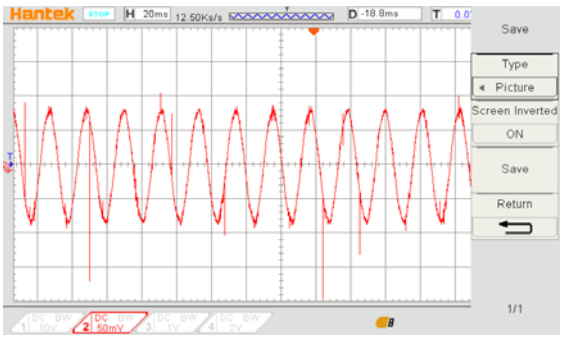

Fig.27 31-MLI output current for inductive load

Fig. 24 shows the output voltage for 31-MLI when using the IHO solution for the gating angles. The wave shape is very close to the sine waveform.

The THD is recorded as =3.9% as shown in Fig. 25 which is much smaller compared to the value of THD=11.3% for unoptimized gating angles.

Figs. 26 and 27 show the output currents for resistive load (R=180Ω) and inductive load (R=180Ω, L=300mH) respectively.

The output current THD is about 3.4% as shown in Fig. 28.

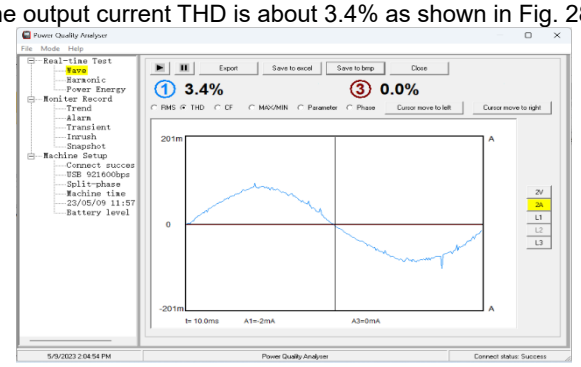

Fig. 28 THD for 31-MLI output current for IHO

7. Conclusion

The research achieves the reduction of THD of the output voltage and current using IHO algorithm in the proposed 31-MLI with the reduced number of switches and DC sources used. The DC sources are added or subtracted from each other to obtain the desired 31-levels staircase at the MLI output. The levels can be extended to any desired values by adding DC sources and power switches while keeping the ring topology of the MLI in its general form. The staircase levels are adopted in this work and the final output shape is quasisquare type. Reducing the percentage of THD requires an optimized angles to drive the switches. The optimal solution algorithms from GA, GWO, and SMA are selected for their efficiency in the field of optimization techniques. Each algorithm has distinct results in terms of reducing THD for a specified range of modulation index. These features of the three algorithms to cover the total range of modulation index are collected and tabulated in the IHO and adopted to control the operation of the 31-MLI. Output voltage THD of 3.9% is achieved using IHO compared with 11.3% when using the unoptimized solutions. This is about 65% THD reduction, and accordingly, this enhances the efficiency of the MLI system. A good agreement between the simulation and experimental results has been achieved. The performance might be further improved if other algorithms are employed to develop the IHO idea, and this is an open field for future research.

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