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doi:10.15199/48.2024.07.48

High Performance Porous Silicon Substrate for the Integration of Millimeter-Wave Passive Devices

***Abstract**. In this letter, the performance of porous silicon (PSi) substrate dedicated for millimeter-wave integrated passive circuits is figured out by integrating mm-wave bandpass filter (MBPF) centered at 60 GHz. PSi is fabricated by electroporisification starting from cheap standard resistivity (1-10 Ω.cm) Si substrate. Besides on its suitability for passive mm-wave circuit integration, this PSi is compatible with CMOS process especially when localized porosification technique is considered. Compared with the conventional MBPF implemented on standard (Std) Si substrate, the MBPF design on PSi shows interesting performance, thanks to the high resistivity of the PSi substrate leading to reduced harmful effects of the substrate.*

***Streszczenie.** W tym liście wydajność porowatego podłoża krzemowego (PSi) przeznaczonego do scalonych układów pasywnych fal milimetrowych jest obliczona poprzez zintegrowanie filtru środkowoprzepustowego fal milimetrowych (MBPF) wyśrodkowanego na 60 GHz. PSi jest wytwarzany przez elektroporyzację, zaczynając od taniego standardowego podłoża Si o rezystywności standardowej (1-10 Ω.cm). Poza przydatnością do pasywnej integracji obwodów fal milimetrowych, ten PSi jest kompatybilny z procesem CMOS, zwłaszcza gdy rozważana jest technika miejscowej porowatości. W porównaniu z konwencjonalnym MBPF zaimplementowanym na standardowym (Std) podłożu Si, projekt MBPF na PSi wykazuje interesującą wydajność, dzięki wysokiej rezystywności podłoża PSi, co prowadzi do zmniejszenia szkodliwych skutków podłoża. (**Wysokowydajne porowate podłoże krzemowe do integracji urządzeń pasywnych wykorzystujących fale milimetrowe**)*

Keywords: Bandpass filter (BPF), coplanar waveguide (CPW), millimeter-wave, porous silicon.
Słowa kluczowe: Filtr pasmowoprzepustowy (BPF), falowód współpłaszczyznowy (CPW), fala milimetrowa, krzem porowaty.

Introduction

In the last decade the millimeter-wave (mm-wave) band above 30 GHz attracted researchers and industrials. The task of designing circuit for wireless communication was very challenging due to the increase of various kinds of losses at these frequencies. Realizing fully integrated circuit on standard CMOS at the mm-wave band further complicates the design especially for the passive integrated circuits which are highly affected by the losses coming from silicon based substrate [1, 2].

Indeed, many works have been reported in the state of the art of literature to address the issue of substrate losses in order to improve the quality factor of passive devices [3, 10]. By observing the mentioned references, it could be concluded that the main focus has been made on the realization of substrates illustrating, in the same time, small relative permittivity and high resistivity. However, it is pertinent to note that the proposed solution must be compatible with CMOS process in order to enable integration of passive and active circuits on the same chip, therefore, allowing the fabrication of fully integrated systems [11]. Based on these conditions, the current article presents an efficient technique allowing the integration of high quality passive circuit, namely, the porosification of localized area in the Si Bulk to obtain which is known in the literature as localized porous silicon [12, 13]. Nonetheless, before the application of localized porous silicon technique it is necessary to demonstrate this concept through the realization of wafers based on porous silicon.

Consequently, after the description of the fabrication process of PSi, this latter will be put under test by integrating a bandpass filter operating around 60 GHz. Filter design remains critical at the mentioned frequency because the designer must tradeoff between many performances, nonetheless, such passive circuit will figure out the usefulness of the PSi as future technique to achieve high performance filters or other passive integrated circuits or devices.

Experimental

Porous silicon fabrication

A standard resistivity (1–10 Ω.cm) of p-type silicon wafer is exposed to an electrolyte that is a 2:1 mixture of hydrofluoric acid (HF 49%) and ethanol, this electrochemical etching platform is used inside a fume-hood at room temperature. The anodization is then conducted at a current density of 10 mA/cm^2 during different etching periods corresponding to different PSi thicknesses [14]. Two substrates have been realized depending on the porous Si layer, namely, a porous Si layer of 50 and 100 µm. This process yields to the mesoporous PSi substrate, the pores sizes of samples were measured by a field emission scanning electron microscope (SEM, JSM-7610 FPlus) under 3.8 keV electron acceleration voltage, with an average porosity of 65% (evaluated by weight measurements) and with a pore size of less than 5 nm in diameter, as shown in Figure 1.

As it will be discussed in next sections, it is interesting to observe the impact of thickness variation on the bandpass filter performances. However, before talking about filter design the electrical characteristics of the obtained substrates will be investigated in the next section.

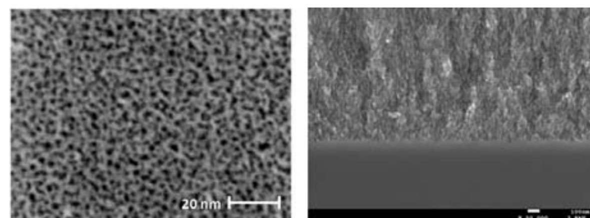

Fig. 1. Top view SEM photograph of the mesopores (left) and Cross-sectional SEM image (right) of PSi.

Substrate electrical performance

Integration of CPW lines

In order to evaluate the quality of substrate and due to their high sensitivity to substrate effects at the SiO_2/Si interface, CPW transmission lines were fabricated to extract

the substrate losses, the effective resistivity, and effective dielectric permittivity (see Figure 2a). The process integration of CPW lines was conducted after the porisification of both substrates, these latters are annealed for 2 hours, first in oxygen at 300 °C to reinforce the structure, then under nitrogen at 420 °C to hold steady it. On the top of both substrates, a 500-nm silicon oxide (SiO_2) is deposited at 300 °C by plasma-enhanced chemical vapor deposition (CVD), followed by a 1-µm-thick layer of aluminum deposited by physical vapour deposition for the definition of the RF transmission lines and devices [15, 16]. The dimensions of the CPW line are: a central signal line width of 38 µm, ground line widths of 208 µm, a spacing of 18 µm between the signal line and the ground lines, and a line length of 8 mm, as illustrated in the cross section of the CPW line in Figure 2b.

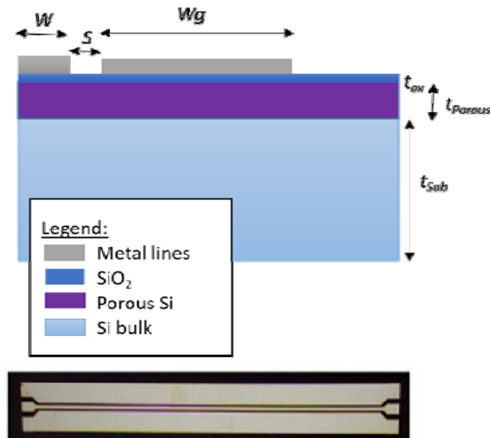

Fig. 2. (a) Illustration of the Si-based substrate and (b) Top view of the CPW line structure

Substrate performances

The extraction of the electrical properties is undoubtedly operation to efficiently examine the proposed PSi and compare its performances with bulk silicon. From the measured S-parameters, we extract the effective resistivity (ρ_{eff}), effective relative permittivity ($\varepsilon_{r,eff}$) and RF line losses using the method described in [17].

The S-parameters measurements were performed through an on-wafer characterization of CPW lines using an Agilent 2-port vectoriel network analyzer (PNA)-X in the frequency range from 10 MHz to 67 GHz. The obtained performances are summarized in Table 1 where they are compared with those of Si bulk and the results are stable above 10 GHz.

The PSi substrate exhibits excellent effective resistivity (5.9 kΩ·cm) compared with the Std substrate's effective resistivity which is only few of Ohms. Also, the scaling down of ε_{reff} from 11.7 to 3.5 is a success because it will offer significant reduction of parasitic capacitances between adjacent integrated circuit nodes. This feature has the effect of reducing crosstalk through the substrate.

Moreover, the most important feature sketched in Table 1 is the significant increase of the quality factor of the integrated CPW transmission lines. This noteworthy growing of quality factor can be justified by the diminution of linear losses (α). As known, these losses are the combination of the losses coming from substrate and conductor, however, at the investigated frequency range the conductor losses are negligible compared with substrate one, therefore, diminution of the substrate losses are due to the increase of the effective resistivity of the proposed PSi.

All the discussed performances have encouraged us to go toward the integration of more complex integrated circuits, and as a proof of concept we are going to tackle the integration of bandpass filter in the next section.

Results and discussion

The proposed PSi substrate is used to integrate a mm-wave bandpass filter. In order to design the bandpass filter on the proposed PSi, the values of resistivity and permittivity experimentally extracted have been considered during the design phase and the electromagnetic simulation.

A planar ring resonator structure was adopted in the design of this BPF [18]. The filter is designed at around 60 GHz frequency which is one of the dedicated frequencies for high data rate wireless personal area network. Our objective is not to propose an original configuration of bandpass filter but it consists to figure out the suitability of the proposed PSi for the integration of high quality passive circuits, therefore, we will not detail the design procedure here as it was well explained in [18]. The only difference between the filter designed in [18] was the position of the feeding line which are not aligned but there is a 90° angle between them. Nonetheless, the particularity in this work is the use of CPW configuration instead of microstrip structure used in [18]. The choice of CPW configuration is crucial because it keeps the filter near to the PSi layer (Figure 2*a*) enabling thus full benefit from the PSi high insulating properties allowing to highlight its interest. In addition, having the ground on the same face as the filter prevents the use of vias which increase the losses coming from shunt resistances. Therefore, we left only with the impact of the substrate since our main target is to evaluate the PSi.The filter was fabricated with the following final physical dimensions (all in µm): W1=10, W2=25, W3=20, L1=750, L2=510, L3=85, the layout and fabrication of the filter are depicted in Figures 3a and 3b. It is observed in Figure 3c the poor quality of the metal tracks of the fabricated filter which is due to the poor quality of the lithography of the narrow lines; such fabrication limitation could lead to increase the conductive losses that badly impact the insertion losses of the filter as it will be seen on the measured performance.

Table 1. Obtained parameters values of the substrate from the extraction of CPW S-parameter measurements

Substrate	Nominal resistivity [Ω·cm]	Effective resistivity ρ_{eff} [kΩ·cm]	Permittivity $\varepsilon_{r,eff}$	Losses α [dB/mm]	Quality factor Q@26/60 GHz
Std	1 - 10	0.01	11.7	3.8	2.1 / 4.9
PSi [50µm]	1 – 10	5.9	3.5	0.18	25.45 / 58.74
PSi [100µm]	1 - 10	7	3.28	0.18	24.64 / 56.86

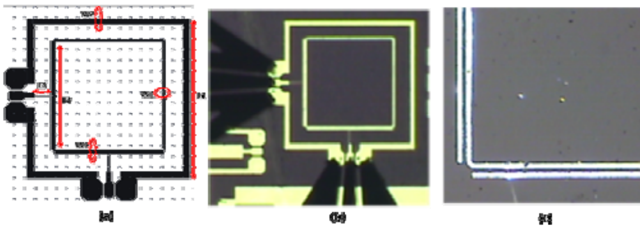

Fig.3. (a) Layout, (b) Photography being measured on the probe station using GSG picoprobes of mm-wave bandpass filter in CPW configuration and (c) Metal tracks of small dimensions

The characterization of the fabricated filters is carried out from 10 MHz to 120 GHz using an Agilent PNA-X vector network analyzer. The measured data are plotted against the simulated ones in Figure 4 and 5. Both filters are well matched since they show 23 and 27 dB of return loss (|S11|) for PSi 50 µm and PSi 100 µm, respectively. It could be noted the impact of PSi thickness on the electrical performance of the filter where we can see the frequency shift in the poles in the responses of |S11|, also the shift in the transmission zero in the upper stop band as shown in the responses of |S21|.

As sketched in Table 1, the variation of PSi thickness, immediately impact the value of $\varepsilon_{r,eff}$ leading to a frequency shift. Moreover, it is important to note the significant shift of the transmission zero between simulation and measurement. This difference could be explained by the process variation which impacts the dimension of the feed lines as explained on Figure 3c. Knowing that those feeding lines are the responsible in generating the transmission zero and any geometrical modification can lead to a frequency shift.

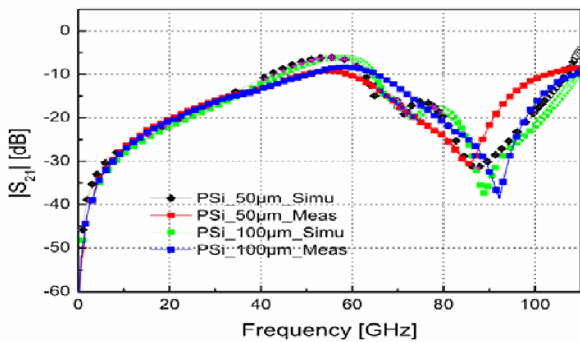

Fig.4. Simulated and measured insertion loss for mm-wave filter implemented on PSi 50 and 100 µm substrates

The measurement results show good agreements with the simulation. Furthermore, it could be noted on the curve of |S21| the increase of insertion loss (IL) of 1.5 dB in the measurement in comparison with simulation. The increase of the IL is due to the increase of various kinds of losses especially the conductor losses due to the quality of the fabrication as stated above.

However, since the objective of this article was to put under test the PSi substrate, it becomes important to identify the reason of such increase in the insertion losses which is not in line with the high quality factor showed with the measured CPW lines in section 2.b. To do so, the two following simulations were performed.

In the first the MBPF was simulated using three cases of metal strips conductivity, namely, perfect conductor, very bad conductor (0.2 10^7 S/m) and Aluminum. Figure 6 shows the comparison, where we could note that the IL increases with the deterioration of the conductivity. In fact lower conductivity leads to greater conductor loss which is

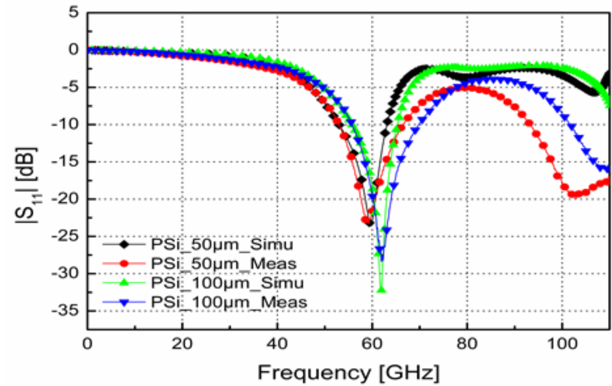

Fig.5. Simulated and measured return loss for mm-wave filter implemented on PSi 50 and 100 µm substrates

translated on the increase of the constant of attenuation, therefore, the IL becomes more important. Also, it is interesting to note how the shape of filter response is kept almost unchanged as well as the selectivity; such behavior reveals that the increase of attenuation constant does not affect the unloaded quality factor of the filter.

Figure 7 shows the second simulation which was carried out to understand the increase of IL in PSi based MBP. In this case, the considered MBPF has been simulated on two substrates, the PSi (ρ_{eff}=5.9 kΩ·cm) and the standard Silicon (ρ=10 Ω·cm). The conductor was set as perfect one in order to keep only the substrate impact. Indeed, the advantage of the PSi is well noted compared with the standard silicon.

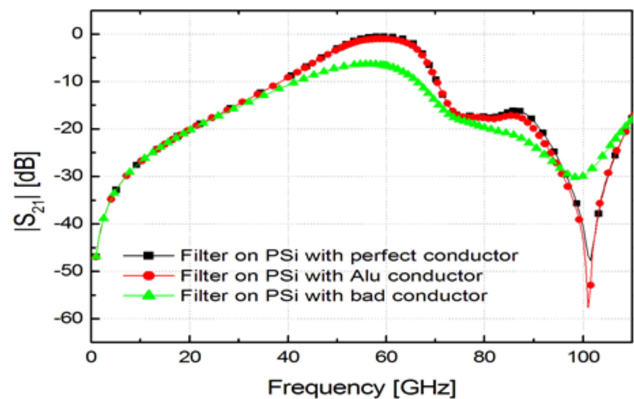

Fig.6. Impact of the quality of strips conductor inMBPF performance

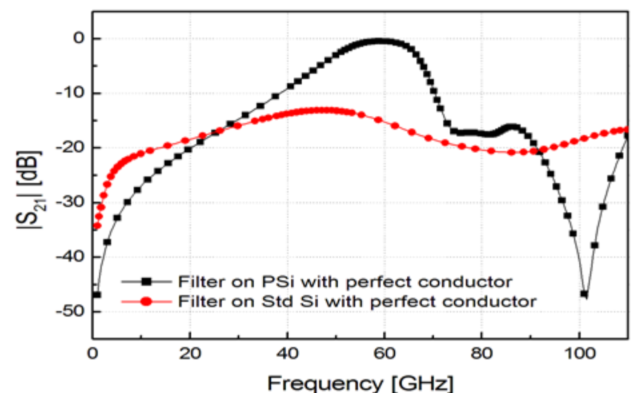

Fig.7. Impact of the substrate in the MBPF performance

In this case the shape of the response change significantly with an increase in IL as well as a widening in the bandwidth, such behavior is due to the dramatic fall of the unloaded quality factor of the filter.

Based on the above discussion we can conclude that the reason of the degradation of the IL in the measured data (Figure 4) is due to the increase of the metallic losses originating from the poor lithography quality of the narrow strips. Once the reason of the measured ILs identified, it could be concluded the advantage of the utilization of PSi substrate instead of Std silicon in the integration of mm-wave passive integrated devices. A performance comparison with the recently reported BPFs is given in Table 2

Table 2. Performance comparison of PSi-based mm-wave filter with BPFs implemented in CMOS technology

Ref.	Center Frequency (GHz)	RL (dB)	IL (dB)	Tech. And Method
[18]	60	> 10	4.9	0.18-μm CMOS
[19]	67	22.2	2.6	0.13-μm SiGe (Bi)-CMOS
[20]	85	25	3.15	Si IPD QMSIW cavity resonator
[21]	34.5	18.3	1.6	130nm-CMOS
This work (PSi_50μm)	**60**	**23**	**0.5**	**PSi CPW**

Conclusion

In this letter, a mm-wave bandpass filter around 60 GHz is integrated on an original PSi substrate. The substrate parameters obtained from the extraction of S-parameter measurements, allowed reaching competitive performance of the designed filter. In addition, the proposed porous silicon substrate shows significant advantage on the standard silicon, since, it offers quality factor ten times greater compared to that of the standard substrate leading to high performance integrated passive devices.

Acknowledgements. Authors would like to thanks Pr J.-P. Raskin for the fabrication of the filter in Winfab of ICTEAM, UCL, Belgium and Pr S. Bourdel for the measurements in IMEP-LAHC, Univ Grenoble, France.

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